International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 05 | May -2017 www.irjet.net p-ISSN: 2395-0072

LOW POWER BASED DUAL MODE LOGIC GATES USING POWER GATING TECHNIQUE

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Abstract - *In this paper, we present the design and enactment D- FLIP-FLOP, SR FLIP-FLOP, J-K FLIP-FLOP using dual mode logic with power gating procedures. This model is used for designing consecutive circuits whose circuit has been done in TANNER, the output waveform is displayed on W-EDIT and delay, average power calculations have been done for these circuits for value of supply i.e. 1.2V.it is use TSMC0.18 Technology.*

Key Words: **D- FLIP-FLOP, SR FLIP-FLOP, J-K FLIP-FLOP, TANNER EDA TOOL**

1. INTRODUCTION

LUCIDITY optimization and recital are basic tasks for digital circuit designers. The logical effort (LE) method was to be offered, for easy and fast appraisal and optimization of delay in CMOS logic paths. Because of its the LE method has become a very popular tool for the designing and developing the purposes and is adopted to be the basis for several computer-aided-design tools. DML gates are achieved very high speed. Even if LE is mainly used for usual CMOS logic gates it is also shown to be valuable for other logic families, such as the pass transistor logic. The dual mode logic (DML), which is converted between two modes of operation. It is contained at 1) static mode and 2) dynamic mode. Static mode is to be stable and it attains very low power rakishness. Dynamic mode achieves very high-speed logic mode is not to be on constant one. It will provide high elasticity. The dual mode logic intimate cannot use logical energy policy.

1.1 Dual Mode Logic gates

A basic DML gate style is serene of a static gate and an extra transistor *M*1, whose gate is connected to a large-scale clock signal DML gates present two possible topologies: 1) Type *A* and 2) Type *B*. In the static mode of operation, the transistor M1 is turned moldy by applying the high Clk signal for Type *A* and low Clk for Type *B* topology. To operate the gate in the dynamic mode, the Clk is enabled, allow for two separate stages: 1) precharge and 2) evaluation. During the precharge phase, the output is charged to *V*DD in Type *A* gates and squared to GND in Type *B* gates. During appraisal, the output is appraised per the values at the gate inputs.

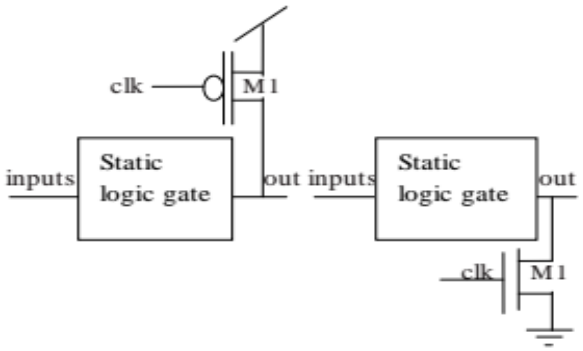

Fig -1: Type A & Type B of Dual Mode Logic

1.2 PRPOSED SYSYTEM

To reduce power in circuits two power gating procedures, namely Sleep and Stack Sleep technique are instigated and the results of best technique are detected.

1. Sleep Technique:

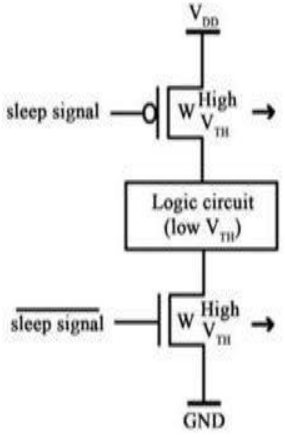

Fig -1: Sleep Technique

This procedure uses the sleep transistor amongst both VDD and the pull up network and amid GND and pull down network.

2. Stack Sleep Technique

The obligatory stack and the sleep transistor techniques are collective to get the sleepy stack structure. The role of sleep transistors in sleepy stack is same as of the sleep transistor in sleep transistor method.

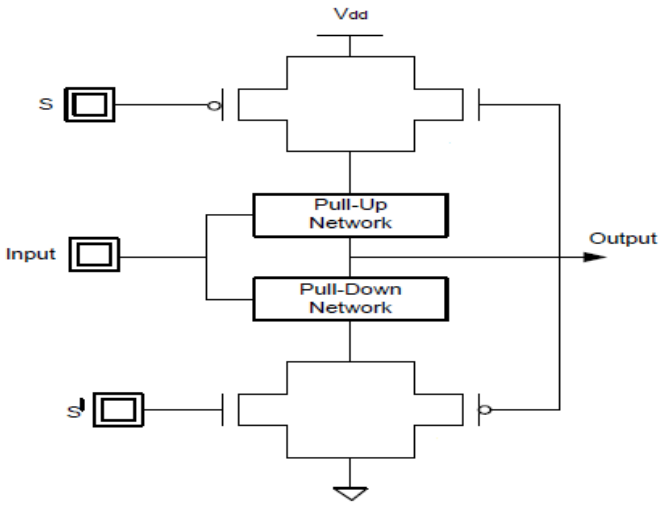

Fig -2: Stack Sleep Technique

3. Dual Sleep Technique

The Dual sleep tactic has the advantage of using the two extra pull up and two extra pull down transistors in sleep mode either in OFF state or in ON state. In regular mode when S=1 the pull down NMOS transistor is in ON state and in the pull up network the PMOS sleep transistor is in ON state since S"=0. During sleep mode state S is forced to 0 and hence the pull down NMOS transistor is in OFF state and PMOS transistor is in ON state and in the pull up network, PMOS sleep transistor is OFF while NMOS sleep transistor is ON. So, in sleep mode state a PMOS is in series with an NMOS both in pull up network and pull down network which cuts the power dissipation. Type B Active PSEUDO NMOS with Dual Sleep Gating Technique.

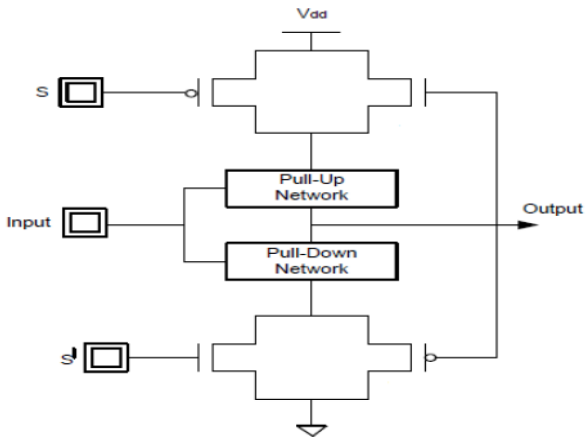

Fig -3: Dual Sleep Technique

2. D FLIP-FLOP

The **D Flip Flop** is by far the most vital of the clocked flip-flops as it certifies that ensures that inputs S and R are never equal to one at the same time. The D-type flip flop are raised from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input. Then this single data input, labelled D, is used in place of the "set" signal, and the inverter is used to generate the complementary "reset" input thereby making a level-sensitive D-type flip-flop from a level-sensitive RS-latch as now S = D and R = not D .

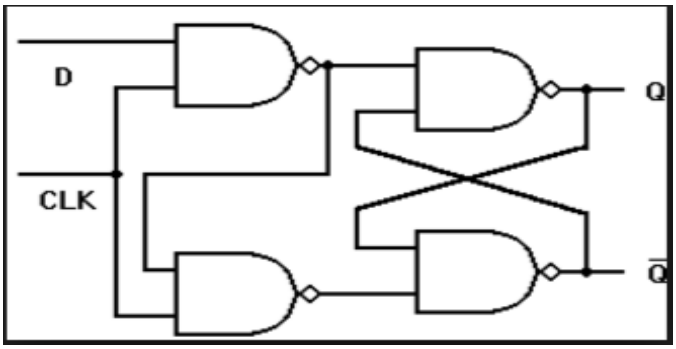

Fig -4: D Flip-Flop

Table -1: Truth Table of D Flip-Flop

Inputs		Outputs		Comments
E	D	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	1	Rset
1	1	1	0	Set

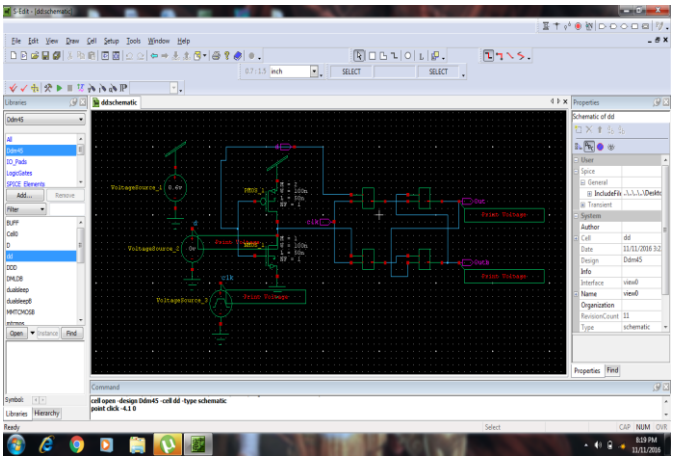

Fig -5: D Flip-Flop in Tanner EDA tool

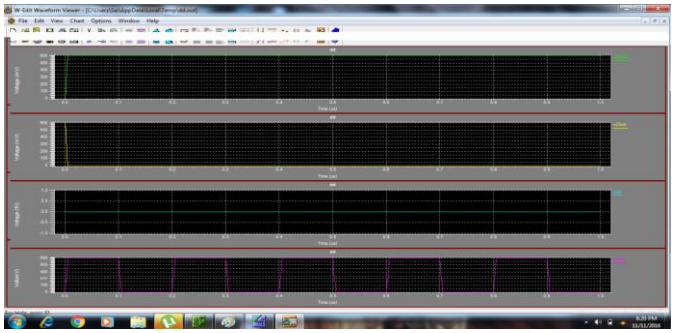

Fig -6: Waveform of D Flip-Flop in Tanner EDA tool

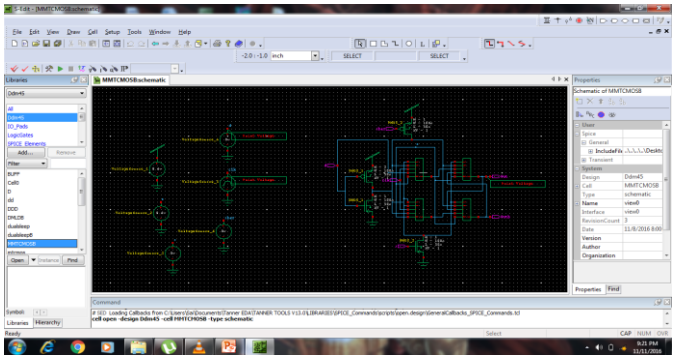

Fig -7: D Flip-Flop in Tanner EDA tool using Sleep A Technique

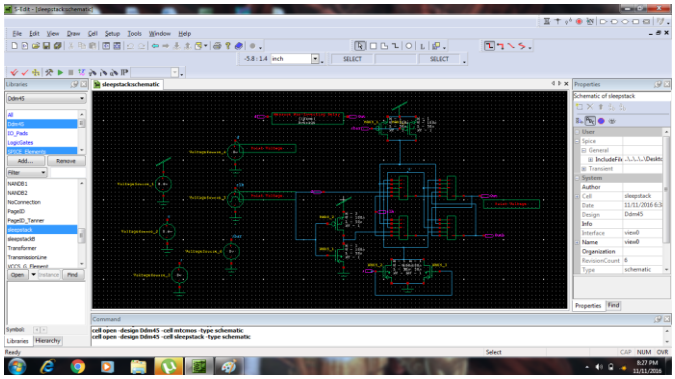

Fig -8: D Flip-Flop in Tanner EDA tool using Stack Technique

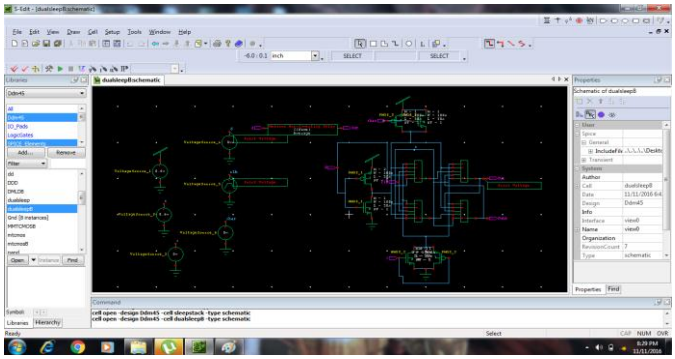

Fig -9: D Flip-Flop in Tanner EDA tool using Dual Sleep Technique

3. S-R FLIP-FLOP

The SR (Set-Reset) flip-flop is one of the meekest sequential circuits and consists of two gates connected as shown in Fig. 5. Bill that the output of each gate is connected to one of the inputs of the other gate, charitable a form of positive criticism or 'cross-coupling'. The circuit has two active low inputs marked S and R, 'NOT' being signposted by the bar above the letter, as well as two outputs, Q and Q. Table 2 shows what happens to the Q and Q outputs when a logic 0 is applied to either the S or R inputs.

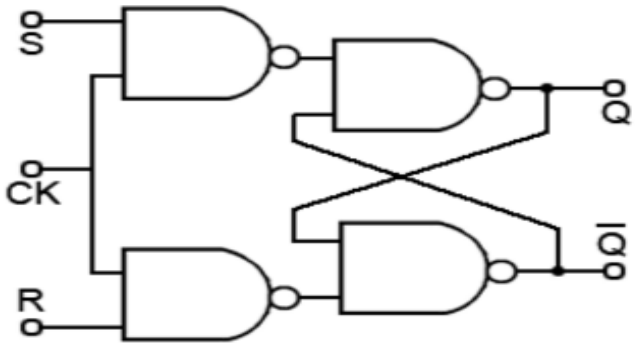

Fig -10: S-R Flip-Flop

Table -2: Truth Table of S-R Flip-Flop

Inputs			Outputs		Comments
E	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
1	0	0	Q_n	$\overline{Q_n}$	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	x	x	Indeterminate

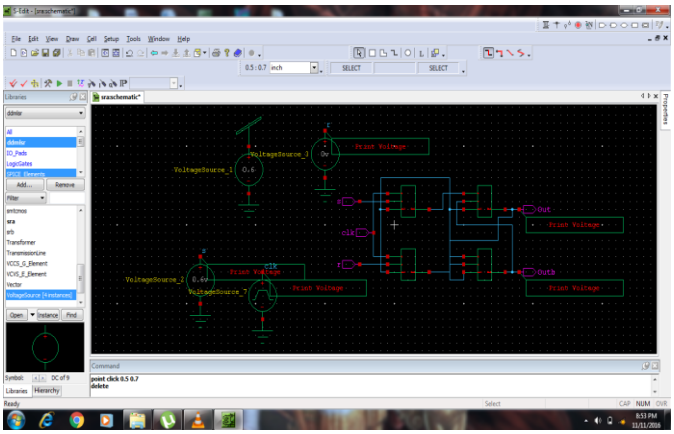

Fig -11: S-R Flip-Flop in Tanner EDA tool

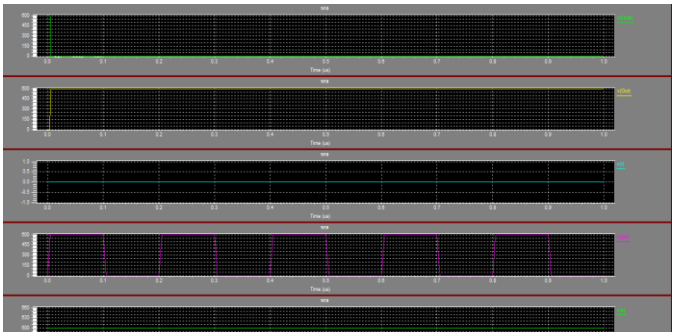

Fig -12: Waveform of S-R Flip-Flop in Tanner EDA tool

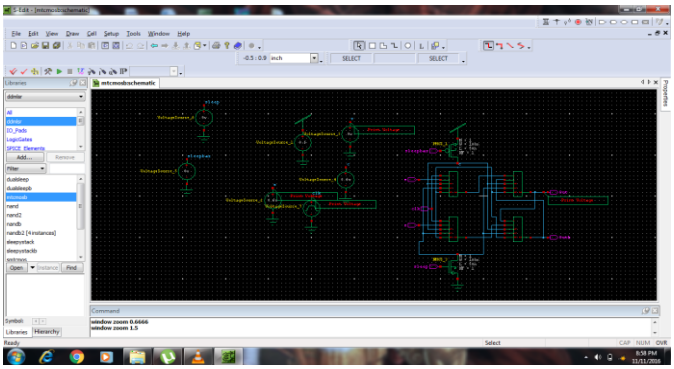

Fig -13: S-R Flip-Flop in Tanner EDA tool using Sleep Technique

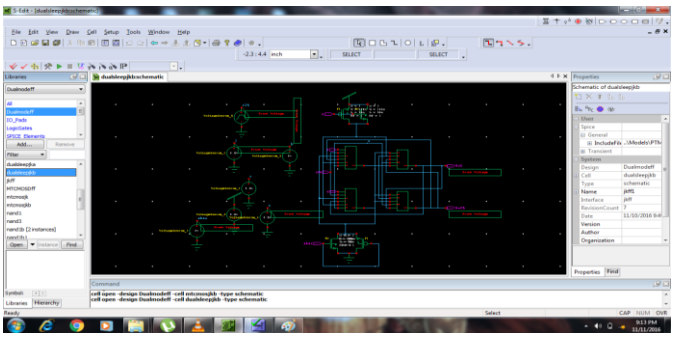

Fig -14: S-R Flip-Flop in Tanner EDA tool using Sleep Stack Technique

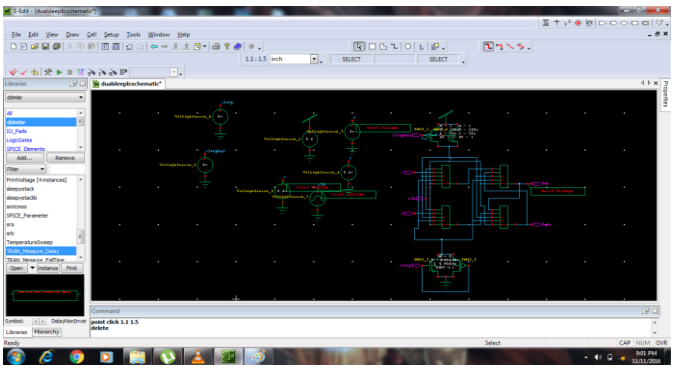

Fig -15: S-R Flip-Flop in Tanner EDA tool using Dual Stack Technique

4. J-K FLIP-FLOP

The J-K flip-flop is the handiest of the basic flip-flops. It has the input- following character of the clocked D flip-flop but has two inputs, habitually labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge. The inputs are labeled J and K in decency of the architect of the device, Jack Kilby. If J and K are both low, then no change occurs. If J and K are both high at the clock edge, then the output will clasp from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no vague states. It can also act as a T flip-flop to accomplish toggling action if J and K are tied together. This toggle bid finds extensive use in binary counters.

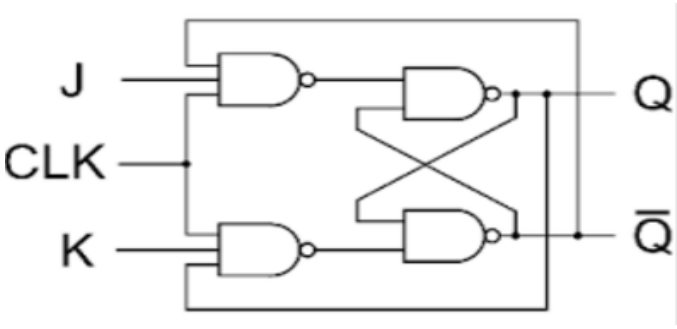

Fig -16: J-K Flip-Flop

Table -3: Truth Table of J-K Flip-Flop

Inputs			Outputs		Comments
E	J	K	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	Q_n	$\overline{Q}_n$	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	$\overline{Q}_n$	Q_n	Toggle

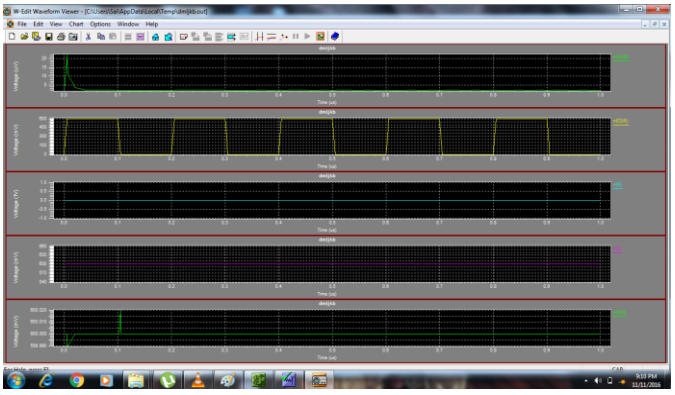

Fig -17: Waveform of J-K Flip-Flop in Tanner EDA tool

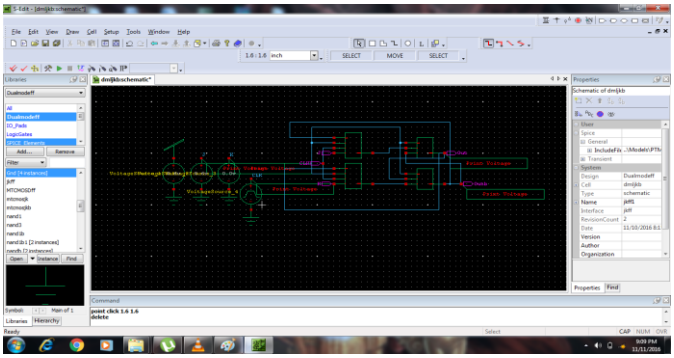

Fig -18: J-K Flip-Flop in Tanner EDA tool

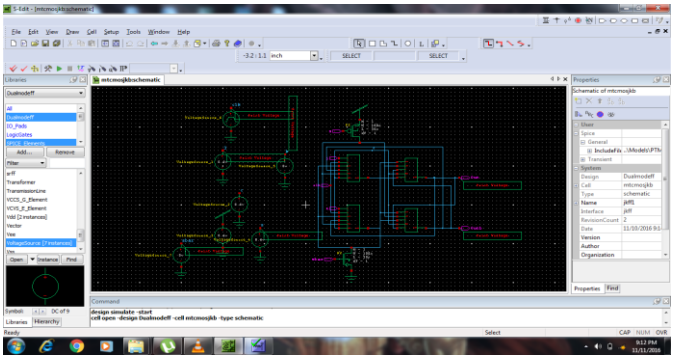

Fig -19: J-K Flip-Flop in Tanner EDA tool using Sleep Technique

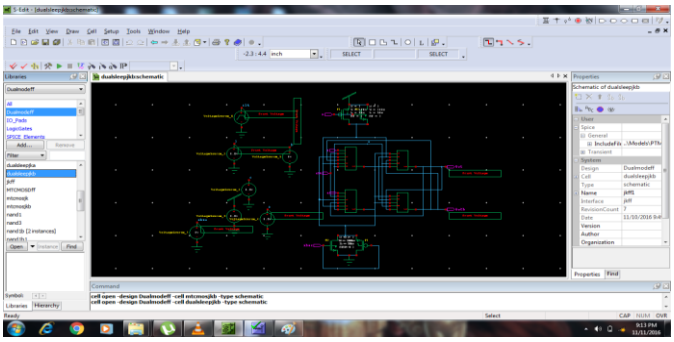

Fig -20: J-K Flip-Flop in Tanner EDA tool using Sleep Stack Technique

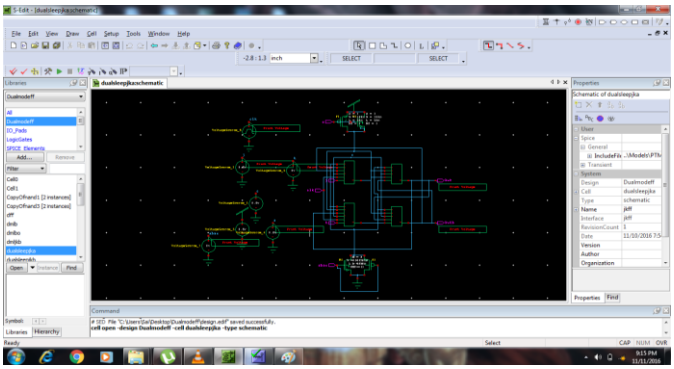

Fig -21: J-K Flip-Flop in Tanner EDA tool using Dual Stack Technique

5.RESULTS

D FLIP-FLOP	POWER DISSIPATION
D FLIP-FLOP	$3.57e^{-7}$
D FLIP-FLOP USING SLEEP TECHNIQUE	$5.01e^{-9}$
D FLIP-FLOP USING SLEEP STACK TECHNIQUE	$3.15e^{-8}$
D FLIP-FLOP USING DUAL STACK TECHNIQUE	$4.52e^{-10}$

S-R FLIP-FLOP	POWER DISSIPATION
S-R FLIP-FLOP	$3.30e^{-8}$
S-R FLIP-FLOP USING SLEEP TECHNIQUE	$4.04e^{-9}$
S-R FLIP-FLOP USING SLEEP STACK TECHNIQUE	$1.25e^{-9}$
S-R FLIP-FLOP USING DUAL STACK TECHNIQUE	$3.58e^{-10}$

J-K FLIP-FLOP	POWER DISSIPATION
J-K FLIP-FLOP	$1.46e^{-9}$
J-K FLIP-FLOP USING SLEEP TECHNIQUE	$8.87e^{-11}$
J-K FLIP-FLOP USING SLEEP STACK TECHNIQUE	$8.06e^{-10}$
J-K FLIP-FLOP USING DUAL STACK TECHNIQUE	$3.80e^{-11}$

6. CONCLUSIONS

While effective in the dynamic mode, sub threshold DML gates achieve an enhancement in speed compared to a standard CMOS, whereas scattering more power and in the static mode, a reduction of power overindulgence is achieved, at the expense of a decrement in performance. The different methods of power gating applied to the DML logic have concentrated the power dissipation further. LE approach for CMOS-based DML logic networks was presented. The proposed approach allowed an efficient optimization of DML logic networks for determined performance in the dynamic mode of operation, which was the focus of this paper. DML logic, optimized per the proposed LE methods, allowed stretched litheness in optimizing various structures of DML networks. This optimization utilized the DML inherent properties of greatly reduced dependent capacitance and ultralow power dissipation in the static operation mode.

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