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Verification of Universal Memory Controller

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Abstract - *This paper describing verification of the Universal Memory Controller (UMC) which is compatible with WISHBONE verification IP .It involves creating a test bench for UMC as DUT. By generating a test cases the UMC features are verified and thus DUT is verified. For the verification of UMC three test cases are used .First test case involving SDRAM, second test case of SSRAM and last test case is of SYNC (synchronous chip select device).*

Key Words: **UMC, DUT, WISHBONE, SDRAM, SSRAM, SYNC**

1. INTRODUCTION

For SOC having different types of memories like SDRAM, DRAM, SSRAM, FLASH etc.., it will require different types of memory controllers for each memory types. Which will add extra space on SOC. Universal memory controller design, improved by integration of the existing memory controller in addition of providing novel features. This make the low power consumption for the design. UMC controller design which is supporting SDRM, SSRAM and SYNC memories what we call as Universal Memory Controller. This UMC design is having some specific function like, it has 8 chip select line and it support different types of memory. Single memory controller which is supporting different memories, for this UMC design, verification is done by generating a test cases in system Verilog language.

1.1 Universal Memory Controller

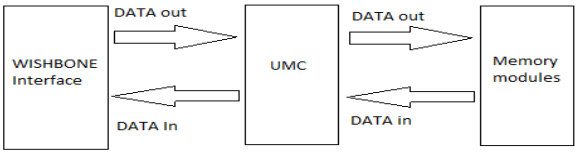

Fig -1: Over view of UMC

Diagram explaining the general module of UMC, which is having WISHBONE block, memory controller and memory module blocks which all are interfaced each other. Wish bone block is a place where we are verifying the UMC by checking read and write dada matching, if both read and write data matching then UMC is working properly and hence verification is done

The WISHBONE is a portable IP core .It is used in semiconductor IP for flexible design methodology WISHBONE is reusable, portable and reliable for the system.

Memory modules containing a different types of memory like SDRAM, SSRAM, and SYNC. These memories attached to the UMC through memory interface. All these memory designs are written in Verilog code, these Verilog codes are included in the top file of the system Verilog module. While verification system Verilog top modules are used.

UMC is having its own architecture design with novel feature supporting. UMC is placed between WISHBONE and memory module. These blocks are interfaced by WISHBONE interface and memory interface to the UMC.

1.2 verification of UMC

Verification of UMC is responsible for verification of UMC subsystem design, micro-architecture and golden models using advanced verification methodology. It executes test/coverage plans and correctness of the design is verified by working with architecture, designers. In verification for test bench, inputs are given to the design and outputs are monitored. Challenge in verification is to determine what to supply as input pattern to the design and what will be the expected output for properly working design under test.

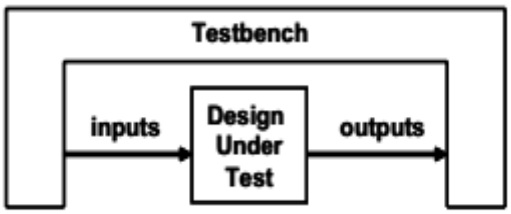

Fig -2:Testbench

2. Verification Environment for UMC

For verification of any design, verification environment has been created. Environment containing a generator (gen), bus function module (BFM), monitor, reference module, coverage, checker and scoreboard.

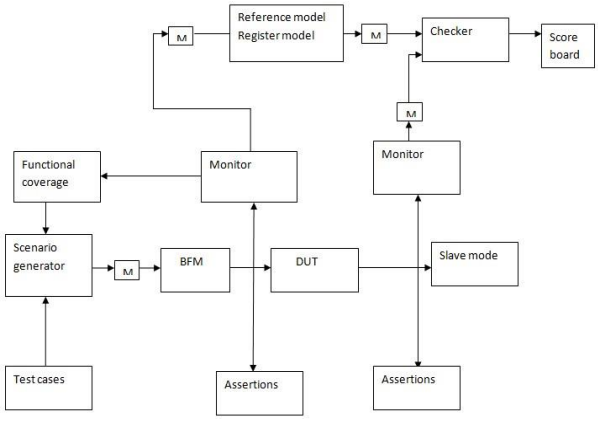

Fig -3:Testbench Environment

- Generator(gen):generator to generates the different test case seniors
- Bus Function Module (BFM): Bus Functional Module act as a block for connecting generator and Design under Test (DUT).It is called as driver also.
- Monitor: Monitor is used to monitor the transaction between the any two blocks.
- Reference module: It is the slandered module with which DUT values is compared.
- Coverage: It is numerical representation of DUT working.
- Checker: It collect the values from DUT and Reference module and make the comparison.
- Scoreboard: Scoreboard are built from classes and are used to perform checks between the DUT data and the expected data.

DUT is nothing but design under test which is UMC in this Verification. While creating environment first we start with the top module, after that we create a class of generator, bus functional module, monitor, checker, reference module, and interface. Mail boxes are used to put and get the data or address from one class to other classes.

2.1 SDRAM module

Synchronous Dynamic Random Access Memory. SDRAM are faster than Asynchronous DRAM. In SDRAM whenever there is change in input side causes changes in the output side only when clock changes. SDRAM memory is divided into four banks, so read and write operations happens faster than other memories.

Pin diagram of Memory Controller and SDRAM both blocks are interfaced by Memory interface shown in figure

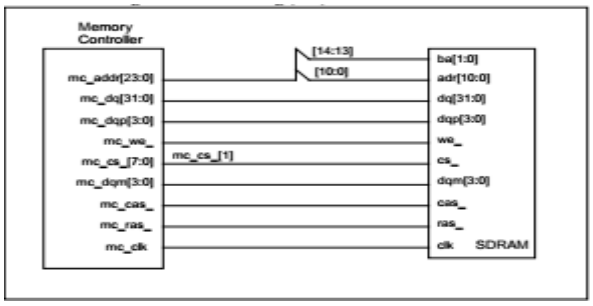

Fig -4: Interface of SDRAM with Memory Controller

The data from memory controller is written to the memory of SDRAM in one address location and from same address location data is read back to the Memory Controller.

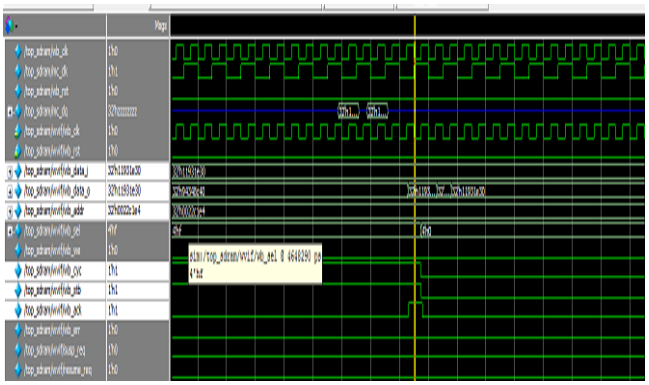

Fig -5: SDRAM Read and Write

Whenever acknowledgement, cyclic and strobe pins goes high read and write operation will happens. When WB pin goes zero read operation will happen, when WB pin goes high wright happens. As the memory is synchronous the out will changes after the clock changes even there is change in input.

2.2 SSRAM module

Synchronous static random access memory. SSRAM is volatile memory it not requires the refresh cycle to store the data. As it is synchronous memory, In SDRAM whenever there is change in input side causes changes in the output side only when clock changes, output depends on clock.

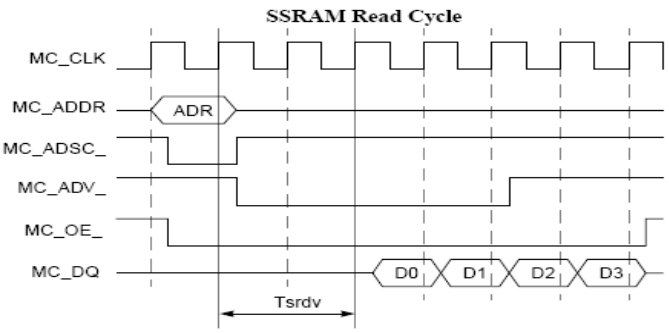

Fig -6: SSRAM Read cycle

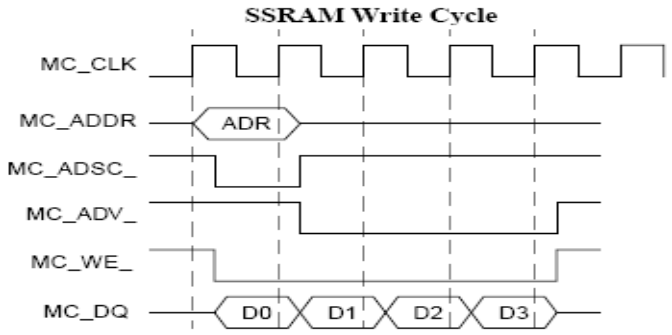

Fig -7: SSRAM Wright Cycle

This is the expected wave forms for read and wright operations. MC_WE goes wright operation will happens. And when MC_OE pin goes low read operations will happen.

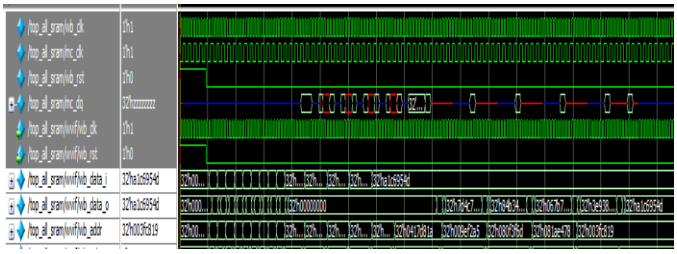

Fig -8: SSRAM Read and Wright

2.3 SYNC

- Synchronous chip select device, it also clock dependent. All SSRAM parameters in respect to the clock and are not configurable
- MC supports standard Sync Burst, Pipelined SSRAMs with double cycle deselect. Synchronous CS devices are synchronous to memory controller's clock.

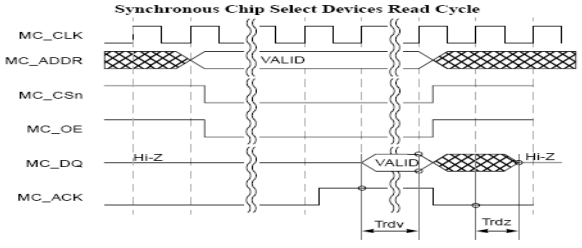

Fig -9: Synchronous Chip Select Device Read Cycle

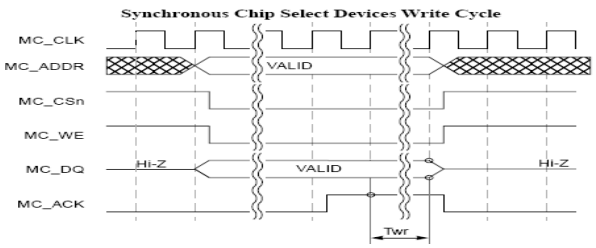

Fig -10: Synchronous Chip Select Device Write Cycle

This is the expected wave forms for read and wright operation. MC_WE goes wright operation will happens. And when MC_OE pin goes low read operations will happen.

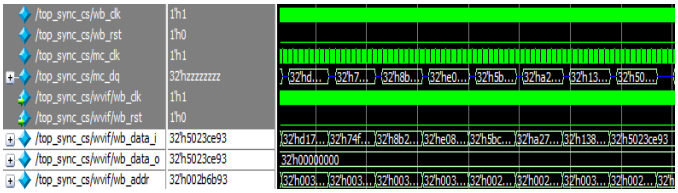

Fig -11: Synchronous Chip Select Device Read and Wright

3. CONCLUSIONS

Memory is the main part of any processer, there are different types of memory present on SOC. To controller the different types of memory instead of using different types of memory controller for each memory, only one memory controller is used called Universal Memory Controller. In this project, the verification is done for the Memory controller which is supporting different types of Synchronous memories, along with many feathers supporting compared to old Memory Controllers. Waveform showing the results of writing data to the Memory Controller and reading it back from memory through the WISHBONE is same. The data which is given the same data is reading back hence Universal Memory Controller is working.

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