Review Paper On

Implementation Of Low Power Hard Decision Viterbi Decoder In VLSI

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Abstract - *For correction of errors at the receiver end, convolutional encoding is used which is a forward error correction technique .Viterbi decoding is the best technique for decoding the convolutional codes but it is limited to smaller constraints length. This paper proposed implementation of low power hard decision viterbi decoder on Xilinx. The techniques used for decoding the data are traceback method and register exchange method.Register exchange method is not appropriate for decoders with long constraint lengths. Therefore in this paper traceback method is used for decoder with long constraint lengths.*

Key Words: Viterbi decoder, convolution encoder, low power, VLSI.

1. INTRODUCTION

There are many methods proposed in the error correction field. Viterbi algorithm is one of the best known method. Error correction method consists of three main parts: the convolutional encoding, the error disturbance, and the viterbi decoding. Firstly original data will be convoluted using its specific convolution formula which produce a codeword. Each codeword consists of 2-bits. The original data and its redundant bit represent a codeword. Therefore, if errors occur in the data transmission, we can still manage to reconstruct the correct data using viterbi algorithm.

1.1 PROPOSED WORK

The two techniques used for decoding the data are traceback method and register exchange method. Register exchange method uses dynamic register due to which power required is more. Therefore traceback method is used with butterful structure that consumes less power. Viterbi decoder decodes the convolutional codes. But during the transmission of data, error gets added in the original information. To remove this error from the transmission channel, Viterbi decoder is used.

2. CONVOLUTION ENCODER

Convolution coding with Viterbi decoding is a forward error correction technique that is particularly suited to a channel in which transmitted signal is corrupted mainly by noise [1].

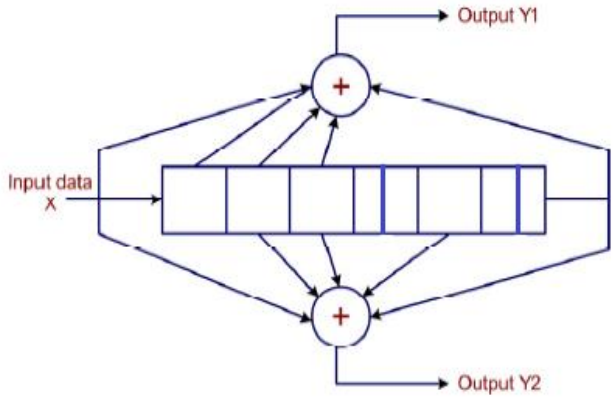

Figure 1: Convolutional encoder with constraint length k=9 and code rate (k/n)=1/2

In most of real time applications like audio and video applications, the convolutional codes are used for error correction [2]. Parameters for convolutional codes are the following: code rate (R), generating polynomial g (n), and number of input bits (k), number of output bits (n) and constraint length (K). The number of transmitted bits per input bit is known as code rate, e.g., a rate ½ encodes 1 bit and produces 2 bits for transmission.

2.1 WORKING OF CONVOLUTION ENCODER

The constraint length is the length of the generating polynomial in bits. Passing the information sequence to be transmitted through a linear finite shift register generates a convolutional code. The shift register consists of k bit stages and n linear algebric function generators. The contents of shift register are multiplied by respective term in generator matrix and are than added together to generate respective code words. By using a convolution operation, the information symbols are encoded. Symbols, which are defined by coefficients in the generator polynomial, are added modulo 2 to each other and form output signal [3].

Input u	Present State(S_1,S_0)	Next State(S_1,S_0)	Output (V_1,V_2)
0	00	00	00
1	00	01	11
0	01	10	11
1	01	11	00
0	10	00	10
1	10	01	01
0	11	10	01
1	11	11	10

Figure 2: Stable state

State table, state diagram and trellis diagram can be represented by convolutional encoder. The contents of the shift register of the encoder defines the state. The output symbol can be described as a function of input symbol and the state, in state table. The transition between different states is shown in state diagram. Description of state diagram of the encoder by a time line that is to represent each time unit with a separate state diagram is known as trellis diagram.

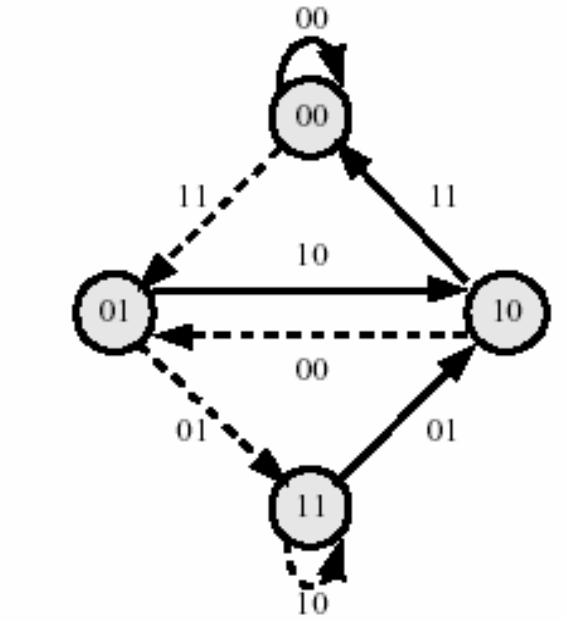

Figure 3: State Diagram

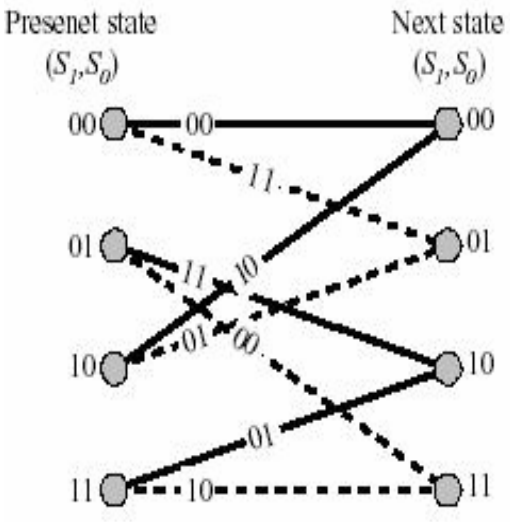

Figure 4: Trellis Diagram

3. VITERBI DECODER

The basic building blocks of Viterbi decoder are branch metric unit (BMU), path metric unit (PMU), add compare and select unit (ACSU) and survivor memory management unit (SMU).

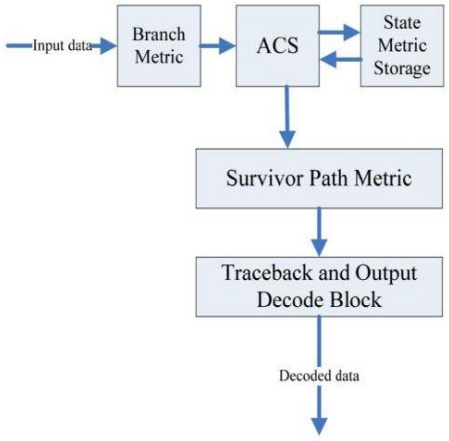

Figure 5: Block diagram of Viterbi decoder

3.1 WORKING OF VITERBI DECODER

3.1.1 BRANCH METRIC UNIT (BMU)

The first unit is called branch metric unit. The received data symbols are compared with the ideal outputs of the encoder from the transmitter and thus branch metric is calculated. Branch metric computation uses hamming distance or Euclidean distance.

3.1.2 PATH METRIC UNIT

Path metric computation unit is the second unit which calculates the path metrics of a stage by adding the branch metrics, associated with a received symbol, to the path metrics from the previous stage of the trellis.

3.1.3 ADD COMPARE AND SELECT UNIT (ACSU)

The ACSU unit is composed of 64 ACS units, each is composed of an ACS butterfly module, which adds the corresponding BM to corresponding PM, compares the new PM, feeds the selected PM to ACSU unit and generates the decision bits. The decoder implements adders for computing the path metric and a compare-select section to decide on the best path. Using bit serial architecture can reduce the power of Viterbi decoder.

4. VITERBI ALGORITHM

In 1971, Viterbi algorithm was introduced by Viterbi. Since it minimizes the probability of error Viterbi algorithm is called as optimum algorithm. Optimum decoding technique is the Viterbi decoder. It is optimum as it results in the minimum probability of error. It is also the relatively straight algorithm to implement in hardware and is the best decoding technique. Viterbi algorithm is a maximum likelihood algorithm and performs decoding, through searching the minimum cost path in a weighted oriented graph, called trellis [4].

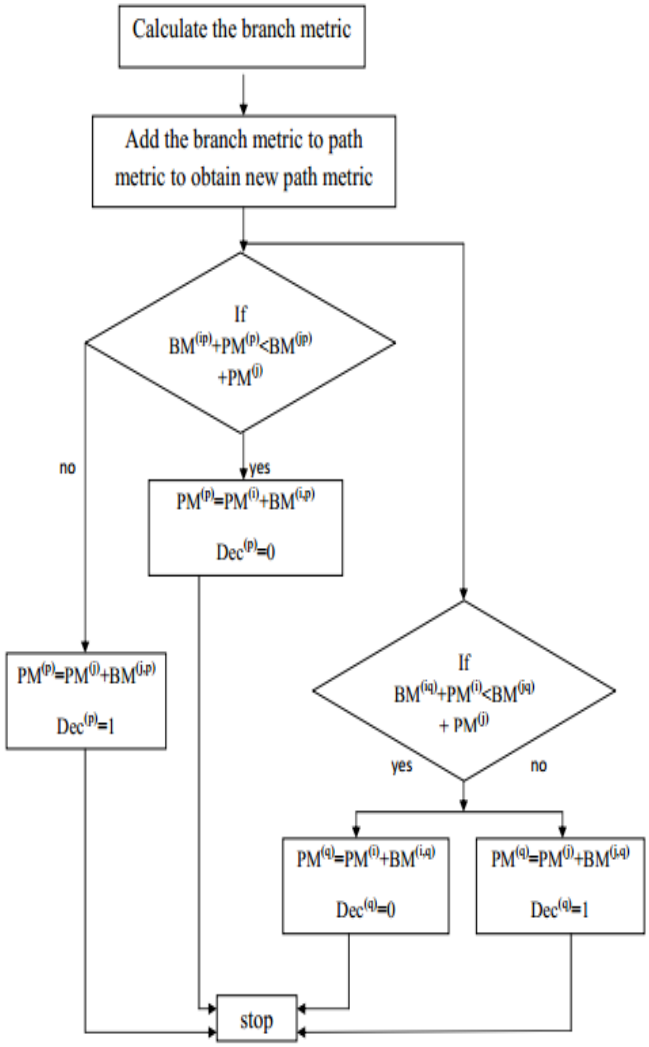

Figure 6: Flowchart for viterbi algorithm

4.1 WORKING OF VITERBI ALGORITHM

The algorithm can be categorized into following three steps.

1. Calculate the branch metrics; that is weigh the trellis.
2. Now the shortest paths to time n is computed, in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. Therefore it is called as add-compare-select (ACS) recursion.

3. Relatively find the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the p1rocess is referred to as survivor path decode. At last, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path [6].

5. REFERENCES

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