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# Implementation of an Efficient Multiplier based on Vedic Mathematics

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**Abstract -** *A High speed processor depends mostly on the multiplier as it one of the key hardware blocks in most digital processing system. This paper depicts and proposes the design of 8*8 bit binary arithmetic multiplier by using Vedic Mathematics .Vedic mathematics is the name given to the ancient system of mathematics which is rediscovered from the Vedas. It is based on Vertical and Crosswise structure of ancient Indian Vedic Mathematics. The Vedic Mathematics also known as Urdhva Tiryagbhyam Sutra is for generating the partial product. The partial product addition in Vedic Multiplier is realized using carry-skip technique. The propound architecture is for two 4 bit numbers, the multiplier and the multiplicand which are grouped as 4 bit number, so that it decomposes 4*4 multiplication modules. This algorithms are executed in VHDL language by using Modelsim and synthesis is done in ISE Project Navigator Xilinx Software.*

***Key Words*: Vedic Mathematics, Urdhva Tiryagbhyam, Modelsim, ISE Project Navigator Xilinx Software, VHDL.**

## 1. INTRODUCTION

With the encroachment of VLSI technology the use for portable and DSP systems has increased efficiently . Multipliers are key components of many high performance systems such as Microprocessors ,Digital signal processors etc. The speed of the Multipliers mainly depends on the number of partial products. And also the speed of adder which are used in it. After eight years of research on 'Vedas', Shri Bharti Krishna Tirthaji reconstructed the Vedic Maths. According to him, Vedic Mathematics is mainly focused on sixteen very important principles or formulae which is termed as Sutras. The variety of applications of vedic mathematics includes Compound Multiplications, Algebraic Operations, Squaring, Cubing, Cuberoot, Quadratic Equation and Co-ordinate Geometry.

In this paper after the introduction of Urdhava Tiryakbhyam Sutra, Multiplier architecture is discussed and is illustrated with two 4 bit numbers. The multiplier and the multiplicand each are proposed as 4 bit numbers so that it decomposes into 4*4 multiplication module. After decomposition, vertical crosswise is applied to carry out the multiplication on first 4*4 multiplication module. Vedic Sutras are applied to binary multipliers using carry save address. The Vedic Multiplier which is discussed in the paper performs partial product Multiplication and addition in parallel which gives a better performance in terms of area and speed.

## 2. URDHVA TIRYAKBHYAM SUTRA

In Urdhva Tiryakbhyam Sutra, Operations are performed in invertical and crosswise manner. Multiplication operation is done by simple addition of partial products. In this Sutra the parallelism architecture is used which means generation of partial products and their summing is performed simultaneously.

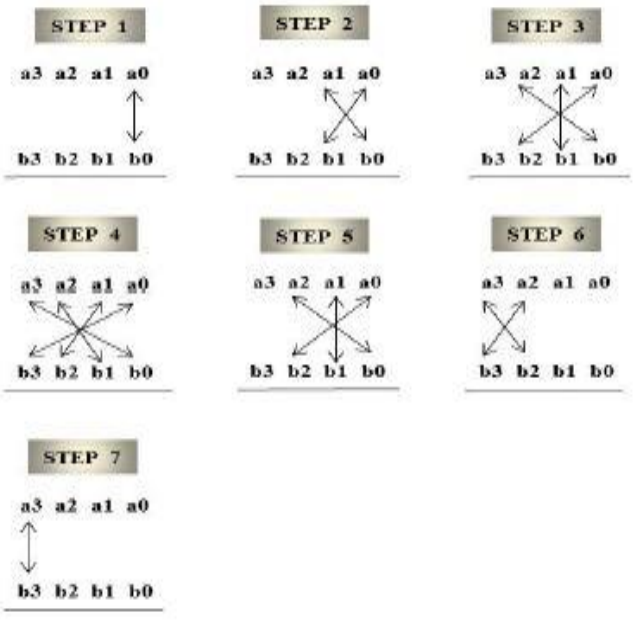


**Fig.1:** Multiplication of two decimal numbers by Urdhva

As a result, processor speed increases. Calculations of Urdhva Tiryakbhyam Sutra is shown in figure. Multiplication of two numbers 325x738 is performed by vertical and crosswise manner ,the result obtained by this multiplication is added with the carry generated from every pervious step and the procedure is continued till last bit of the input.

## 3. VEDIC ALGORITHM

Vedic Multiplier is based on Vedic Mathematics. Vedic Mathematics is an ancient way of Calculation. It was rediscovered from Vedas in between 1911 to 1918 by Sri Bharti Krishna Tirthaji (1884-1960), who was mathematician and Sanskrit scholar. The Vedic mathematics is based on the sixteen Sutras of Urdhva Tiryagbhyam. It simply means "Vertical and Crosswise Multiplication". The Speciality of it is minimizied number of calculations, reduced space, saving computational time and it is applicable in all cases of multiplication. This method is most efficient when the number of bits in Calculation Increases. The structure of this method is shown in the figure. This Figure gives us clear idea of "vertical and crosswise multiplication".

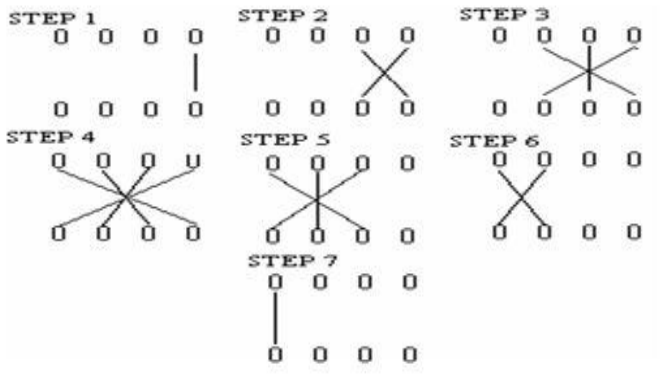


**Fig 2 :** Vedic Algorithm

In multiplication of two 4 bit numbers the process is divided into 7 steps. The first number is a3a2a1a0 which is multiplier and second number is b3b2b1b0 which is multiplicand as shown in the step1 of the figure. The LSB ( least significant bit ) of multiplier is multiplied with LSB of the multiplicand and the result of this multiplication is stored as the LSB of the final result. Then as shown in the step2 of the above figure the LSB of multiplier is multiplied with second higher bit of multiplicand and second higher bit of multiplier is multiplied with LSB of multiplicand and then these two partial products are added. After adding these two numbers the LSB of addition is taken as the second higher bit of the final result and remaining bits of the addition are taken as carry bit. This carry formed can be of Multi bit. Then follow the steps which are given in the above figure and this gives us the result of the 4 bit multiplication.

## 4. THE PROPOSED MULTIPLIER ARCHITECTURE

This method can be used for any N x N bit multiplication. This Vedic multiplier is independent of clock frequency because partial product and their sum are calculated in parallel. And also because of this it does not require high clock frequencies for multiplication and this is the reason, less switching takes place. Because of less switching delay and Minimized Power the result of we get is more efficient in terms of delay and power. In this paper we are presenting 4 bit multiplication and for that we require 2 bit vedic multiplier, 4 bit adder and also 6 bit adder. The detailed explanation of these architectures is given below.

### 4.1 Vedic Multiplier for 2X2 Bit Module

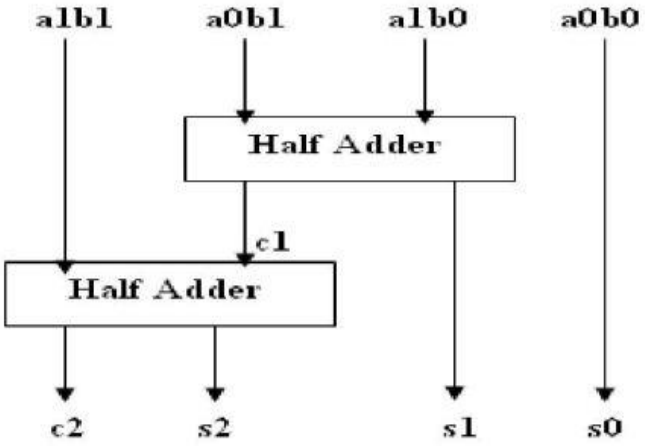


**Fig 3:** Vedic multiplier for 2X2 bit

A basic block diagram of 2x2 multiplier is as shown in figure. In this diagram a0, a1 are the bits of first digit and b0, b1 are the bits of second digit. In this multiplier we are taking AND of respective bits and then further the steps are followed as shown in Block Diagram. The multiplication is done on the Sutra of Urdhva-Tiryagbhyam. The result obtained is of 4 bits.

### 4.2 Vedic Multiplier for 4X4 Bit Module

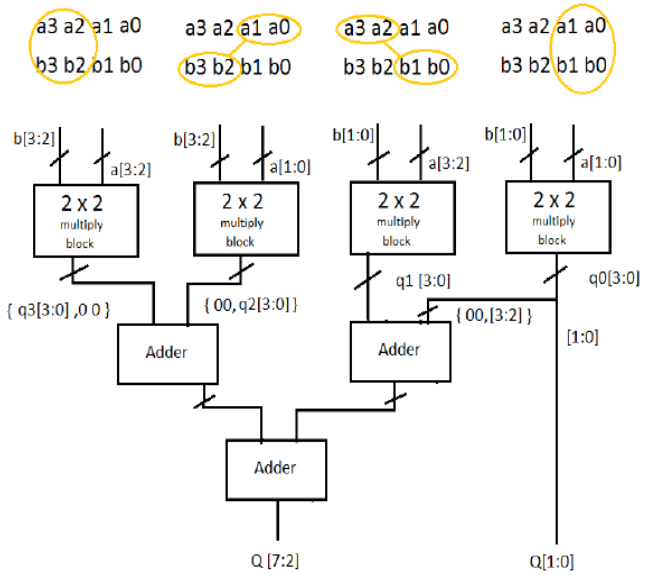


**Fig 4:** Vedic multiplier for 4X4 bit

After the implementation of basic 2x2 multiplier it is easy to implement 4X4 multiplier. In the diagram a0, a1, a2, a3 are the bits of first digit while b0, b1, b2, b3 are the bits of second digit. For 4x4 bit multiplication we require four 2x2 multiplier, three adders. After doing the procedure as shown in figure we can implement the 4x4 Vedic multiplier. The result obtained is of 8 bits.

### 5. IMPLEMENTATION ON XILINX SOFTWARE

Now we are moving to main programming part of the proposed Multiplier. Using the Vedic Multiplier we will develop a program. In this work the 4 bit multiplier is designed in VHDL(very high speed integrated circuits hardware description language), Synthesis and Simulation was done in XILINX ISE 10.1.6 ISE Project Navigator and simulator navigated in the XILINX package. XILINX is software which is based on VHDL language. We have performed our programming using the Spartan-3E family, Device is XC3S1600E and Package is selected as FG3200 and speed grade is -4. Integrated Software Environment is a Software tool produced by XILINX for synthesis and analysis of HDL design, enabling the developer to synthesize their design, examine RTL diagrams, perform time analysis ,simulate a design reaction to different stimuli and configure the target device with the programmer. It includes ISE simulator which we can use for simulation and functionality verification of program.

### 6. RESULTS

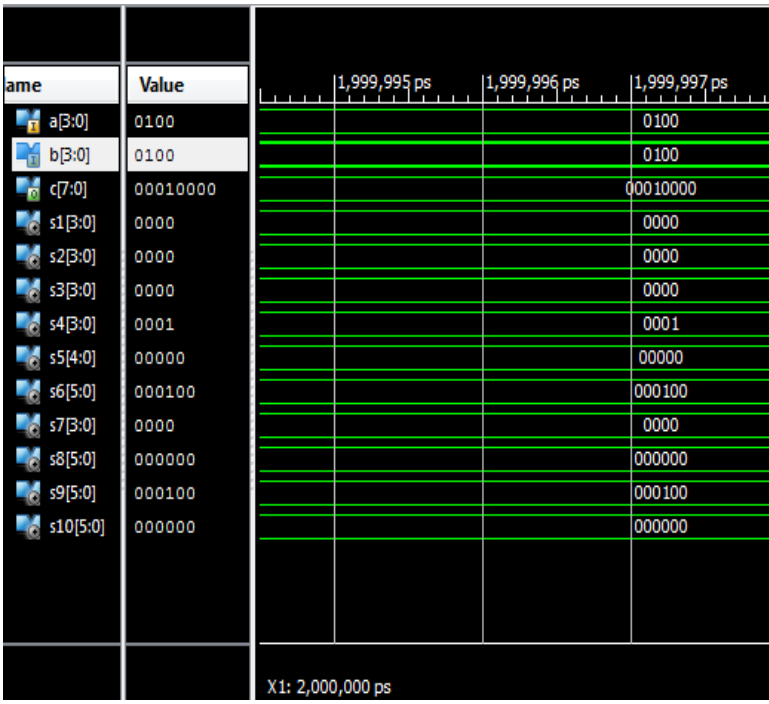


**Fig 5: Vedic Multiplier 4 bit**

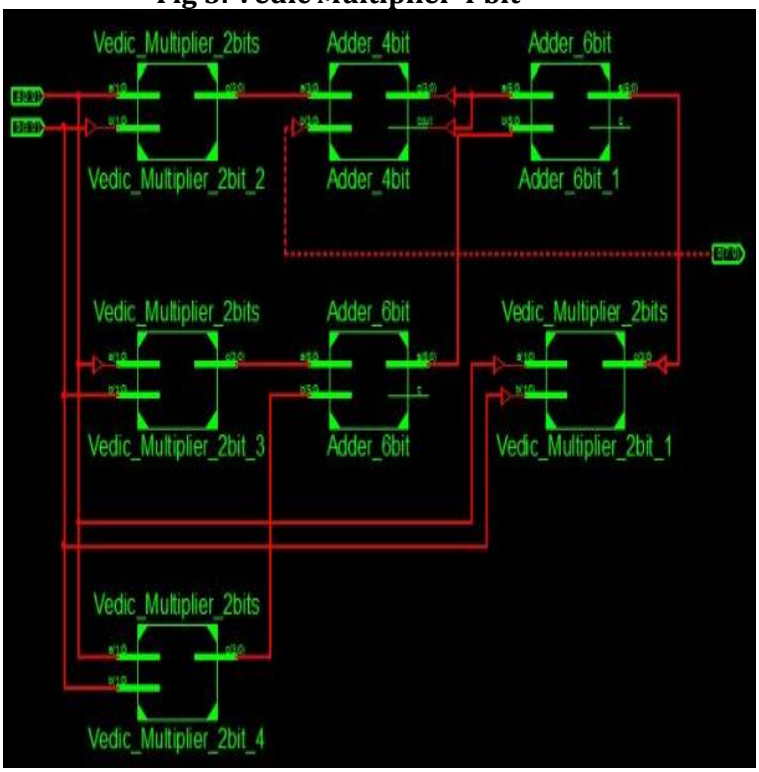


**Fig 5: RTL Schematic of 4 Bit VEDIC Multiplier**

## 7. CONCLUSIONS

This paper presents an unique method of Multiplication based on Vedic Mathematics. Generally the Vedic Multiplier based on Vedic Mathematics are much faster than the Conventional Multipliers. This gives us scheme hierarchical multiplier and clearly indicates the computational advantages offered by Vedic Methods such as it gets condensed for inputs of large number of bits and modularity gets augmented. The computational path delay is found to be lesser as compared to the Conventional Multiplier, which was our Motto. Vedic Multiplier has less number of gates required for given 8*8 multiplier so its power dissipation is very small when compared to the other Multiplier architecture. In terms of area, the proposed Multiplier is far better than the Conventional Multiplier.

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