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Three Phase Hybridised Seven-Level Inverter Fed BLDC Motor

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ABSTRACT:-

Multilevel inverters are much superior to conventional two level inverters for their improved performance. This paper presents a novel three phase seven level inverter to reduce harmonic content in output voltage and load current. Operation principle and switching scheme oh proposed inverter are analysied in details. Level shifted multi carrier pulse width modulation (LS-PWM) is used as the switching scheme for the proposed inverter. By proper controlling of modulation index, it is possible to achieve 7,5 and 3 level inverter operation. To assess the proposed inverter topology, comparison with other classical three phase seven level topologies are done based on count of power circuit components. The validity of proposed inverter is verified through simulation for RL-load.

INDEX TERMS—Multilevel inverter, LS-PWM, modulation index

INTRODUTION

Recently multilevel inverters are getting wide acceptance because of its features such as high quality voltage with low distortion , reduced dv/dt stress and reduced electromagnetic interference. The concept of multilevel inverter is to achieve higher power conversion with series of power semi conductor switches connected to low voltage dc sources, such that the switching produces high quality staircase voltage wave form quality of power increases with higher voltage levels, but it may result in increased number of power electronic switches which in effect increase cost, control complexity and reduces overall efficiency.

Plenty of multilevel inverter topologies and unique modulation schemes were introduced in recent researches. major three multilevel structures that have been reported in literature are neutral point lamped (NPC) inverter, flying capacitor inverter (FC), cascade H-BRIDGE INVERTER(CHB). Major drawbacks of dc link capacitors and increased number of clamping diodes with higher number of voltage levels. FC inverter uses flying capacitor as clamping device. Phase redundancies present in FC inverter avoids capacitor voltage balancing issues. FC inverter system becomes more bulky and expensive as number of levels increase. CHB inverter topology provided a good and efficient solution for high power applications. However, it requires more isolated dc sources and increased number of switches.

With the introduction of new multilevel topologies, modulation techniques also started developing. Modulation schemes were reported in literature and with features like reduced THD, easy implementation and less computation time. Space vector modulation(SVM) and multi carrier sinusoidal pulse width modulation have got greater attention as the modulation scheme for multilevel inverters.

In this paper, a novel hydrid three phase seven level inverter is proposed. Inverter uses reduced number of switches compared to other symmetrical seven level topologies.

Proposed seven level topology

The proposed active filter topology is shown in Fig. It consists of an H-bridge configuration made from three-level flying capacitor branches. Essentially, it is a voltage-source inverter (VSI) with capacitive energy storage (Cdc) shared by all three phases. Total of eight switching devices are used in each phase. A tapped reactor is used to connect the two legs of the Hbridge. Typically, the reactor is wound to be center tapped, making the output line-to-ground voltages (vag for example) the average of the voltages from each side of the H-bridge. Then, the line-to-ground voltages will have five distinct voltage levels. However, with this topology, the tap is set at 1/3. This results in seven distinct output voltages, and therefore, improves the power quality. The switching operation is described next, wherein all seven levels are clearly illustrated.

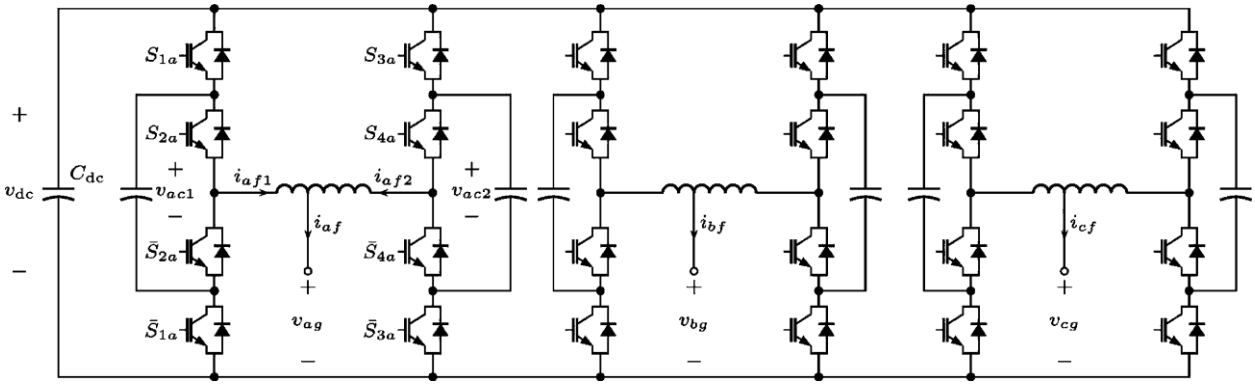


Fig. Proposed seven-level inverter topology

TABLE I :-ACTIVE FILTER LINE-TO-GROUND VOLTAGES

s_a	v_{a1}	v_{a2}	v_{ag}
0	0	0	0
1	0	$v_{dc}/2$	$v_{dc}/6$
2	$v_{dc}/2$	0	$v_{dc}/3$
2'	0	v_{dc}	$v_{dc}/3$
3	$v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$
4	$v_{dc}/2$	v_{dc}	$2v_{dc}/3$
4'	v_{dc}	0	$2v_{dc}/3$
5	v_{dc}	$v_{dc}/2$	$5v_{dc}/6$
6	v_{dc}	v_{dc}	v_{dc}

The core of the reactor is highly permeable in a sense that it requires vanishingly small magneto motive force to set up the flux. The core does not exhibit any eddy current or hysteresis loss. All the flux is confined in the core, so there is no leakage flux. The resistance of the reactor is negligible.

Suppose that voltages vx1 and vx2, with respect to a common ground, are applied to the input terminals x1 and x2, respectively. For this ideal model, it is straightforward to determine the voltage between the output terminal x and terminal x2

$$v_{xx2} = \left(\frac{N_2}{N_1 + N_2}\right)(v_{x1} - v_{x2}) = \frac{2}{3}(v_{x1} - v_{x2}).$$

The voltage at the output terminal with respect to the common ground is therefore

$$v_{xg} = v_{xx2} + v_{x2} = \frac{2}{3}v_{x1} + \frac{1}{3}v_{x2}.$$

In the general analysis presented earlier, x represents a phase, and the phase may be a, b, or c. Each leg of the H-bridge has a voltage-clamping capacitor, and the voltages at the two input terminals of the reactor can be 0, vdc/2, or vdc, where vdc is the nominal voltage of the capacitor Cdc, as shown in Fig.

For each phase, there are nine different switching states, corresponding to nine terminal voltage combinations. These combinations can produce a line-to-ground voltage at the output terminal that has seven distinct voltage levels. For phase a, these states are detailed in Table I.

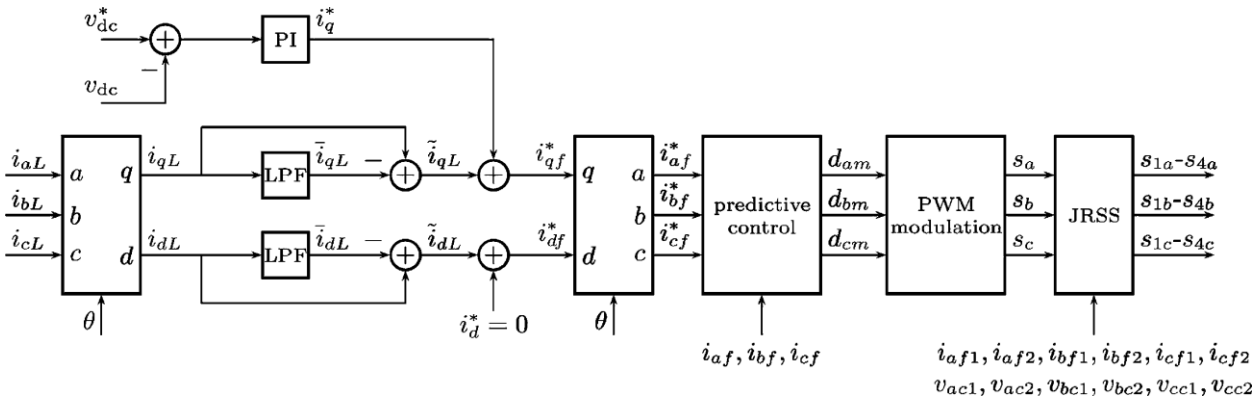


Fig. seven level control diagram.

PWM MODULATION

High quality seven level output voltage can be obtained by adopting proper modulated scheme. Level shifted multicarrier PWM scheme is employed as the switching strategy for the proposed seven level inverter.

In this paper, a predictive current regulator is implemented to track the harmonic currents, which has the advantages of simple structure and less computational requirement. Given the measured system voltages and filter inductor currents, the required phase a filter voltage can be calculated based on the known value of the filter inductance

$$v_{af}^{*} = \hat{v}_{as} + \frac{(\hat{i}_{af}^{*} - i_{af})L_f}{\Delta t}$$

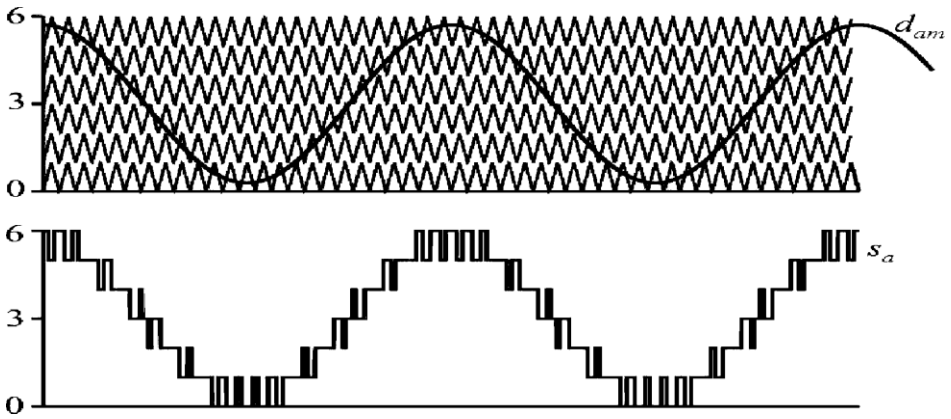


Fig. Seven-level voltage-source modulation.

Where Δt is the controller switching period, ˆvas is the predicted source voltage and can be calculated through linear extrapolation

$$\hat{v}_{as} = v_{as}(t) + 1.5\Delta t\ [v_{as}(t) - v_{as}(t - \Delta t)]$$

BLDC MOTOR

Brushless Direct Current (BLDC) motors are one of the motor types rapidly gaining popularity. BLDC motors are used in industries such as Appliances, Automotive, Aerospace, Consumer, Medical, Industrial Automation Equipment and Instrumentation.

As the name implies, BLDC motors do not use brushes for commutation; instead, they are electronically commutated. BLDC motors have many advantages over brushed DC motors and

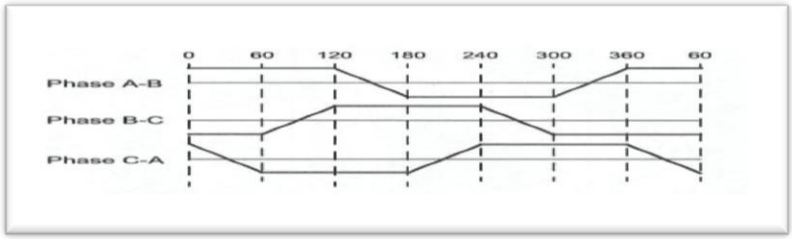


Figure 2.1 Trapezoidal Back EMF

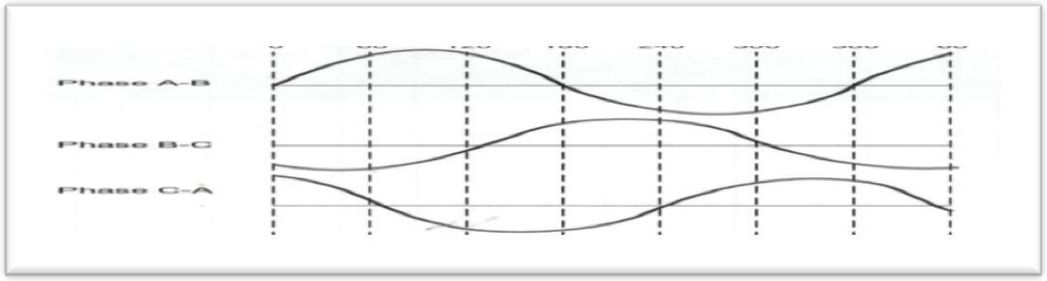


Figure 2.2 Sinusoidal Back EMF

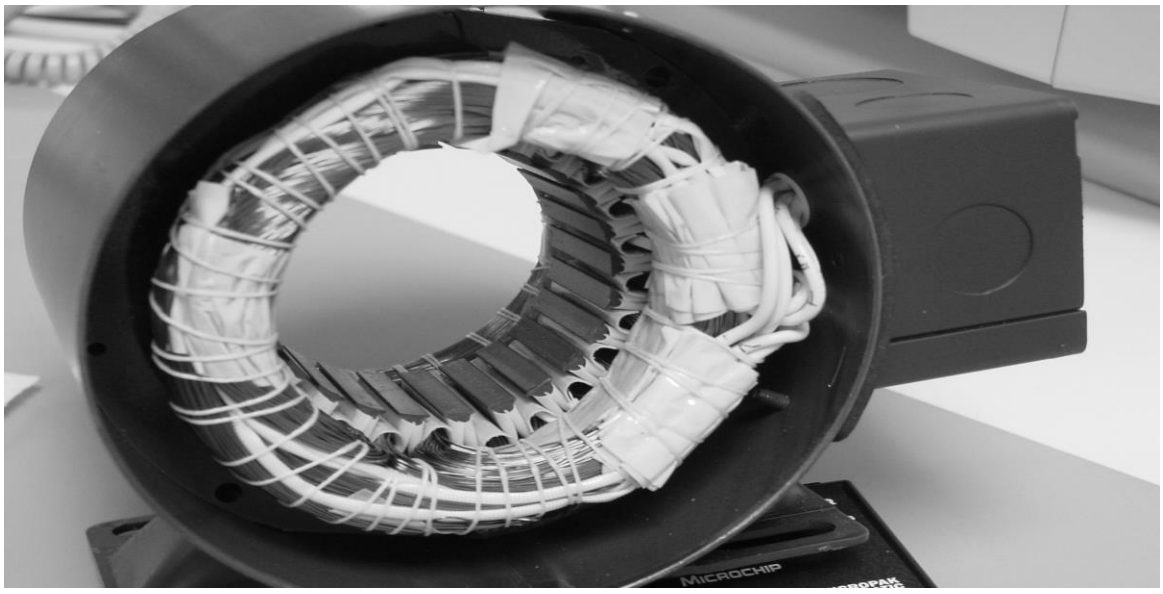


Figure 2.3 Stator of a BLDC motor

Stator

The stator of a BLDC motor consists of stacked steel laminations with windings placed in the slots that are axially cut along the inner periphery (as shown in Figure 2.3). Traditionally, the stator resembles that of an induction motor; however,

the windings are distributed in a different manner. Most BLDC motors have three stator windings connected in star fashion. Each of these windings is constructed with numerous coils interconnected to form a winding. One or more coils are placed in the slots and they are interconnected to make

a winding. Each of these windings is distributed over the stator periphery to form an even numbers of poles.

Rotor

The rotor is made of permanent magnet and can vary from two to eight pole pairs with alternate North (N) and South (S) poles. Based on the required magnetic field density in the rotor, the proper magnetic material is chosen to make the rotor. Ferrite magnets are traditionally used to make permanent magnets. As the technology advances, rare earth alloy magnets are gaining popularity. The ferrite magnets are less expensive but they have the disadvantage of low flux density for a given volume. In contrast, the alloy material has high magnetic density per volume and enables the rotor to compress further for the same torque. Also, these alloy magnets improve the size-to-weight ratio and give higher torque for the same size motor using ferrite magnets

HARMONIC DISTORTION

Harmonic problems are almost always introduced by the consumers' equipment and installation practices. Harmonic distortion is caused by the high use of non-linear load equipment such as computer power supplies, electronic ballasts, compact fluorescent lamps and variable speed drives etc, which create high current flow with harmonic frequency components. The limiting rating for most electrical circuit elements is determined by the amount of heat that can be dissipated to avoid overheating of bus bars, circuit breakers, neutral conductors, transformer windings or generator alternators.

Certain types of loads also generate typical harmonic spectrum signatures that can point the investigator towards the source. This is related to the number of pulses, or paths of conduction.The general equation is h = (n * p) +/- 1, where h is the harmonic number, n is integer (1,2,3,..) and p is the number of pulses in the circuit, and the magnitude decreases as the ration of 1/h (1/3, 1/5, 1/7, 1/9,...). Table 4 shows examples of such.

Type of device	Number of pulses	Harmonics present
half wave rectifier	1	2,3,4,5,6,7....
full wave rectifier	2	3,5,7,9,...
three phase, full wave	6	5,7, 11,13, 17,19,...
(2) three phase, full wave	12	11,13, 23,25, 35,37,...

Table. Typical Harmonics Found for Different Converters.

monic limits for current depend on the ratio of Short Circuit Current (SCC) at PCC (or how stiff it is) to average Load Current of maximum demand over 1 year, as illustrated in Table 5. Note how the limit decreases at the higher harmonic values, and increases with larger ratios.

RATIO Iscc / I load	Harmonic Range	Limit as % of Fundamental
Less than 20	Odd numbers less than 11	4.0 %
Between 20 and 50	Odd numbers less than 11	7.0 %
Greater than 1000	Odd numbers greater than 35	1.4%

Table5. Current Harmonic Limits as per IEEE 519-1992

For voltage harmonics, the voltage level of the system is used to determine the limits, as shown in Table 6. At the higher voltages, more customers will be effective, hence, the lower lim

Figure8. Power Quality Monitor with Harmonic Analysis

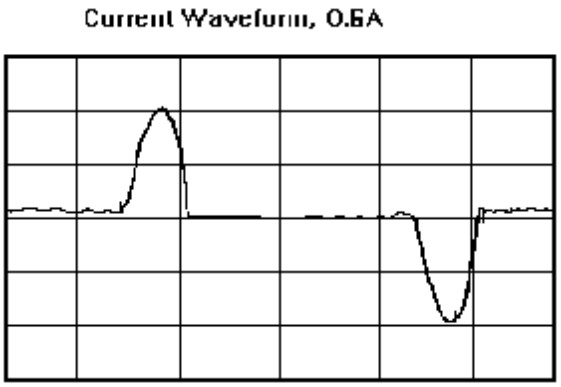


Figure5. Current Waveform

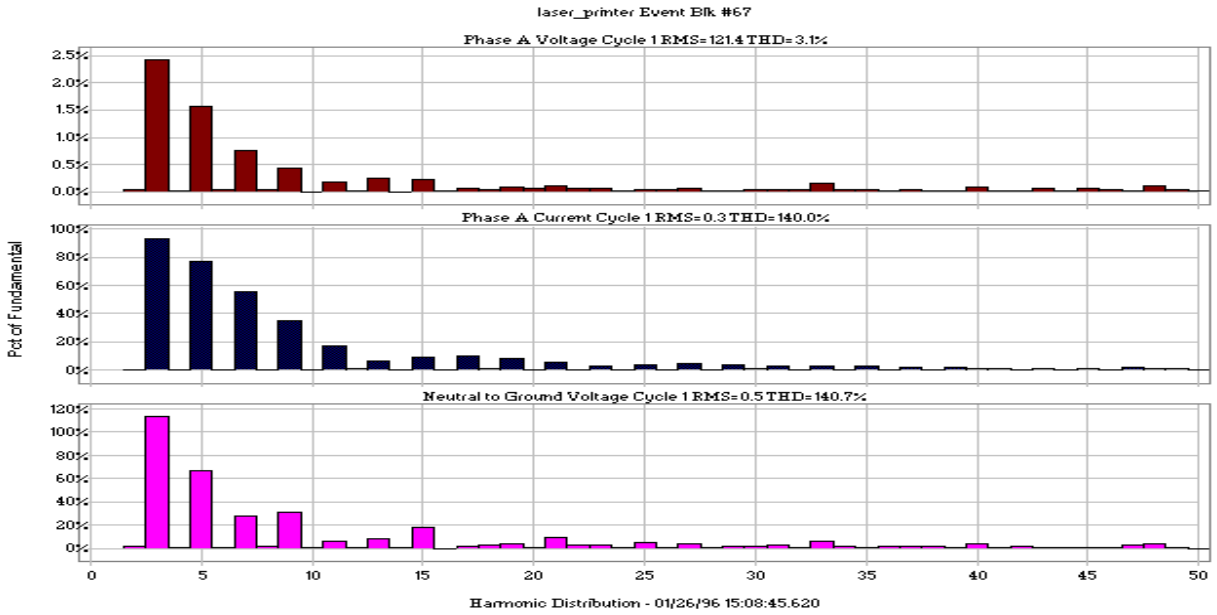


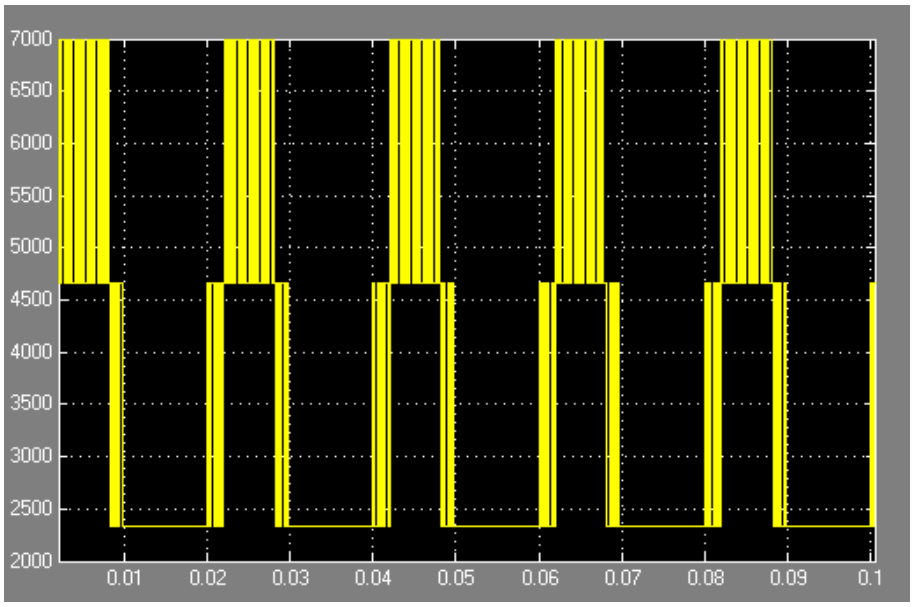
Figure6. Harmonic Spectrum of Current Waveform Shown in Figure 5

If the rectifier had only been a half wave rectifier, the waveform would only have every other current pulse, and the harmonic distortion.

SIMULATION RESULTS

Validity of proposed seven level inverter is verified in MATLAB/SIMULINK. LS-PWM is carried out by comparing three carrier signals of frequency 2KHZ with rectified sinusoidal signal of fundamental frequency 50HZ. Switching signals are generated by using logical expressions as mentioned in section. Performance of proposed inverter in 7, 5 and 5 level operations are analysied in details. DC bus voltages of 70v and 140v are selected.

PWM Modulation , gate signals are generated, output voltage and load current for modulation index of 0.9 is shown in fig. output voltage and load current for Ma=0.6 and 0.3. phase shift between inverter output voltage and load current is due to the inductive nature of d load. THD in load curret are found to be 2.25% and 5.96% for modulation index of 0.9, 0.6 and 0.3 respectivelly.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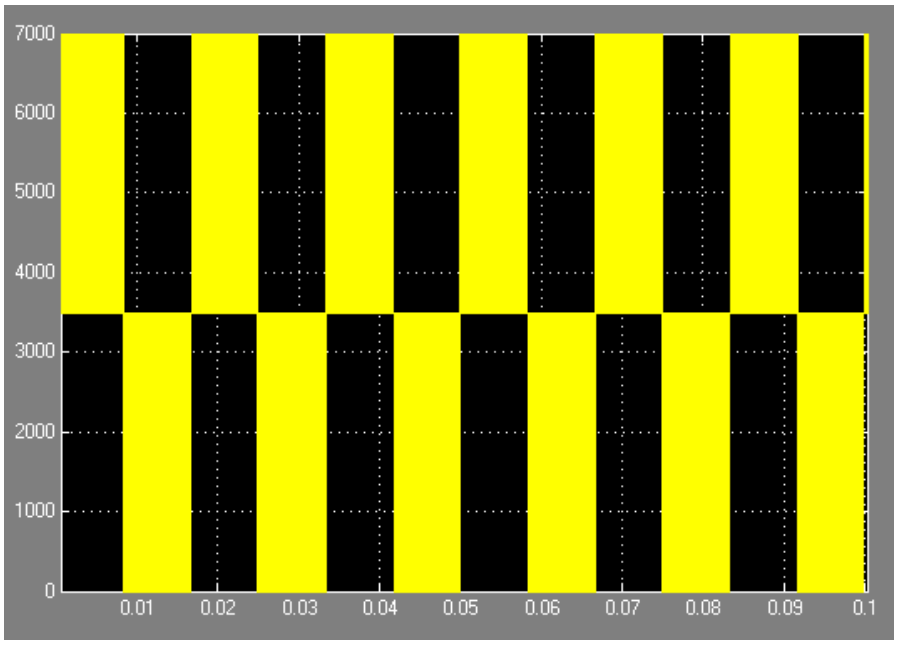
Va1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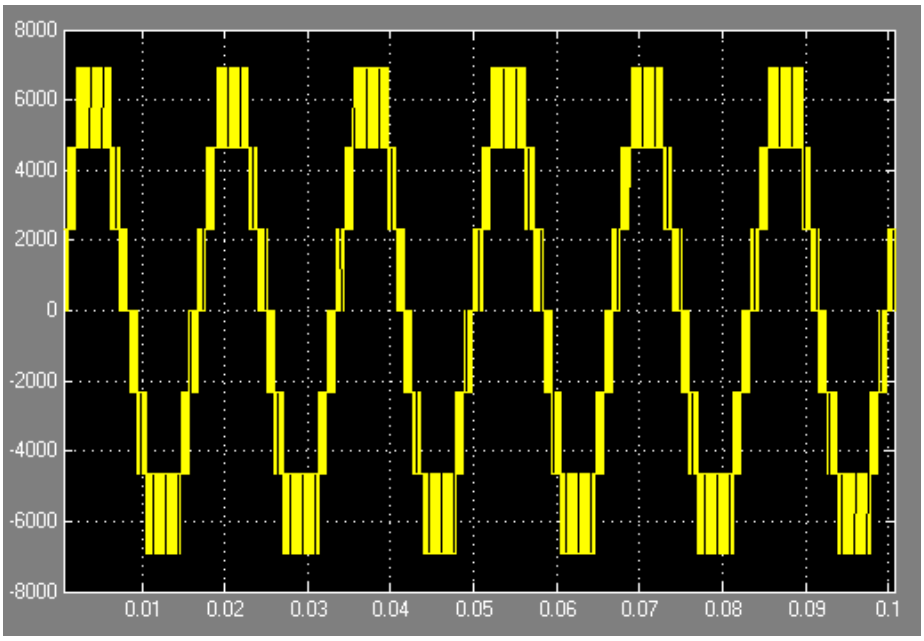
Va2



Vh

Conclusion

A novel three phase seven level inverter topology has been proposed. Proposed inverter is able to provide output voltage of good quality with reduced harmonic content. Inverter requires less number of components Which is turn reduces cost and power losses. LS-PWM technique is used as the modulation scheme for generating switching signals. It logical expressions for generating gate signals from PWM are derived.

Proposed inverter is able to produce output voltage of three , five, seven level respectively by controlling modulation index.

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