IMPLEMENTATION OF SRAM USING DOUBLE SLEEP WITH DTCOMS

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Abstract - *Speed, power consumption and area, is some of the most important factors of concern in modern day memory design. Most microprocessor use large on-chip SRAM caches to bridge performance gap between the processor and the main memory. Due to their growing embedded applications coupled with the technology scaling challenges, considerable attention is given to the design of low power and high performance SRAMs.In this paper, we proposed 4T SRAM cell using double sleep with dual threshold voltage transistors. Low threshold voltage transistors are mainly used in deriving bit lines while high threshold voltage transistors are used in latching data voltages. The advantages of dual threshold voltage transistors can be reduce the access time and maintain data reduction at the same time.*

Key Words: Dual threshold CMOS (DTCMOS), Static random access memory (SRAM), Double sleep, leakage current.

1. INTRODUCTION

Semiconductor memories are most important subsystem of modern digital systems. In new era the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. But due to the high density, power dissipation gets increases and speed decreases. So there is need for design of low power and high speed circuit in memory. A memory in terms of Computer hardware is a storage unit. There are different types hardware used for storage, such as magnetic hard drives and tapes, optical discs such as CDs and DVDs, and the electronic memory in form of integrated memory or stand-alone chips.

The main focus of this paper is the SRAM. There are some very important requirements for a memory when it is to be embedded as on-chip cache. First and foremost it has to be reliable and stable. This is of course true for all memories, but is especially important for cache due to the more extreme Performance requirements and area limitations. Secondly the memory has to have high performance. The sole purpose of cache is to speed up the operation of the CPU by bridging over the performance gap between main memory and the CPU. Another most important requirement is low power consumption. With increasing memory sizes these contribute with more and more power loss.

2. SRAM

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors that forms two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations.

In addition to such six transistor (6T) SRAM, other kind of SRAM chips use 4,8,10 (4T, 8T, 10T SRAM), or more transistors per bit. Four transistor SRAM is quite common in standalone SRAM devices (opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high resistance pull up resistor. The principle drawback of 4T SRAM is increased static power due to the constant current flow through one of the pull down transistors.

1.1 4T SARM cell using RSL

4T SRAM contains 4 transistors, a pair of pmos and nmos makes twisted inverter and two nmos as access transistor in inverter nmos works as driver transistor and pmos works as load transistor. Unlike 6T cell it requires 4 mos a pair of nmos and pmos forms cross coupled inverter and 2 nmos for access transistor used to access cell to transfer data during read and write cycle. The load devices used in this design are made of polysilicon resistors or it can be depletion type NMOS or PMOS. The enhancement types of nmos are used as the pass gates which act as the data access switches. The use of resistive load inverters with un doped poly silicon resistance in the latch structure results in a significantly more compact cell size as compared to the other SRAM design. The value of the resistance used in this design should be low such that it can attain acceptable noise margin for the resistive load inverter. On the other hand, a high value of load resistance is reduce the amount of standby current being driven by the memory cell.

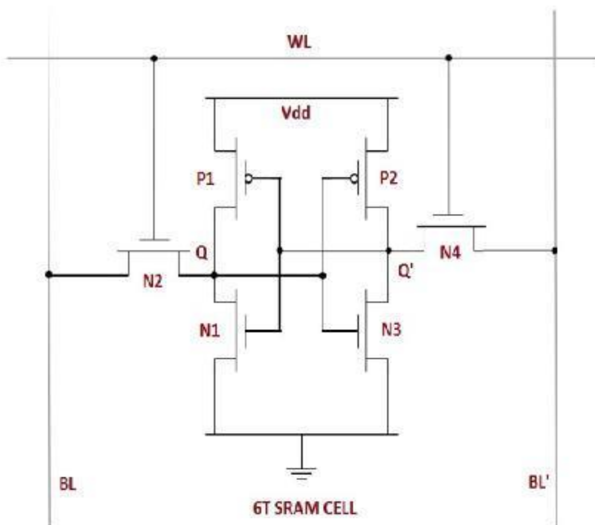

Fig 1. 6T SRAM cell

1.2 Standby mode

In this mode the word line is not asserted. The pass transistor will disconnect the cell from the bit lines. So if the word line is not asserted then the access transistor or pass transistor does not let the memory cell to connect with the bit lines(bit and bit bar). This will cause the two cross coupled inverter formed to continue to strengthen each other to the supply. When cell is in standby mode no action could be taken and to store the data more power is consumed by the SRAM. So there is need of techniques to reduce the leakage current.

1.3 Read mode

The read operation is started by enabling the word line (WL) and joining the bit lines bit and bit bar to the internal nodes of the cell. The voltage of column bit is remained high and volume of bit bar is pulled down. Now the difference is amplified as a logic “1” output. The read operation for “0” is performed vice-versa. The difference between bit and bit bar should be minimum and this difference is sensed and amplified as logic “0”.

1.4 Write mode

The write operation is performed by applying the desired value to the bit line “Bit”. Like if we wish to write logic “1” then we make “Bit” to high and “Bit bar” to low. Similarly if we want to write logic”0” then we performed the operation vice-versa. The word line WL should be asserted for this mode.

3. DTCMOS

There are many techniques which reduce power dissipation and wake low power SRAM cell divided word line

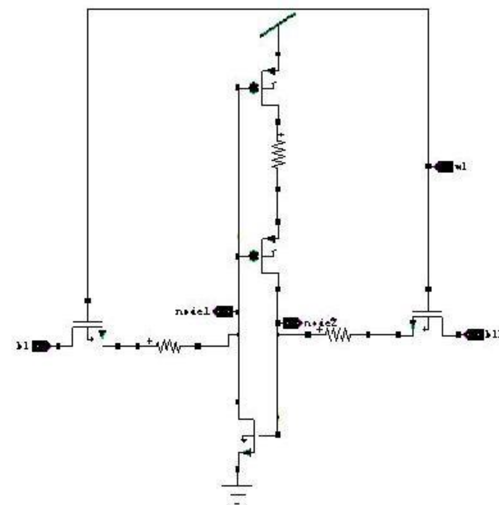

Fig2. 4T SRAM cell using RSL

architecture, memory banking architecture, pulsed word line and reduced voltage swing techniques are used to reduce only active power dissipation. On the other hand during standby mode, there is leakage power dissipation due to presence of sub threshold and gate tunneling leakage currents. To avoid these leakage, dual threshold (dual Vth) techniques applied on SRAM.

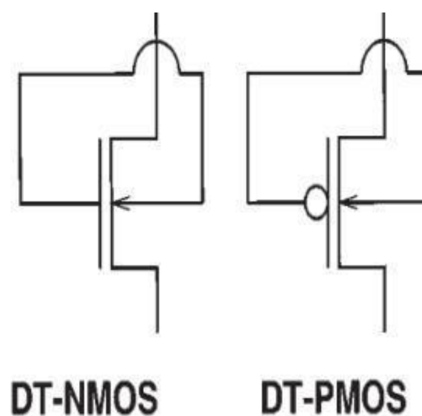

Fig3. Dual threshold nmos and pmos

Switching loss is fixed cause, but conduction loss by on resistance of switch is increased by an output current increased. When output current is increased, conduction loss is increased more than switching loss in high output current. Finally switching developments that have low on-resistance to heighten efficiency of SMPS is essential. In this paper we proposed DTCMOS without high leakage currents in high power supply voltages using this DTCMOS concept. When the switch is become ON, the body voltage of the switch MOS is controlled by diode connection CMOS and the threshold voltage is lowered. . When the switch is become OFF, body of CMOS is connected to each the power supply and the ground. When the switch is ON, the proposed DTCMOS due to low threshold voltage is low on- resistance than conventional

CMOS switches. Limitation of power supply voltage by the leakage current is overcome by minimizing body leakage current that is a DTCMOS fault through deciding supply and the ground.

In threshold MOS (DTCMOS) topology, gate of the transistor is connected to its substrate terminal. Therefore, the substrate voltage continuously changes with the gate voltage of the transistor. The change in the substrate voltage dynamically alters the threshold voltage. The DTCMOS behaves exactly like a normal transistor in the OFF state i.e. VIN = VDD (VIN=0) for PMOS (NMOS). Both exhibit exactly same parameters such as off current, threshold voltage etc. However, in the ON state as gate to source voltage (VGS) increases, substrate to source voltage (VBS) also increases. This further decreases the threshold voltage of DTCMOS transistor. The reduction in the threshold voltage is due to reduced body charges that increase the carrier mobility. This in turn lowers the effective normal field. All these effects collectively lead to a higher ON current in the DTCMOS transistor.

A DTCMOS circuit produces an output based on a logical combinational of input logic signals. The circuit includes input transistors which receive on a respective gate a respective logic signal. The transistors have a body contact which is connected to the gate of another transistor. Transistors which are receiving later arriving logic signals therefore have a threshold voltage lowered by an earlier arriving logic signal. By coupling the earlier arriving logic signal with a a body contact of the another input transistor, the threshold voltage may be lowered period to processing of the subsequently arriving logic signal. The DTCMOS circuit may be implemented in SOI with the attendant benefits of a lower supply made possible by the lowered voltage threshold each of the transistors without sacrificing leakage current inherent in DTCMOS circuits.

4. Dual Threshold CMOS (DTCMOS):

Data signals traverse integrated circuits through different paths of logic gates whereas the start-and end points of these paths are marked by sequential elements like registers. The maximum frequency to clock the registers is determined by the path with the longest propagation delay, called critical path. Thus, it is possible to trade off delay for leakage in all other, non-critical paths. Such an attempt is exploited by the Dual Threshold CMOS (DTCMOS) design technique. Therefore, this approach offers various gates for the same logical function that differ in evaluation delay and power dissipation due to leakage current. As shown, the transistor's threshold voltage *Vth* mainly determines delay and leakage. So, DTCMOS approaches apply fast gates with transistors that have low *Vth* (LVT gates).

Further, gates are used that have the same logical functions but consist of transistors with high *Vth* (HVT gates). These gates offer slower evaluation but also decreased leakage currents. Finally, to reduce the design's overall leakage currents at constant performance, as many HVT gates as possible are applied to the non-critical paths so that the delays of the paths do not exceed the critical path delay which consists solely of LVT gates.

5. SIMULATION RESULT

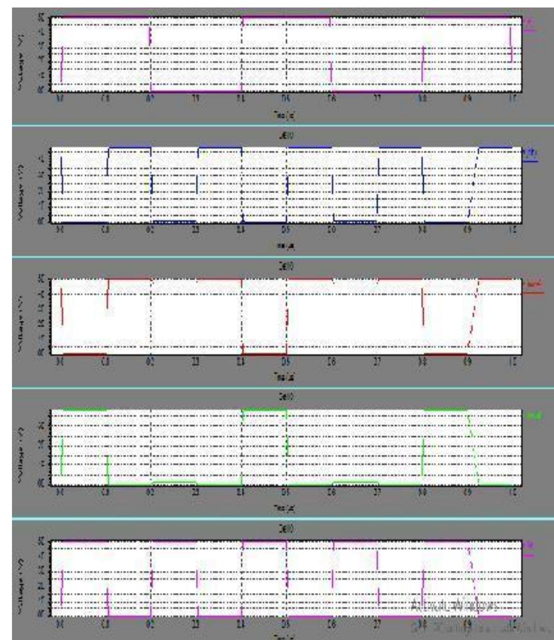

Fig4. 6T SRAM using CMOS logic

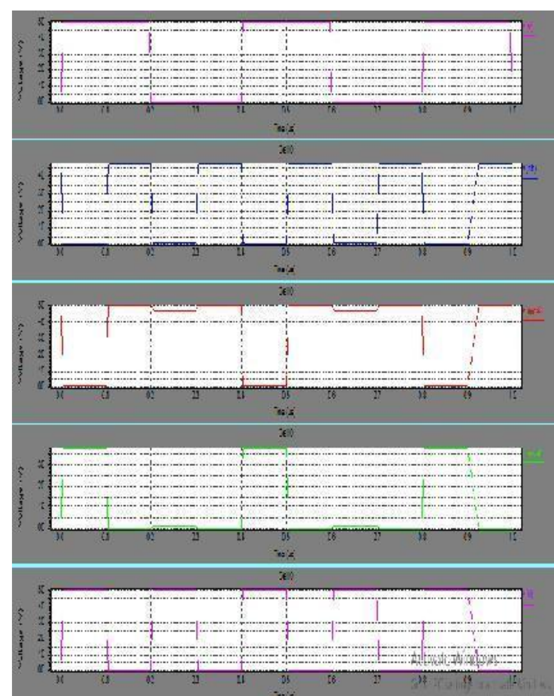

Fig5. 4T SRAM using RSL

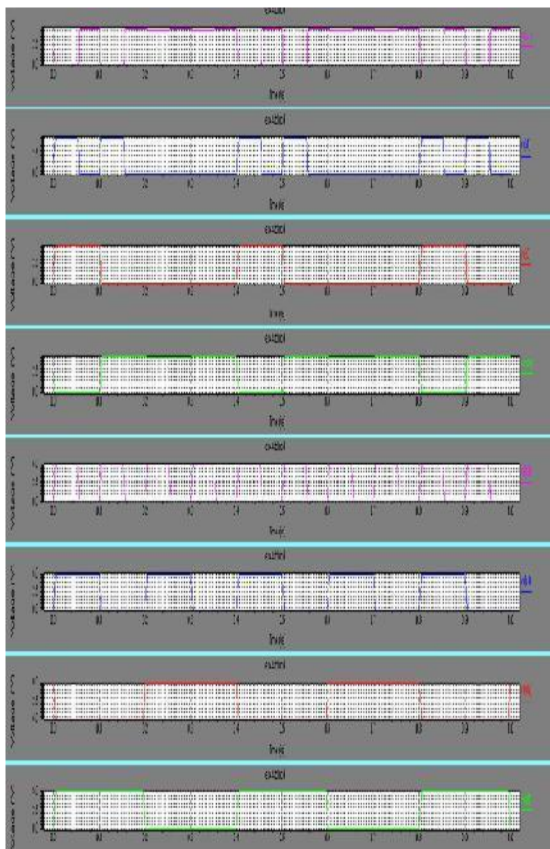

Fig5. 4T SRAM using double sleep with DTCMOS

Table- 1: Power analysis of RSL and DTCMOS

Design	Power Consumption in 65 nm Technology	Power Consumption in 45 nm Technology
4T SRAM with resistive switch logic	$5.83e^{-4}$ W	$4.13e^{-5}$ W
4T SRAM with dual threshold logic	$1.83e^{-4}$ W	$2.69e^{-5}$ W

6. CONCLUSIONS

This approach offers various gates for the same logical function that differ in evaluation delay and power dissipation due to leakage current. As shown, the transistor's threshold voltage *Vth* mainly determines delay and leakage. So, DTCMOS approaches apply fast gates with transistors that have low *Vth* (LVT gates). Further, gates are used that have the same logic function that consists of transistors with high *Vth* (HVT gates). These gates offer slower evaluation but also decreased leakage currents. Finally, to reduce the design's overall leakage currents at constant performance.

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