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SHIFT REGISTER USING CNT FET BASED ON SENSE AMPLIFIER PULSED LATCH FOR LOW POWER APPLICATION

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Abstract - *Recent day's power consumption and area reduction is the major concern in circuit design. Shift register is a basic building block of memory devices. In this design reducing power in shift register using pulsed latchesinstead of flip-flops. Because shift register based flip-flops consumemore power. The pulsed latches designed by Carbon Nano Tube technology. CNTFET technology is one of the best replacement of CMOS technology because of its excellent properties such as high thermal conductivity, small atomic diameter of carbon and also high tensile strength. Here shift register based on pulsed latches using CMOS technology and CNTFETtechnology has been compared. This shift register has been implemented in 32nm CNTFET technology in HSPICE.*

Key Words: **Pulsed latch, Shift register, Flip-flop, CNTFE*T* memory devics.**

1. INTRODUCTION

In the past area, speed, and cost is the major concerns of the VLSI designers. Power consideration is the second concerned. Now a day's power is the primary concerneddue to remarkable growth and success in the field of batteries based devices such as laptops, mobile phones, tablets etc. The motivations for reducing power consumption differ application to application.

There are different power minimization techniques are available. In a circuit three components are responsible for power dissipation: short circuit power, dynamic power and static power. Dynamic power is primary power dissipated when charging and discharging capacitors.

$$P_{dynamic} = C_L VDD^2 \alpha f \quad \ldots (1)$$

Shift registers are a sequential logic circuit. It is used to shifting the binary information and also canstorethatbinary information. So only shift registers are basic building blocks in memory devices.

The following sections includes conventional shift register, shift register using pulsed latch, shift register based pulsed latch using CNTFET are discussed.

2. LITERATURE SURVEY

Elio Consoli, et al., (2012) [1] presents Flip-flops (FFs) are key building blocks in the design of high-speed energy efficient microprocessors, as their data to outputdelay(D-Q) and power dissipation strongly affect the processor's clock period and overall power. From previous years the Transmission-Gate Pulsed Latch (TGPL) [3] proved tobethe most energy-efficient FF in a large portion of the design space, ranging from high speed to minimum ED (Energy Delay) product designs while simple Master-Slave FFs(TGFF and ACFF) are the most energy efficient in the low-power E-D space region. TGPL also has the lowest DQ delay along with STFF. However, the latter has considerably worse energy efficiency, hence, the TGPL is the best reference for a comparison. Seongmoo Heo, et al., (2007) [2] presentednew techniques to evaluate the energy and delay of flip-flop and latch designs and shows that no single existing design performs well across the wide range of operating regimes present in complex systems. We propose the use of a selection of flip-flop and latch designs, each tuned for different activation patterns and speed requirements. We illustrate our technique on a pipelined MIPS processor data path running SPECint95 benchmarks, where we reducetotal flip-flop and latch energy by over 60% without increasing cycle time. Bai Sun Kong, et al., (2001) [4] presented a family of novel low power flip flops, collectively called conditional-capture flip-flops (CCFFs). They achieve statistical power reduction by eliminating redundant transitions of internal nodes. These flip flops also have negative setup time and thus provide small data to output latency and attribute of soft-clock edge for overcoming clock skew-relatedcycletime loss. The simulation comparison indicates that the proposed differential flip flop achieves power savings of up to 61% with no impact on latency while the single ended structure provides the maximum power savings of around 67%, as compared to conventional flip flops. Borivoje Nikolic, et al., (2000) [5] presented a design and experimental evaluation of a new sense amplifier based flip-flop (SAFF). It was found that the main speed bottleneck of existing SAFF's is the cross-coupled set reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology that significantly reduces delay and improves driving capability. The performance of this flip-flop is verified by measurements on a test chip implemented in 0.18µm

effective channel length CMOS. Umiing KO, et al., (1996) [8] presented performance, power, and energy efficiency of several CMOS master slave D flip flops (DFF's). To improve performance and energy efficiency, a push pull DFF and a push pull isolation DFF are proposed. Among the five DFF's compared, the proposed push pull isolation circuit is found to be the fastest with the best energy efficiency.

3. CONVENTIONAL SHIFT REGISTER

The Shift registers are normally having group of flip-flops. Flip-flop is a 1 bit memory cell. In shift register the flip-flops are controlled by the clock. The number of flip-flops in shift register represent the number of bits used in it. When clock pulse is high data bit is enter into the first flip-flop in the shift register and the data is shifted to the other flip-flop during each clock pulse. The shifting is done by two ways, one is serial shifting and another one is parallel shifting. The following fig.1 shows the master slave flip-flop and based shift register.

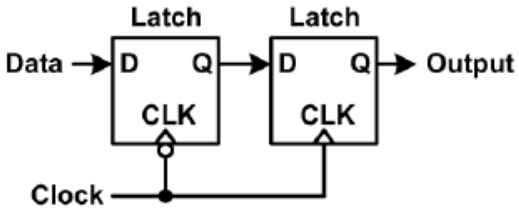


Fig-1: Master-slave flip-flop.

The following fig.2 represent the one of the flip-flop model namely Power PC Style flip-flop (PPCFF). It is fastest and high quality structure and have a short direct path and low power clock load.

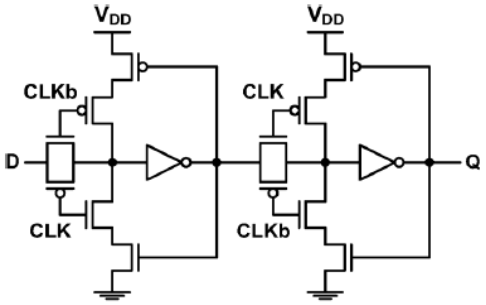


Fig-2: Schematic diagram of PPCFF.

An optimized shift registers are not designed by flip-flops because it consume more power and impose heavily clock load.

4. SHIFT REGISTER USING PULSED LATCH

4.1. Pulsed latch

The important parameters of shift register such as area, power and delay can be reduced by the use of pulsed latch. Pulsed latch means that combination of latch and pulsed clock generator. The fig.3 represent the pulsed latch circuit. Pulsed latch have small number of transistors compare with flip-flop. So the area of the shift register will become reduce. Pulsed latch is a latch that can capture the data during the particular time defined by the width of clock waveform. Pulsed latch uses narrow clock pulse so important low power characteristics such as clock power will be low.

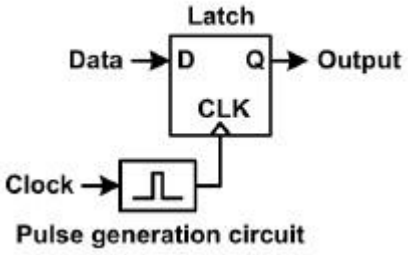


Fig-3: Pulsed latch circuit.

This shift register solves the timing problem between the latches by the use of multiple non overlap delayed pulsed clock signals. The pulsed clock generator generates the pulsed clock signals. Another one advantage of the pulsed latch is to reduce the hold time violations. Because pulsed latch is an ideal sequential component for high performance and low power VLSI design environment.

4.2. Pulse clock generator

Pulse clock signal generated in a pulse clock generator consisting of delay circuits and AND gate. The clock pulse width in the conventional pulse clock generator is larger than the summation of rising and falling times. But delayed pulsed clock generator produces pulse width is smaller than the summation of rising time and falling times.

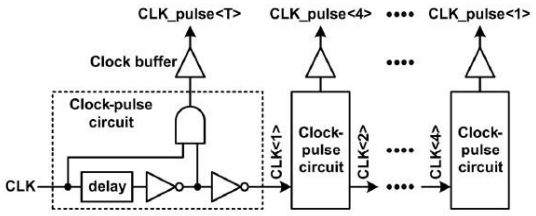


Fig-4: Pulsed clock generator.

Because each shape pulsed clock signals generated from the AND gate and two delay signals. So only this delayed pulse clock generator is suitable for generating narrow clockpulse

4.3. Sense amplifier pulsed latch

In this shift register based pulsed latch design, we select the one of the pulsed latch type is static differential sense amplifier shared pulsed latch (SSASPL). Because the short clock signal used in shift register cannot through the long wire due to the parasitic capacitance and resistance. The clock pulse shape is degraded at the end of wire because rising and falling times of clock pulse increases due to wire delay. One way to solve this problem by increase the clock pulse width but this makes decrease the clock frequency. Final solution of this problem is inserting the clockbufferfor send the clock pulse with small wire delay. The following figure shows the schematic diagram of SSASPL. It has small number of transistors (9) compare with otherpulsedlatches.

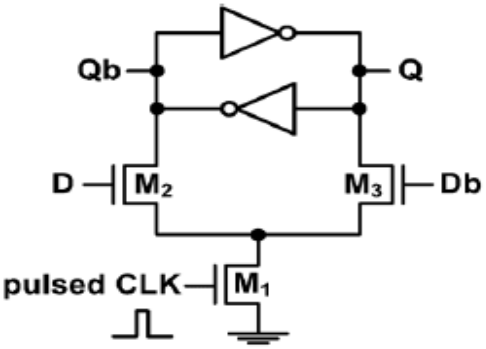


Fig-5: Sense Amplifier Pulsed Latch.

4.4. Shift register based SSASPL

The proposed shift register consisting of sense amplifier pulsed latch. The N bit shift register divided into M bit sub shift register. N bit shift register have N+1 latches because N latches for N bit and one for temporary latch is used for temporary storage the bit for next latch in next shift register. Dividing the N bit shift register is used to reduce the delayed pulse clock signals. Each shift register performs shifting operations with N+1 latches. This shift register solves the timing problem between the latches by using multiple non-overlap delayed pulsed clock signals instead of single pulsed clock signal. The following diagram the shift register using SSASPL.

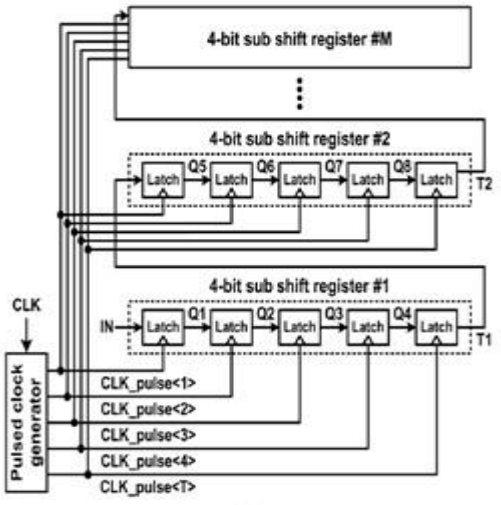


Fig-6: Shift register using SSASPL.

5. SHIFT REGISTER USING CNTFET

Carbon Nano Tube is a carbon allotropic variety, tubeshaped material and having a diameter measuring onthenanometer scale. It was discovered by Ijima in 1991. CNT is a suitable alternative to conventional silicon technology for future nano electronics because of their unique electrical and mechanical properties. Also has 1D ballistic transport of electrons and holes. Carbon Nano Tube Field Effect Transistor is a transistor that employs the single CNT or array of CNTs as a channel material instead of polysilicon in the conventional MOSFETs. CNTs play a role onbothsideson thermal insulation due to unique in that they are thermally conductive only along their length not sides of it. The important parameter of the CNT is chirality that means the distortion or direction to rolled by the grapheme. Carbon nano tubes are high strength and less weight material and flexibility allow for them to be added other materials. The structure of the CNTFET is same as the MOSFET except the CNT is attached between the source and drain then act as a channel.

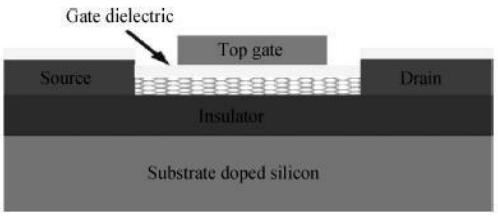


Fig-7: Schematic diagram of CNTFET.

Depending upon the number of tubes used in the channel, the CNT can be classified as follows, Multiwall Nano Tube (MWNT), Single wall Nano Tubes (SWNT). CNTFET can control the threshold voltage by changing the chirality or diameter of the CNT.

Fig-8: Rolled up sheet of grapheme.

The sense amplifier pulsed latch is used in the shift register. It requires pulsed clock signal and two differential inputs. It requires 17 transistors in which M1-M10 transistors are used to generate the pulsed clock signal. The remaining transistors M11-M17 represent the sense amplifier pulsed latch operations. Here 4 bit shift register is considered. Usually shift register classified into four types as following, serial in serial out (SISO), serial in parallel out (SISO), parallel in serial out (PISO), parallel in parallel out (PIPO). The following figure represents the proposed shift register based pulsed latch using CNTFET. It has three connectionfor data shifting operations. The proposed shift register containing five pulsed latch serially. The data enter into the one latch, the output from that latch is connected to the next latch. The additional latch in the shift register isusedtostore the data temporally then send to the next latch in the next shift register. The first type is serial in serial out shift register (SISO) which accepts the data serially and produces data on output serially. The following diagram represents the serial in serial out shift register using CNTFET.

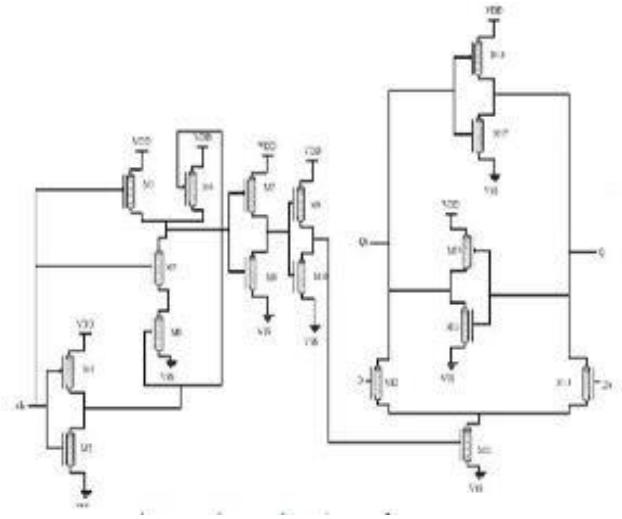


Fig-9: Schematic diagram of SSASPL using CNTFET.

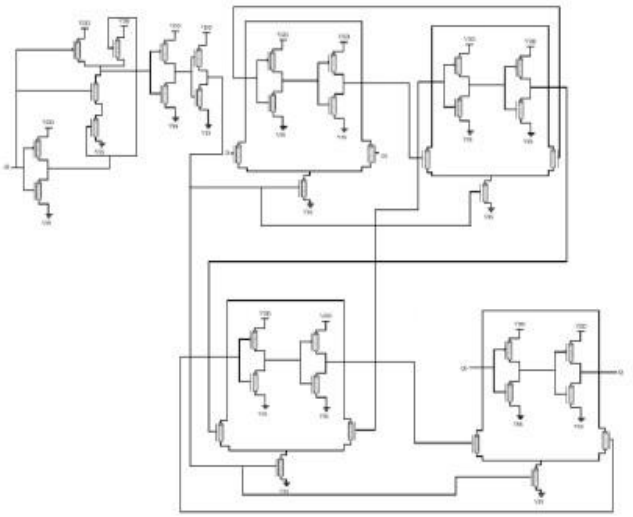


Fig-10: Serial in serial output shift register using CNTFET.

6. SIMULATION AND RESULTS

This section includes simulation of shift register using flip-flop, pulsed latch. The shift register using PPCFF simulation as shown in fig.

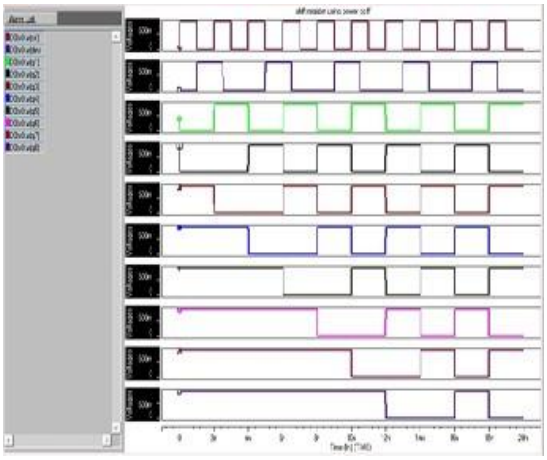


Fig-11: Shift register using PPCFF.

Pulse clock generator simulation as shown in following fig. the clock input is given to the inverter and followed by AND gate then buffer. The buffer is used to store the data temporally then send to the SSASPL in shift register.

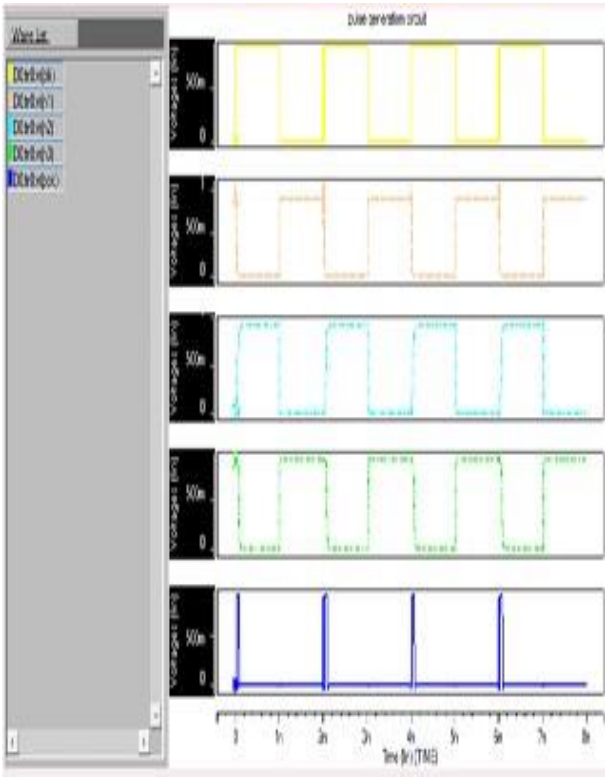


Fig-12: Waveform of pulse clock generator.

The output of the pulsed clock generator is send to the input of the one NMOS transistor in SSASPL. The waveform of the SSASPL is as shown in fig.

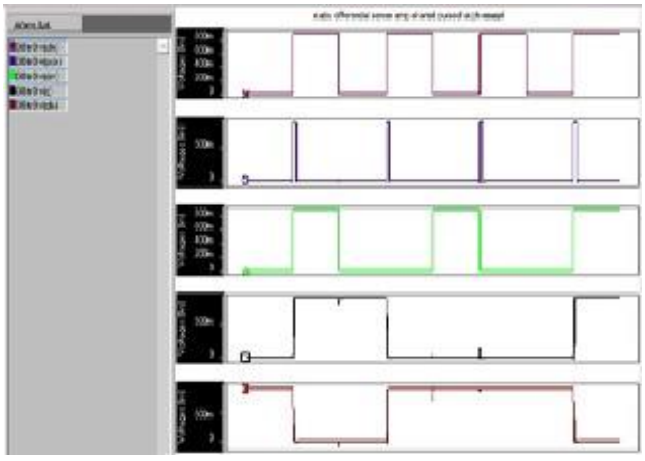


Fig-13: Waveform of the SSASPL.

Finally, the output of shift register based pulsed latch using CNTFET technology is as shown in fig.

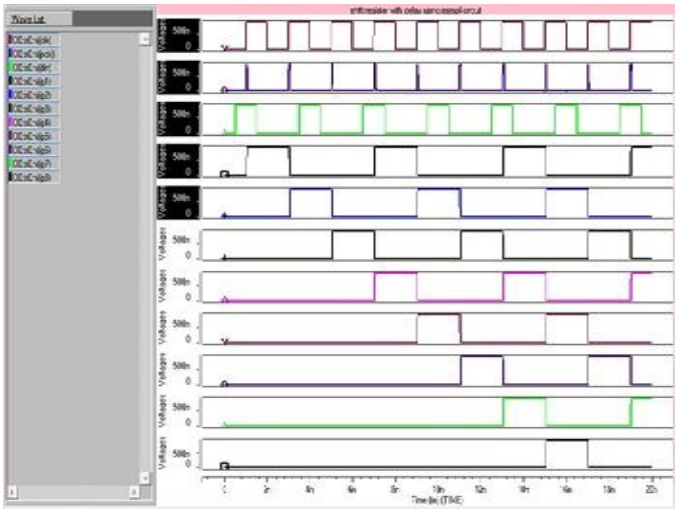
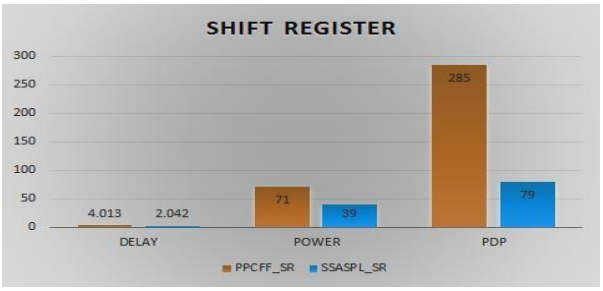


Fig-14: Waveform of shift register based pulsed latch using CNTFET.

And also compare the power delay product of PPCFF and SSASPL based shift registers.



C hart-1: Delay,power and powerr delay product(PDP) comparison of two shift register.

The following table represents the transistors comparison between the pulsed latches and flip-flops**.**

Table-1.Transistors comparison.

Type	Number of Transistors
Sense amplifier pulsed latch	**7**
Transmission gate pulsed latch	10
Hybrid latch flip-flop	14
Power PC style flip- flop	**16**
Strong ARM flip-flop	18
Data mapping flip-flop	22
Adaptive coupling flip-flop	22

7. CONCLUSIONS

This paper proposed the low power sense amplifier pulsed latch based shift register using CNTFET technology. Through the discussion we can conclude CNTFET is best replacement of MOSFET due to their power dissipation and delay.

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