International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 04 | Apr -2017 www.irjet.net p-ISSN: 2395-0072

A Novel Adder Logic Design for Power Delay Product Minimization

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Abstract - *Adders are widely used in the VLSI based application to perform arithmetic operations such as microprocessor and DSP. The low power and high speed architecture is the major concern in the adder circuit design. To achieve compactness and low power consumption, we need to reduce the number of transistors in one bit full adder. To design and analyze various one bit full adder circuits. In order to achieve a better performance a novel method of adder logic called 6T 1-Bit full adder has been proposed. The proposed logic is based on XOR-XNOR logic style which generates full swing output simultaneously. By using this technique the design has been extended to 8-Bit carry select adder (CSLA). Because the CSLA is compromise between RCA and CLA (Carry Lookahead Adder). The 120nm technology layout for basic building block (6T full adder) and 8-bit CSLA circuits has been designed in Microwind and DSCH software. The result analysis shows that the proposed adder circuit is highly efficient in terms of power, delay and PDP compared to existing full adder circuits. The Power Delay Product of the proposed 6T Adder was found extremely very low (0.00012FJ). As for the 8-bit CSLA, the average power consumption is 0.529 µW.*

***Key Words*: – Full Adder (6T), Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Low Power, Power Delay Product (PDP).**

1. INTRODUCTION

Arithmetic operations are frequently used in many VLSI-based systems. The design of faster and highly reliable adders is of major importance in such systems. The ever increasing demand for electronic devices requires the use of power efficient VLSI circuits. Increased usage of the battery operated portable devices, like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, and ultra large-scale integration designs with an improved power, delay characteristics. Now a day, designing of low power and high speed performance VLSI circuits is one of the biggest challenges. Also power and delay parameters of any VLSI circuit can't be reduced at the same time, but we can optimize these two parameters. There is demand for compact low power devices in the market. Full adder is being one of the most fundamental building blocks of all the arithmetic circuit applications. In ALU, Full Adder performs the addition bit by bit with carry input. The full-adder circuit adds three one-bit binary numbers (A,B,C) and outputs two one-bit binary numbers, a sum (S) and a carry (C_{out}). The Boolean equation is given below

SUM = A XOR B XOR C (1)
CARRY = (A AND B) OR (B AND C) OR (C AND A) (2)

2. REVIEW OF FULL ADDER TOPOLOGIES

In this section, several different designs of low power and high speed adders are introduced. There are several conventional adder logic such as CMOS adder, Mirror adder, Transmission gate adder, each having its own merits and bottlenecks which require 28, 24, 20 transistors respectively for the implementation of 1-bit full adder. To reduce the transistor count, four type of 1bit full adder transistor adders are reviewed they are 16T (hybrid adder), 10T (SERF Adder), 8T, 6T adders.

2.1 Complementary Metal Oxide Semiconductor (CMOS)

In general the Standard CMOS logic design consists of pull-up and pull-down network. A classical design of standard static CMOS full adder is based on regular CMOS structure using 28 transistors with conventional pull-up and pull-down Transistor. The existence of the PMOS block in static CMOS circuits is a main drawback because it has low mobility compared to the NMOS, high noise margin and weak output driving capability.

2.2 Mirror Adder

The 24 transistors are used for the implementation of one bit full adder. A maximum of two series transistors can be observed in the carry-generation circuitry. The N-MOS and P-MOS chains are completely symmetrical. The reduction of the diffusion capacitances is particularly important. The capacitance at node *Co* is composed of four diffusion capacitances, two internal gate capacitances, and six gate capacitances in the connecting adder cell.

2.3 Transmission Gate Adder (TGA)

In TGA both (PMOS & NMOS) combined in parallel fashion. PMOS and NMOS act as a switch in complementary mode.

There are 20 transistors are required to construct one bit full adder.

2.4 Hybrid Adder

There are 16 transistors are required for the design of one bit hybrid full adder (Fig. 1). Hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation. And it has some voltage degradation problem.

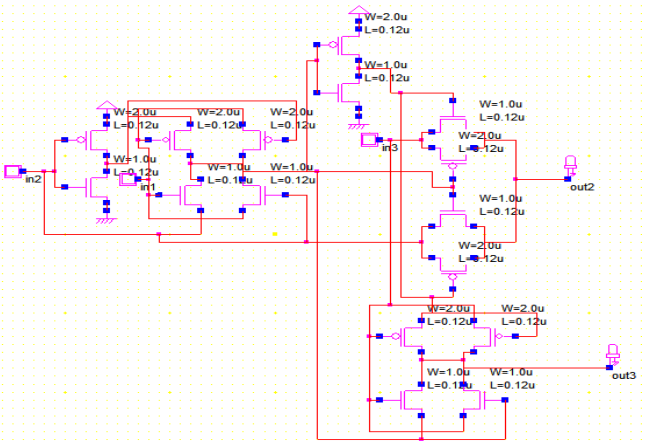

Fig -1: One bit hybrid full adder

2.5 Static Energy Recovery Full Adder (SERF)

The Static Energy Recovery adder (Fig. 2) is the extreme low power design because in this design there will be direct contact path between supply and ground. Due to this, it suffers from static power dissipations. It requires 10 transistors for the construction of one bit full adder.

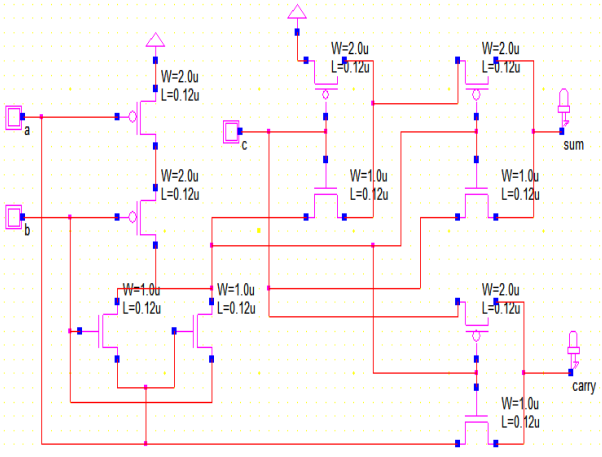

Fig -2: One bit static energy recovery full adder

2.6 8T Adder

The XOR gate is replaced by XNOR gate. So the need for inverter is avoided. This reduces the transistor count to 8. The simulation results show that the output voltage swing of 8T adder is not as good as SERF adder. One of inverters is reduced in 8T adder design. The 8T adder also requires inverting input Cbar as in the case of SERF adder. The only advantage of 8T adder is that transistor count is reduced to 8 from 10. The same equations used for SERF adder is used here. There is only one drawback in the proposed circuit that it has poor time delay comparative other circuits.

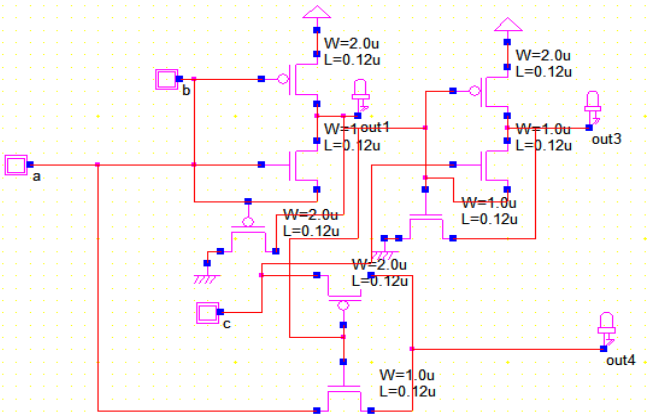

Fig -3: One bit 8t full adder

3. DESIGN APPROACH OF THE PROPOSED FULL ADDER

The XOR-XNOR logic style is used in proposed 6T full adder which produces full swing output. In the proposed 6T full adder sum is generated using 2 transistor XOR module twice, PMOS and NMOS is used to generate the carry. The full adders of various designs of less transistor count will be in use of 3- module implementations that is XOR or XNOR for both sum as well as carry generating modules. The design of PTL based technique will be required 4 transistors in least to design a XOR or XNOR model. The symbolic diagram of 6T adder is

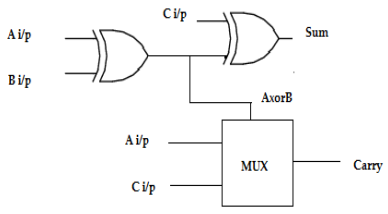

Fig -4: Symbolic circuit diagram of proposed full adder

The main concern of this design is to use the tristate inverter in the place of normal inverter which has been used for all low power designed circuits; because of the power consumption of the tristate inverter is less compared to normal one. We have used two XOR cells and transmission gate multiplexer to design the full adder. Sum is generated by two XOR gates Carry output is generated by 2×1 multiplexer (MUX).

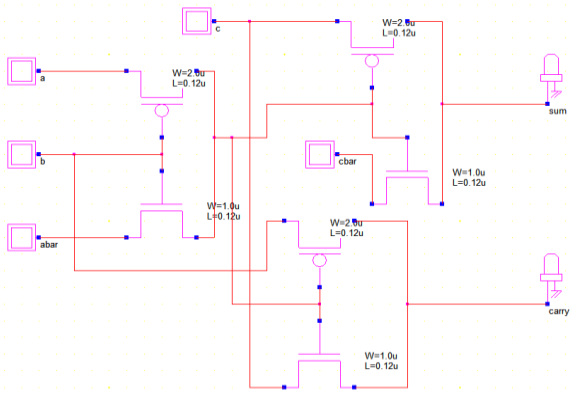

Fig -5: Proposed 6T full adder.

In this design (a XOR b) signal is passed to the pass transistor based multiplexer made of two transistors to choose one among two signals. To generate carry (a XOR b) is sent to multiplexer to choose between a, c and to generate sum (a XOR a) is sent to choose between cbar, c. This simulation results comparatively less power consumption than the earlier designs.

i) Dynamic Power: For reducing the dynamic power output and input capacitance values can be minimized. The power consumption of a CMOS digital circuit can be represented as where f is the clock frequency, C is the average switched Capacitance per clock cycle, VDD is the supply voltage, J short is the short circuit current, and J leak is the off current. The Charging and discharging a capacitive output load further increases this dynamic power consumption. The dynamic power consumption can be calculated by

$$Power_d = V_{DD} * f_c * \sum_{j=1}^{N} \alpha j * Cloadj * \Delta Vj \quad (3)$$

ii) Static Power: The static power is the power dissipated by a gate when it is inactive or idle. For reducing the short and static power, avoid using both V_{dd} and GND simultaneously in circuit's components (i.e) there is no direct path from vdd to gnd.

$$Power_s = Vdd * Idd \quad (4)$$

4. PERFORMANCE ANALYSIS OF THE PROPOSED 1-BIT FULL ADDER

The proposed adder requires only 6 transistors whereas the other adders require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other full adders. The use of less number of transistors in this paper also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed 6T full adder is significantly improved in comparison with the earlier type of adders. The detailed comparison of the proposed full adder with other full adders in 120-nm technology is represented in Tables 1.

Table -1: Simulation Result for Full Adders in 120nm Technology with 1.2 Power Supply

ADDER DESIGN	PDP(fj)	AREA(μm²)	TRANSISTOR COUNT
(Hybrid)16T	32.77040	156.8	16
(SERF)10T	38.36400	179.6	10
8T	13.00800	162.3	8
(Proposed) 6T	0.000012	117.9	6

The performance of the proposed full adder in terms of power consumption and propagation delay with variation in supplied voltage was carried out (not shown here) and the corresponding comparison of the PDP (with the other existing designs) is shown in Fig. 6.The output waveform of proposed adder is shown in Fig. 7.

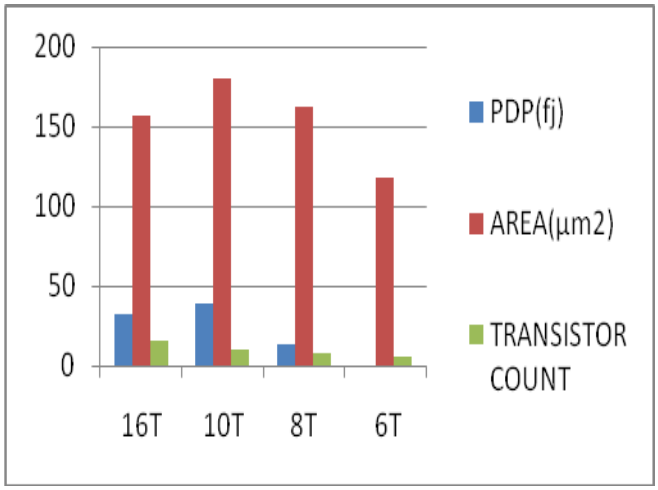

Chart -1: Comparison of various one bit full adder designs

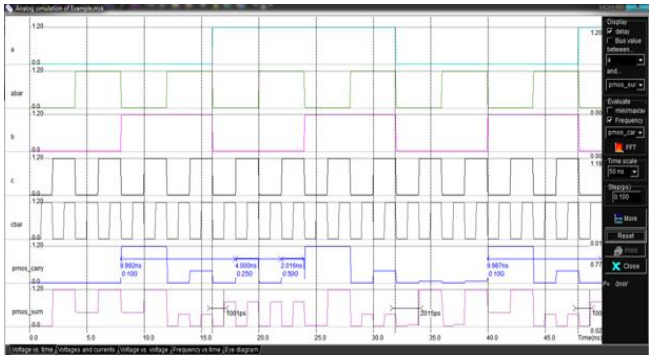

Fig -7: Output waveform for proposed 6t full adder circuit.

5. 8-BIT ADDER LOGIC DESIGN

By using one bit full adder, we can construct the adder logic cells such as ripple carry adder, carry look ahead adder, carry skip adder and carry select adder etc., Ripple carry adder is one of the efficient adder which is easy to design and also easy to analyze but slow in processing. Each full adder inputs carry C_i which is the input of previous adder input as shown in Fig 8. Since each carry bit "Ripples" to the next full adder.

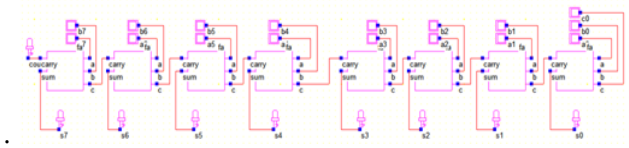

Fig -8: 8-bit RCA using 1-bit full adder

An 8-bit carry select adder is implemented as an extension of the proposed 1-bit full adder shown in Fig 9. It is compromise between RCA and CLA.

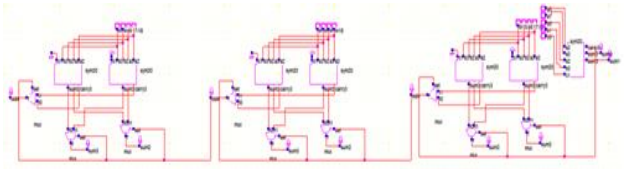

Fig -9: 8-Bit CSA Using 1-bit Full Adder

6. PERFORMANCE OF 8-BIT ADDER LOGIC DESIGN

Table -2

DESIGN	POWER (µW)
RCA	9.726
CSA	0.526

The Table 2 shows that performance analysis of 8 bit RCA and CSLA by 120nm technologies. Compared to (Fig. 10) RCA, the CSLA achieve a better performance in power consumption.

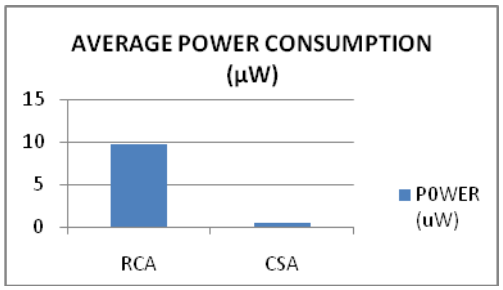

Fig -10: Comparison of 8-bit RCA and CSLA

6. CONCLUSION

The simulation results of the novel 6T full adder have been compared with the previous designs like hybrid adder(16T), SERF (10T), 8T using Microwind tool in 120nm technology. According to the simulation, the proposed circuit consumes less area and power. Results established that the proposed adder offers improved PDP compared with the earlier reports. The 1-bit 6T full adder has been used to implement an 8-bit Carry Select Adder and it is found that average power consumption is only 0.526µW compared to 8-bit RCA. The post layout simulation have been done for both the proposed circuits (Novel 6T FA and 8-bit CSLA).

Layout of Proposed Circuits

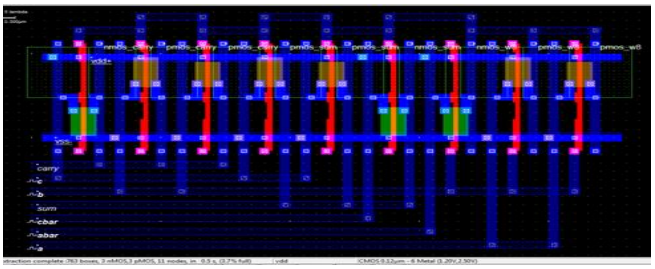

Fig -11: Layout of 1-bit full adder (Proposed 6T) in 120nm technology

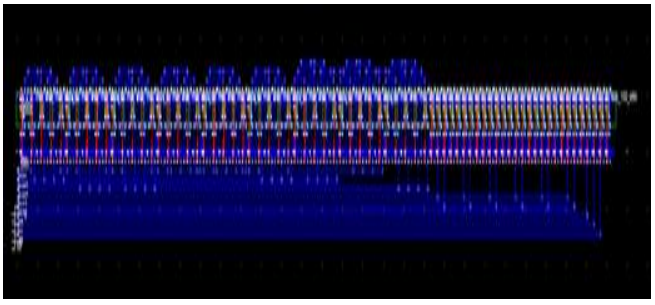

Fig -12: Layout of 8-bit carry select adder in 120nm technology

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