Highly Reliable Radiation Hardened Memory Cell for FINFET Technology

Shantha Devi.P[1], Vennila.P[2], Ramya.M[3], Krishnakumar.S[4]

[1]*PG Scholar,Department of ECE,Theni Kammavar Sangam College of Technology,Tamilnadu,India.*
[2]*PG Scholar,Department of ECE,Theni Kammavar Sangam College of Technology,Tamilnadu,India.*
[3]*PG Scholar,Department of ECE,Theni Kammavar Sangam College of Technology,Tamilnadu,India.*
[4]*Assistant Professor, Department of ECE,Theni Kammavar Sangam College of Technology,Tamilnadu,India.*

---***---

Abstract - *The need for low power circuit is well known because of their extensive use in the electronic portable equipments. The scaling of CMOS devices to nanometer regime results in increased process variations, increased leakage current and short channel effects which not only affect the reliability of the device but also performance expectations. FINFET is expected to replace conventional MOSFETs for integrated memory applications due to its better resistant to some of the sources of intrinsic parameter fluctuations. The 6T/8T SRAM cell was designed in 32nm FINFET technology. It provides better power and PDP compared to MOSFET. But it cannot withstand in soft errors. Hence low power and highly reliable radiation hardened SRAM memory cell (RHM) using 12T &14T is proposed to provide enough immunity against single event upsets (SEUs) in 32nm FINFET technology. The proposed cell can not only tolerate upset at its any sensitive node regardless of upset polarity and strength, but also recover from multiple-node upset induced by charge sharing on the fixed nodes independent of the stored value. Moreover, the proposed cell has comparable or lower overheads in terms of static power, area and access time compared with previous radiation hardened memory cells.*

***Key Words*: Scaling, Reliability, Radiation hardened memory (RHM), single event upsets (SEUs) FINFET, 12T SRAM, 14T SRAM.**

1. INTRODUCTION

Very Large Scale Integration (VLSI) is the process of creating an integrated circuit(IC) by combining thousands of transistors in to a single chip. An electronic circuit might consist of a CPU, RAM, ROM and other glue logic. VLSI lets IC makers add all of these into one chip. Memory is an indispensable part of computer and microprocessor based systems. Memory is an indispensable part of computer and microprocessor based systems. The data used in a program as well as the instructions for executing the program are stored in the memory. Hence, digital systems require memory facilities for temporary as well as permanent storage of data to perform their functions. Over the past decades, the MOSFET has continually been scaled down in size, typical MOSFET channel lengths were once several micrometers, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. The difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation [3]. MOSFET has some technical problems like i) short channel effects and ii) Corner Effect Corner. So to overcome the difficulty faced by traditional MOSFET, FINFET came into role and to make the transistors more efficient. The FINFET has been developed to overcome the problems faced by MOSFET [5]. It is basically a multi gate Field Effect Transistor which has been scaled further of MOSFET. It has all properties similar to a transistor, but has some advantages on CMOS. Independent gating of the FINFETs double gates allows significant reduction in leakage current.

In this paper, low-power and highly reliable radiation hardened SRAM memory cell (RHM) using 12T&14T is proposed to provide enough immunity against single event upset in 32nm FINFET technology [4]. The proposed cell can not only tolerate upset at its any sensitive node regardless of upset polarity and strength, but also recover from multiple-node upset induced by charge sharing on the fixed nodes independent of the stored value. In this paper, simulation is carried out in HSPICE 2008.3 software with the help of 32nm FINFET PTM files [14].

2. LITERATURE SURVEY

Ashok Kumar.C [1] discusses the issues in design of SRAM memory cell for low power applications. Here 6T architecture SRAM cell is taken as a reference model which is designed using 180nm technology and area, power and speed is estimated. Kalsoom Mehrabi [6] proposed a new seven transistor (7T) SRAM cell that improves read stability and write ability of conventional 6T SRAM cell. Separating read & write access transistor in this cell solves the conflict of access transistor sizing. Using the virtual ground in this design causes leakage power reduction for each cell by

stacking effect. Maisagalla Gopal [9] proposed a novel eight transistor (8T) CMOS SRAM cell design to enhance the stability and to reduce dynamic and leakage power. The Stability of the proposed cell has been analyzed using N-curve metrics. Zhiyu Liu [13] proposed new nine transistor (9T) SRAM cell for simultaneously reducing leakage power & enhancing data stability. The read static noise margin of proposed 9T circuit is enhanced by 2 times compared to 6T SRAM cell. Shiny Grace [12] proposed a 10T SRAM cell with reduced power & with improved static noise margin. The 10T SRAM employs a single bit line with dynamic feedback control which enhances the SNM at ultra low power. Further, the power consumption is trimmed down by the use of transistors.

3. CONVENTIONAL 6T AND 8T SRAM MODEL

3.1 6T FINFET SRAM

3.1.1 Operation of 6T SRAM

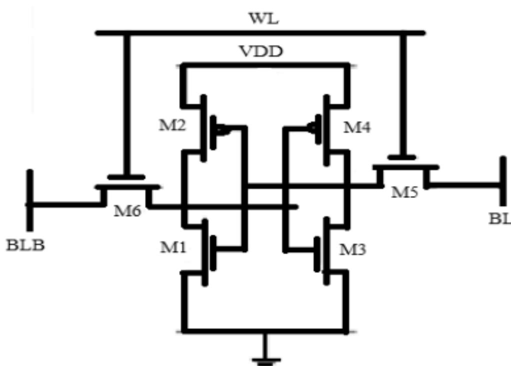

Fig -1: Conventional 6T SRAM

Standby Mode: Word line is not asserted in this mode *(*WL=0*)*, so access transistors M5 and M6 will be OFF and no data will be accessed by the bit-lines as shown in figure 3. The cross-coupled inverters will continue to feedback each other and hold the data in the latch as long as it is connected to the supply.

Read Operation: Word line is asserted (WL=1), which enables both the access transistor and connect cell from the bit lines BL and BLB. In read operation value stored in the nodes Q and QB are transferred to respective bit-lines BL and BLB. If 1 is stored at node *Q* then M2 and M4 will be ON and M1 and M3 will be OFF. BLB will be discharged through the driver transistor M4 and BL will be pulled up through the load transistor M2 toward VDD.

Write Operation: Word line is asserted (WL=1). If 1 is stored in the cell and 0 is to be written then bit line BL will be lowered to 0V and BLB is raised to VDD. For proper functioning of SRAM cell i.e. read and write operation certain aspects have to be taken in mind. These design issues decide the stability of read and write operations.

3.2 8T FINFET SRAM

The architecture of the 8T SRAM FinFET that stores *i* bits in one block. The minimum operating voltage and area per bit of the proposed SRAM depend on the number of bits in one block. A configuration that stores four bits in one block is selected as the basic configuration by considering the balance between the minimum operating voltage and the area per bit. The minimum operating voltage and area per bit of the proposed SRAM depend on the number of bits in one block. A configuration that stores four bits in one block is selected as the basic configuration by considering the balance between the minimum operating voltage and the area per bit. The basic configuration of the proposed SRAM includes four cross-coupled inverter pairs, pass gate transistors (PGL1~4 and PGR1~4), block mask transistors (MASK1 and MASK2), write access transistors (WR1 and WR2), read buffers (RD1 and RD2), a head switch (P1), and cross-coupled PMOSs (P2 and P3).

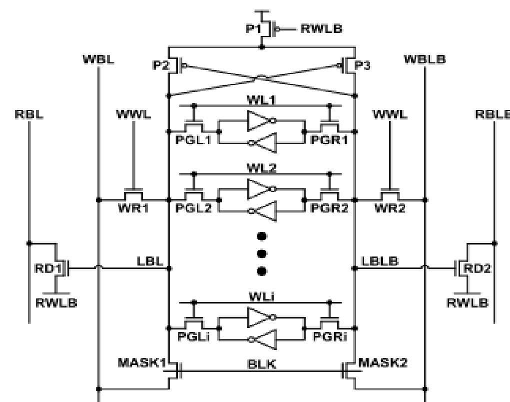

Fig -2: 8T SRAM FINFET Architecture

3.2.1 Operation of 8T SRAM

Hold State: WLs, WWL, and WBLs are held at 0 V. BLK is held at *V*DD to connect the WBLs and the LBLs, so that the LBLs are discharged to 0 V and the read buffers are turned OFF. Further, the RWLB is also held at *V*DD to turn OFF the head switch and to eliminate the RBL leakage current.

Read Operation: This operation is performed in two phases. During the first phase, BLK of the selected block is forced to remain at 0 V, and the selected WL is enabled. The read operation in the first phase is similar to that of the average-

8T SRAM, except that the RBL is not discharged because the RWLB is high in the first phase. With the assertion of WL, although the 1 storage nodes is disturbed, the read disturbance is small because of the small capacitance at the LBL. This smaller read disturbance makes the proposed SRAM be able to operate in significantly lower operating voltage compared with 6T SRAM cell. The second phase starts with the falling of the RWLB. The assertion of the RWLB enables not only the discharge of the RBL but also the feedback of cross-coupled pMOSs Positive feedback of the cross-coupled pMOSs increases the LBL to the value of the full VDD, owing to which the LBL can achieve a full swing, and the gate of the read buffer is driven by the full VDD, without the need for a boosted WL voltage. Thus, in the FinFET technology suppressed WL voltage can be used to enhance the read stability, without degrading the read delay. The suppressed WL voltage is used to enhance the read stability, and the full-swing LBL minimizes the read delay. In the case of 8T SRAM MOSFET architecture, the read buffer consists of two stacked nMOSs that reduce the RBL leakage. In Proposed SRAM architecture, a single nMOS is used as the read buffer to increase the read current, and the buffer foot is attached to reduce the RBL leakage. The column half-selected block is in the hold state in which the read buffers are turned OFF, so that the RBL discharge is not affected by the column half-selected block.

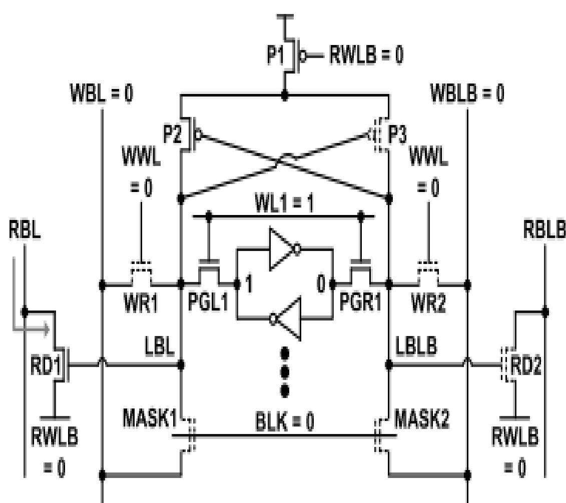

Fig -3: 8T FINFET SRAM Read Operation

Write operation:

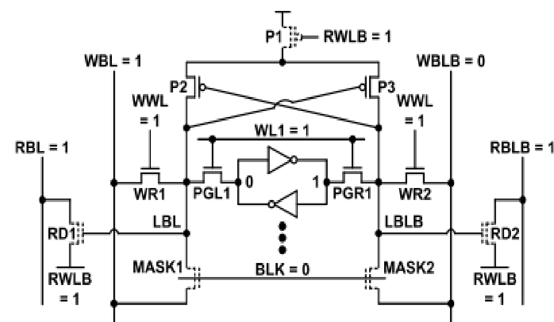

Fig -4: 8T FINFET SRAM Write Operation

BLK of the selected block is forced to remain at 0 V, and the selected WL is enabled. Further, the WWL is forced to remain at VDD so that the write access transistors are turned ON, and the WBLs are forced to remain at a certain voltage level on the basis of the write data. Both the storage nodes are connected to the WBLs through pass gate transistors and write access transistors. Thus, the write operation is differential, and the write ability of the proposed SRAM is better than that of average-8T SRAM, whose write operation is single-ended.

4. ADVANCED SRAM MODEL

Single event upsets (SEUs) induced by particle radiation are becoming an increasing important threat to the reliability of memories fabricated in nanoscale CMOS technologies. SEUs are caused by particle-induced charge which is derived from direct ionization from heavy ions and indirect ionization from protons and neutrons. An energetic particle passes through the sensitive node of a semiconductor device it frees electron-hole pairs along its path as it loses energy. The electric field present in a reverse-biased junction depletion region can separate electron-hole pairs, so that the particle-induced charge is very efficiently collected through drift processes leading to an accumulation of extra charge at the sensitive node.

4.1 12T FINFET SRAM

A new low-power and highly reliable radiation hardened memory cell (RHM-12T) is proposed using 12 transistors, which is capable of fully tolerating SEU at its any sensitive node, but also can tolerate multiple-node upset on two fixed nodes independent of the stored value.

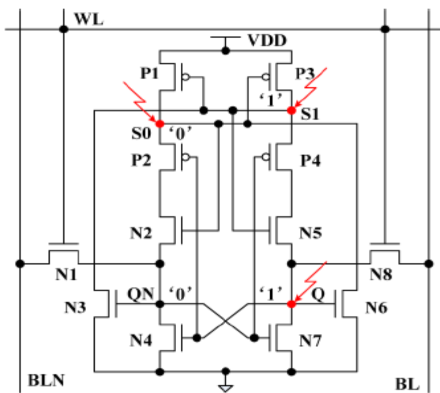

Fig -5: Proposed radiation hardened memory cell RHM-12T

4.1.1 Operation of 12T SRAM

Hold Operation: Word line WL is ‘0’, transistors P3, P4, N5, N6 and N4 are turned ON and the other transistors are turned OFF. It is shown that the state of the memory cell is maintained.

Read Operation: Bit lines BL and BLN are precharged to VDD. When word line WL is ‘1’, node Q keeps its initial state ‘1’, because transistors P3, P4 and N5 are still ON. However, bit line BLN is discharged through transistors N1 and N4. Then according to the voltage difference between bit lines BL and BLN, the state of the memory cell is output by a differential sense amplifier.

Write Operation: word line WL is ‘1’, and bit lines BL and BLN are set to ‘0’ and ‘1’ respectively. Node QN is forced to ‘1’, thus transistors N7, N3, P1 and N2 are turned ON, transistors P3, P4 and N5 are turned OFF. Simultaneously node Q is pulled down to ‘0’ so that transistors N4 and N6 are both OFF and transistor P2 is ON. Then word line WL is changed to ‘0’, the new state of the memory cell is stored.

4.2 14T FINFET SRAM

The proposed 14T SRAM is demonstrated in figure 6 and then operation of 14T SRAM is also explained as follows.

A new low-power and highly reliable radiation hardened memory cell (RHM-14T) is proposed using 14 transistors, which is capable of fully tolerating SEU at its any sensitive node, but also can tolerate multiple-node upset on two fixed nodes independent of the stored value.

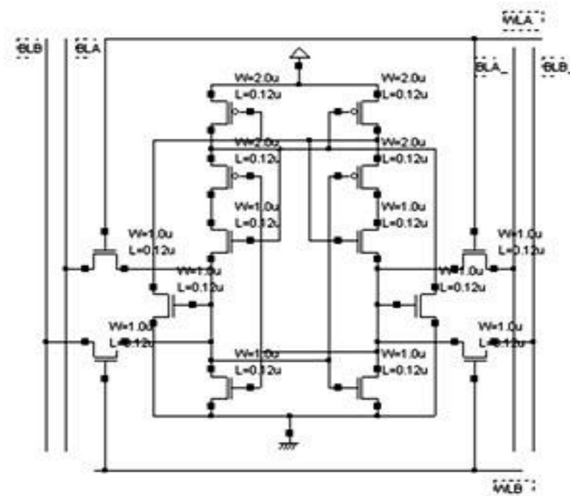

Fig -6: Proposed radiation hardened memory cell RHM-14T

4.2.1 Operation of 14T SRAM

The 14T SRAM is a dual port memory cell but read & write operations are similar to 12T SRAM. Here we can do the following operations simultaneously,

1. Read –Read operation

2. Write –Write operation

3. Read – Write operation

If WLA=1 then the data in the bit lines BLA & BLA_are stored in the output node Q & QB through the access transistors (N1, N8). Simultaneously we can assert WLB (1) the data in the bit lines BLB & BLB_ are stored in the output node Q & QB through the access transistors (N9,N10).For read operation, the data stored in the output node Q & QB are transferred to both the bit lines BLA’s & BLB’s simultaneously by enabling the word lines WLA(1) & WLB (1).

5. SIMULATION RESULTS

The 32nm FINFET based SRAM cell has been developed using the spice code and it is analyzed through the Synopsys spice software tool HSPICE with the help of 32nm Predictive Technology Models which is obtained from ptm.asu.edu. The following are the FINFET SRAM results for 12T & 14T.

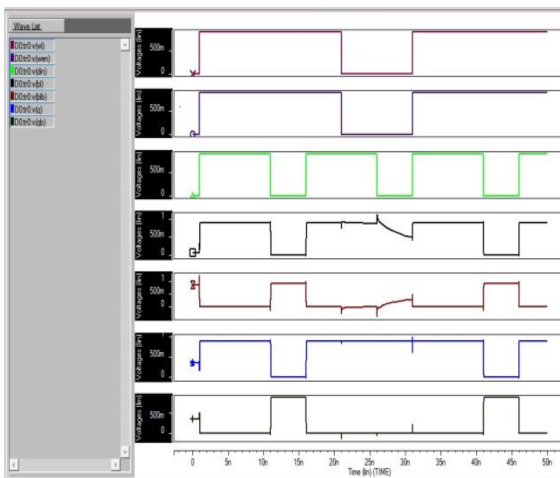

Fig -7: 12T FINFET SRAM Write Operation

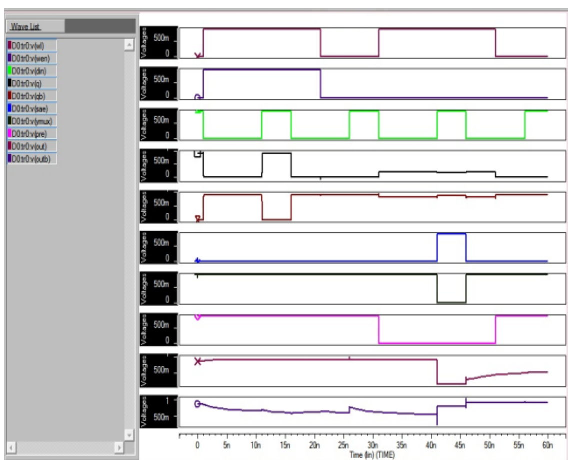

Fig -8: 12T FINFET SRAM Read Operation

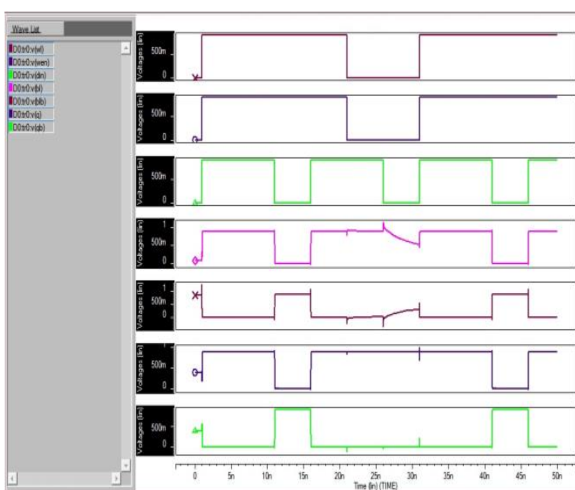

Fig -9: 14T FINFET SRAM Write Operation

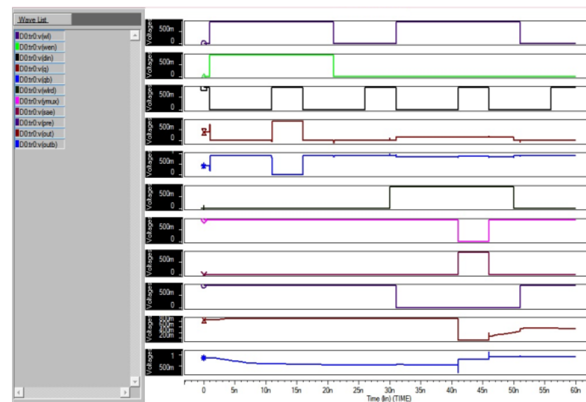

Fig -10: 14T FINFET SRAM Read Operation

6. CONCLUSIONS

FINFET was a promising substitute for bulk CMOS. In this paper, low power and highly reliable radiation hardened SRAM memory cell (RHM) using 12T &14T is proposed to provide enough immunity against single event upsets (SEUs) in 32nm FINFET technology. It was simulated using HSPICE-Simulator and output waveform was displayed on Avanwaves. Performance metrics like Delay, Power and Power Delay product (PDP) calculations for 12T & 14T SRAM had been done in 32nm FINFET technology. The proposed cell can not only tolerate upset at its any sensitive node regardless of upset polarity and strength, but also recover from multiple-node upset induced by charge sharing on the fixed nodes independent of the stored value. Moreover, the proposed cell has comparable or lower overheads in terms of static power, area and access time compared with previous radiation hardened memory cells.

REFERENCES

[1] Ashok Kumar.C (2016), "Performance Analysis of Low Power 6T SRAM Cell in 180nm and 90nm", IEEE.

[2] Chang I.J , Kim J.J , Park S.P ,Roy K , (2009), 'A 32 kb 10T Sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS', IEEE J. Solid- State Circuits,vol.44 no.2,pp.650-658.

[3] Chang L. (2008) 'An 8T-SRAM for variability tolerance and low voltage operation in high-performance caches', IEEE J. Solid-State Circuits, vol. 43,no.4, pp. 956-963.

[4] Jing Guo (2014), "A Novel Low Power and Highly Reliable Radiation Hardened Memory Cell for 65 CMOS Technology", IEEE Trans. Very Large Scale Integration (VLSI) Syst. vol.61,no.7,pp.1994-2001.

[5] Khayatzadeh. M, Lian. Y, (2014), 'Average-8T differential-Sensing sub-threshold SRAM with bit interleaving and 1k bits per bitline', IEEE Trans. Very Large Scale Integration (VLSI) syst., vol. 22, no. 5,pp. 971-982.

[6] Kolsoom Mehrabi (2015), "A Robust and Low Power 7TSRAM Cell Design", in proc. Symp.CAD, IEEE.

[7] Kyoman Kang (2015), "Full Swing Local Bitline SRAM Architecture Based on the 22-nm FINFET Technology for Low Voltage Operation", IEEE Trans. Very Large Scale Integration (VLSI) Syst. Pp. 1-9.

[8] Li .Q, Wang .B, Kim T.T, (2012), 'A 5.61 PJ, 16 kb 9T SRAM with single-ended equalized bit lines and fast local write-back for cell stability improvement', in Proc. Eur. Solid-State Device Res. Conf., pp. 201-204.

[9] Maisagalla Gopal (2013), "8T SRAM Cell Design for Dynamic and Leakage Power Reduction", IJCA, vol.71, no.9, pp.43-48.

[10] Maiz. J, Hareland. S, Zhang. K, Armstrong.P, (2003), Characterization of multi-bit soft error events in advanced SRAMs', in IEDM Tech. Dig., pp. 21.4.1-21.4.4.

[11] Mayuri Khapekar (2015), "power andTemperature Analysis of 12T CMOS SRAM Designed with Short Channel Devices", IOSR- JVSP, vol.5, issue 1, pp. 28-36.

[12] Shiny Grace.P (2016), "Design of 10T SRAM Cell for High SNM and Low Power", ICDCS, IEEE, pp. 281-285.

[13] Zhiyu Liu (2008), "Characterization of a Novel Nine-Transistor SRAM Cell", IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol.16,no.4, pp. 448-492.

[14] http://www.ptm.asu.edu