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Effect of W/L Ratio on SRAM Cell SNM for High-Speed Application

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Abstract - *As the scaling of CMOS technology, data stability of SRAM cell has become a major problem. In present, the demand of the low power VLSI circuit is on high. The SRAM cell static noise margin (SNM) has to be improved, to enhance the power performance. In respect to the future technologies, SRAM cell stability will be a primary concern in nanometer regime due to variability and decreasing power supply voltages. 6T-SRAM can be boosted for stability by deciding the cell layout, device threshold voltage, word line voltage, and the cell ratio. This paper analyzed the read and write stability by graphical method VTC. By varying the cell ratio as well as word line voltage, we keep observation on Read stability (RNM) and found a good variation in its stability at 45nm technology.*

***Key Words*: CMOS, Cell Ratio (CR), Pull-up Ratio (PR), SRAM, Static Noise Margin (SNM).**

1. INTRODUCTION

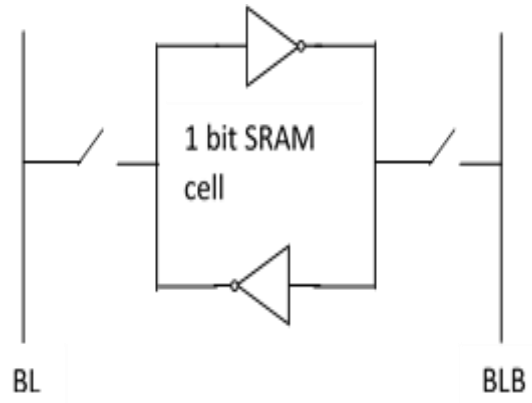
VLSI research market is the market which consistently moves towards growth in the direction of research. This is the broad variant field in which we can research at any level. As in the field of VLSI evolution of new technology, the technology and supply voltage continuously moderates and its impacts on the size of the circuit and delay or its performance which improves respectively. Day by Day the technology going towards diminishes and complexity increases. In present industry works on 32nm technology and in present research work on 14nm CMOS process is being used. As technology diminishes the speed of the circuit is increased. Static Random Access Memory (SRAM) is a category of semiconductor memory, to store one bit it uses bi-stable latching circuitry. In the area of multimedia applications, system on chip (SOC) and high-performance server processor, SRAM become an important component as a wide range of microelectronics applications. According to Gordon Moore's Law, the number of transistors per square inch on integrated circuits had doubled every year since their invention [1].

As with the evolution of new technology in which transistor scaling means a reduction of transistor size is reduced by the factor of 0.7 and due to this transistor scaling it takes improvement in the performance and cost of integrated circuits. As the growth of the device count per chips growth with the exponential due to this reason, the SRAM has frequently used in the integrated system. As the device count per chip, SRAM achieves high integration density steady with the reliability and performance required.

2. CONVENTIONAL 6T SRAM BIT – CELL

The Conventional SRAM (CV-SRAM) cell consist of six MOS transistors ('2'PMOS and '4'NMOS) as shown in fig.2 and in the memory bit cell of SRAM consist of back to back CMOS inverters are connected as shown in fig.1.1

Fig-1.1: Back to Back inverter latch circuit with access switches



2.1 The SRAM Bit-Cell

SRAM is a volatile semiconductor memory. The memory bit-cell have 6 MOS transistors M1, M2, M3, M4, M5, and M6. M5 and M6 are the pass transistor or access transistor which are controlled by a word line (WL) as shown in fig.1.2.

SRAM stores the bit in the form of voltage. SRAM stores the binary data one of two possible states either '0' or '1'. SRAM has 6 transistors so that's why it consumes more power with high chip area and therefore low density. SRAM speed is fast. SRAM has simple interfacing. SRAM does not need any periodic refresh operation, unlike DRAM. SRAM can operate at a lower supply voltage and it has a larger noise immunity due to larger Noise Margins.

Two basic requirements of SRAM cell are:

1. When the data read operation perform then the stored information in the SRAM should not destroy.

2. When the data write operation perform then the SRAM should allow to alteration in the stored information [2].

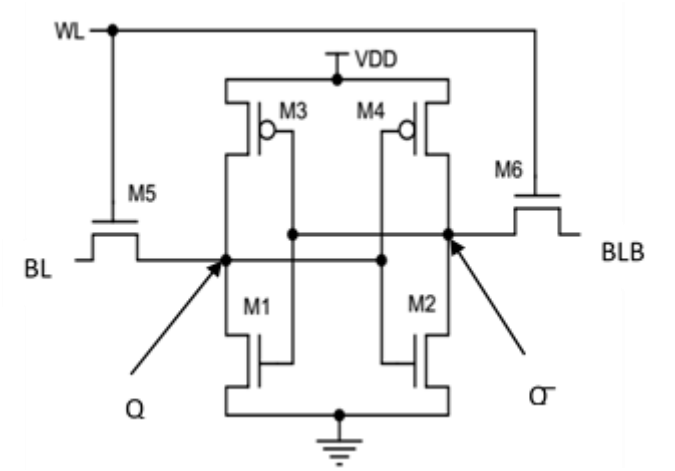


Fig-1.2: 6T- CMOS SRAM Bit-Cell

2.2 The Operation of SRAM Bit-Cell

There are mainly three states or three operations of SRAM memory cell, the Standby (Hold) Operation, Data Read Operation and Data Write Operation.

1. *Standby Operation (Hold):* In the hold operation the word line (WL) connected to the ground (WL=0) so then access transistors M5 and M6 are in cut-off mode or switch off and they disconnect the cell from bit lines (BL and BLB). Now 4 transistors are left M1, M2, M3, M4 and they formed two cross-coupled inverters and continue to reinforce to each other as long as they disconnected from the outsource. The current flows in this state from the supply voltage are known as standby current [3].

2. *Data Read Operation:* In the Read Operation the bit lines BL and BLB are precharged to VDD. And the word line also connected to the VDD after then the access transistors M5 and M6 are ON and as the memory stores previous information i.e. Q='0' and Qb='1' then the transistor M2 and M3 will be turned off and M4 and M1 will on and now the current will flow through BL-M5-M1 as shown in fig.2.1 and thus precharged BL will be discharged and BLB remains same. At last the voltage difference between BL and BLB will be detected by Sense Amplifier. So it means that the Read '0' Operation will be performed. And if the data stored Q='1' and Qb='0' then the transistor M1 and M4 will be turned off and M2 and M3 will be on and the current will flow through the BLB-M6-M2 as shown in fig 2.2 and thus precharged BLB will be discharged and BL remains same.in this way, the Read '1' Operation will occur [4].

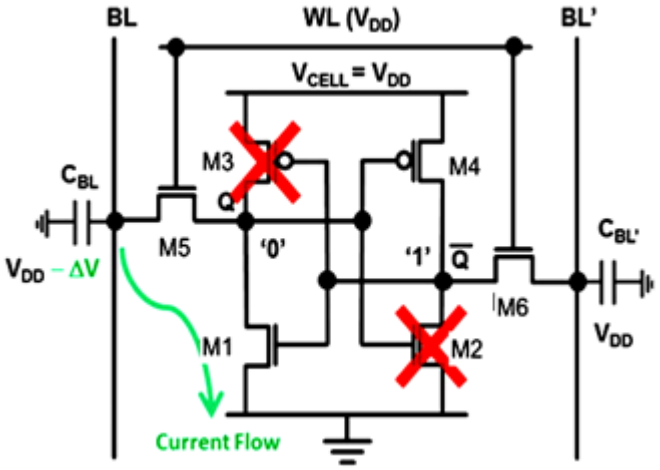


Fig-2.1: Current flow and the voltage level at each node during the read operation. The initial data stored in the SRAM cell is '0' (i.e., Q = 0).

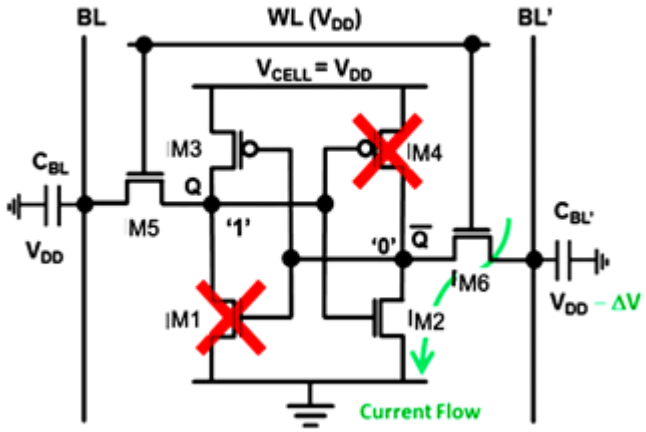


Fig-2.2: Current flow and the voltage level at each node during the read operation. The initial data stored in SRAM cell is '1' (i.e., Q = 1).

3. *Data Write Operation:* In the Write Operation BL and BLB are complementary to each other as BL='0' and BLB= '1'.

Write operation has been divided into 4 cases:

a. When '0' is stored and writing '0' is requested.
b. When '0' is stored and writing '1' is requested.
c. When '1' is stored and writing '0' is requested.
d. When '1' is stored and writing '1' is requested.

Case (a) and (d) are the insignificant cases in which same data write over the previously stored data so we cannot see any variation in these cases.

Now in case (b): When '0' is stored and writing '1' is requested. bit lines BL will be precharged and BLB will be driven from VDD to GND. And the Word Line should be high after then access transistor M5 and M6 are ON and as the memory stores previous information i.e. Q= '0' and $\overline{Q}$ ='1' then the transistor M2 and M3 will be turned off and M4 and M1 will be turned on and now the current will flow through BL-M5-M1 and M4-M6-BLB thus precharged BL will be discharged and BLB remains same. The voltage at node $\overline{Q}$ drops and the voltage at Q increases until the voltage level of $\overline{Q}$ will be low enough to turn on the transistor M3 and turn off M1 or the voltage level at node Q will be high enough to turn on transistor M2 and turn off the transistor M4 [4]. After then the voltage level of Q and $\overline{Q}$ will be flipped to VDD and GND respectively. As shown in fig.2.3.

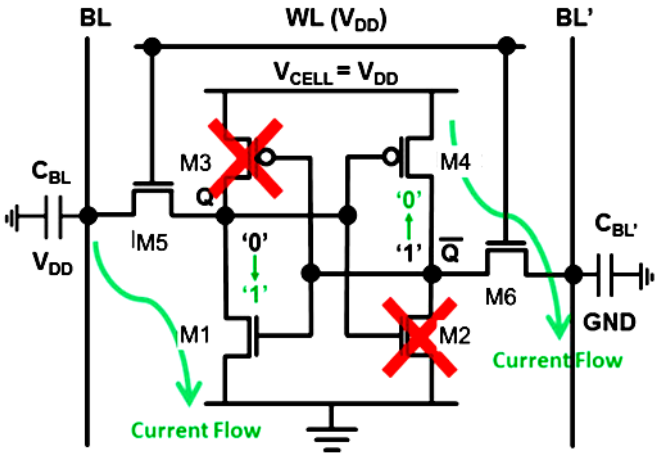


Fig-2.3: Current flow and the voltage level at each data storage node (i.e., Q and $\overline{Q}$) when writing '1' at the node Q are required. The initial data stored at the node Q was '0'.

Now in case (c): When '1' is stored and writing '0' is requested. Bit lines BLB will be precharged and BL will be driven from VDD to GND. And the word line should be high after then access transistor M5 and M6 are ON and as the memory stores previous information i.e. Q= '1' and $\overline{Q}$='0' then the transistor M1 and M4 will be turned off and M2 and M3 will be turned on and now the current will flow through M3-M5-BL and BLB-M6-M2 thus precharged BLB will be discharged and BL remains same. The voltage at node Q drops and the voltage at $\overline{Q}$ increases until the voltage level of Q will be low enough to turn on the transistor M4 and turn off M2 or the voltage level at node $\overline{Q}$ will be high enough to turn on transistor M3 and turn off the transistor M1. After then the voltage level of $\overline{Q}$ and Q will be flipped to VDD and GND respectively. As shown in fig 2.4.

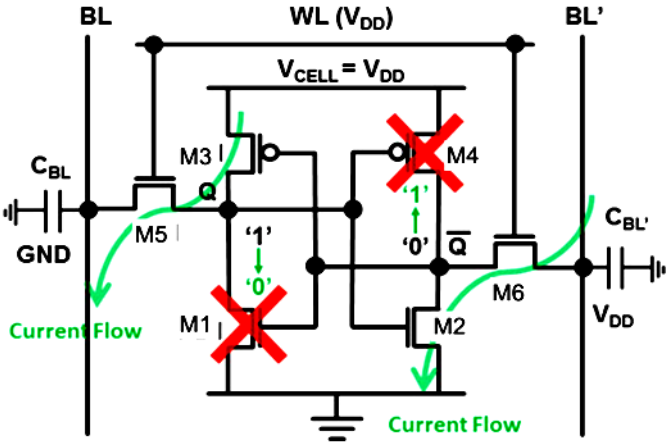


Fig-2.4: Current flow and the voltage level at each data storage node (i.e., Q and Qb) when writing '0' at the node Q are required. The initial data stored at the node Q was '1'.

3. STATIC NOISE MARGIN

Static Noise Margin, it shows the stability of SRAM circuit. To find the SNM we draw the inverter characteristic and its mirror characteristic and then we fix a possible maximum square in between the lobe of these two characteristics. In this graphical method, we plot the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and the inverse VTC^{-1} from Inverter 1(inv1) as shown in fig 3.2 [5].

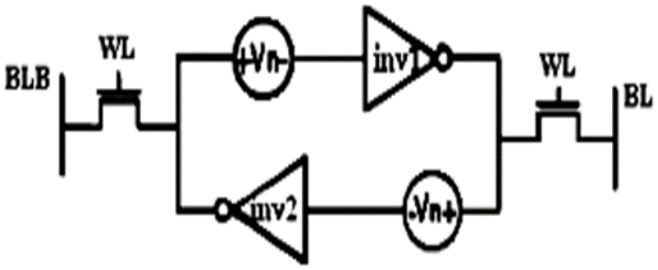


Fig-3.1: Standard Setup for SNM

The resulting two-lobed curve is called a "Butterfly Curve" and is used to determine the SNM. The SNM is defined as the length of the side of the largest square that can be trimmed inside the lobes of the butterfly curve as shown in fig 5. Static Noise Margin of the SRAM Cell depends on the various factors like Cell Ratio (CR), Pull-up Ratio (PR), Supply Voltage, Data Retention Voltage (DRV), Word Line Voltage (Vwl), Threshold Voltage (V_{th}). For the good stability of the SRAM cell must have Good SNM. For Good SNM we have to choose the desired value of the Cell Ratio (CR), Pull-up Ratio (PR), Supply Voltage, Data Retention Voltage (DRV), Word Line Voltage (Vwl), Threshold Voltage (V_{th}). Driver Transistor plays an important role in the SNM and it is approximately 70% depends on the Driver Transistor [6].

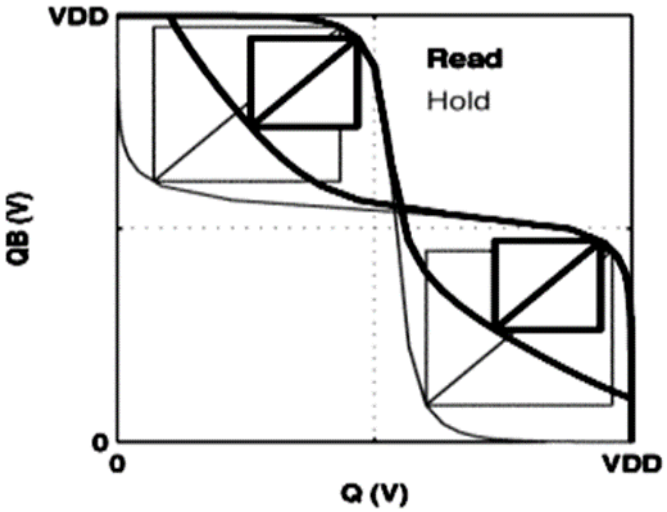


Fig-3.2: Butterfly curve for SNM

The ratio between the sizes of the driver transistor to the access transistor is called as Cell Ratio (CR). Similarly, the ratio of load transistor to the access transistor is called as Pull-up Ratio (PR).

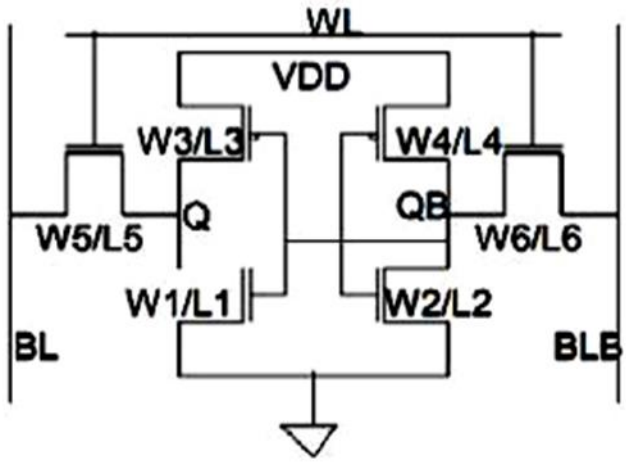


Fig-3.3: circuit for the basic SRAM Cell

CR= (W1/L1)/(W5/L5) = (W2/L2)/(W6/L6) (During Read Operation)

PR= (W3/L3)/(W5/L5) = (W4/L4)/(W6/L6) (During Write Operation)

Basically, there are three types of SNM during Standby mode, Read mode, Write mode which are Static Noise Margin (SNM), Read Static Noise Margin (RSNM) and Write Noise Margin (WNM) [7].

3.1 Read Static Noise Margin (RNM)

The cell is most susceptible when accessed during a read operation because it must hold its state in the presence of the bit line precharged voltage. If the cell is not deliberate properly, it may flip its state during a read cycle which results in either a wrong data being read or a destructive read where the cell flips state. Thus, the worst noise margin is obtained during read access. Figure 3.4 shows the equivalent circuit during a read operation.

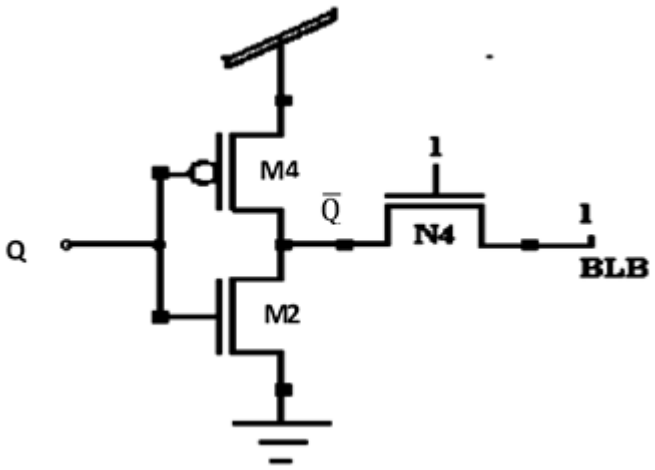


Fig-3.4: The equivalent circuit during read operation

For measuring the Read Static Noise Margin (RSNM) the biasing condition will be that both BL and BLB are precharged to VDD and Word Line is set to be high. Then the voltage at node Q is swept from 0 to VDD while calculating the voltage at node Qb . Then data will export from the tanner tool (W-Edit) and open it on the Excel sheet the draw a VTC of Qb vs. Q as shown in fig 3.5.

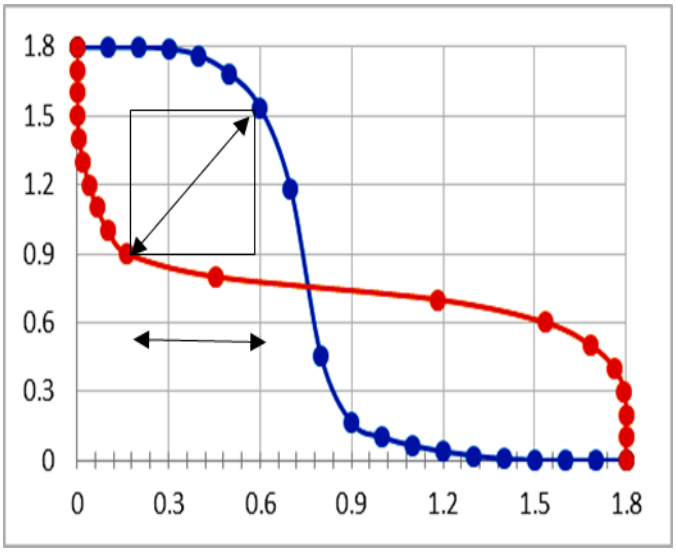


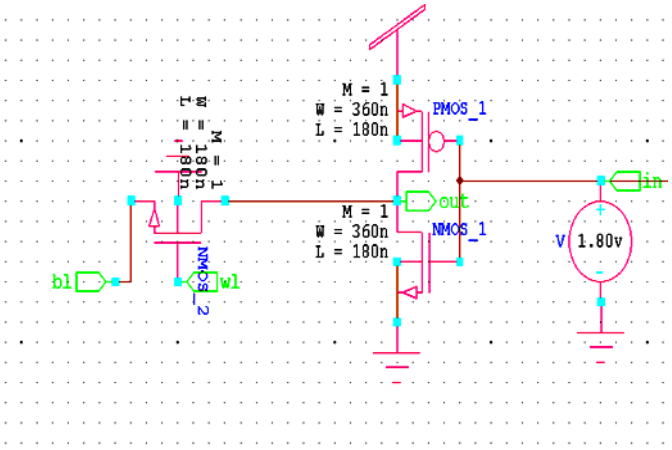
Fig-3.5: Read Static Voltage Transfer Characteristics Curve (RNM)

Read Margin is directly proportional to the cell ratio. The Cell Ratio should be satisfactorily large to ensure that such a read failure does not occur [8].

$$\frac{W1/L1}{W5/L5} \gg 1$$

3.2 Write Noise Margin (WNM)

The smallest square that can be embedded between the Read VTC and Write VTC that embedded square side will be WNM. We can find the Write Ability using two methods either VTC Curves or N-Curve [9]. Here we determined the Write Noise Margin from the VTC Curve. For measuring the Write Noise Margin (WNM), the biasing condition will be that both BL and BLB are precharged to VDD and the word line is set to be high. The biasing condition of WNM is identical to the biasing condition to the RSNM then the voltage at node Q is swept from 0 to VDD while calculating the voltage at node Qb this is to measure one of the two VTC Curves and this VTC will be Read VTC Curve as shown in fig.3.6. For other VTC Curve, the biasing condition will be that the bit line BL will be precharged and the bit line BLB will be connected to ground at the same time and then we measure the other VTC Curve and this VTC Curve will be



Write VTC Curve as shown in fig 3.8.

Fig-3.6: The equivalent circuit during Write operation (Read VTC)

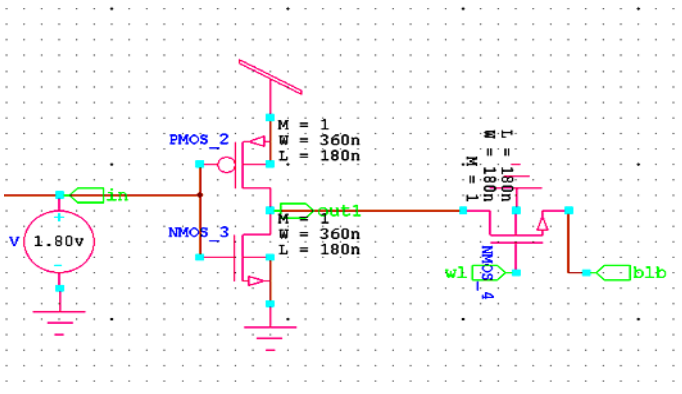


Fig-3.7: The equivalent circuit during Write operation (Write VTC).

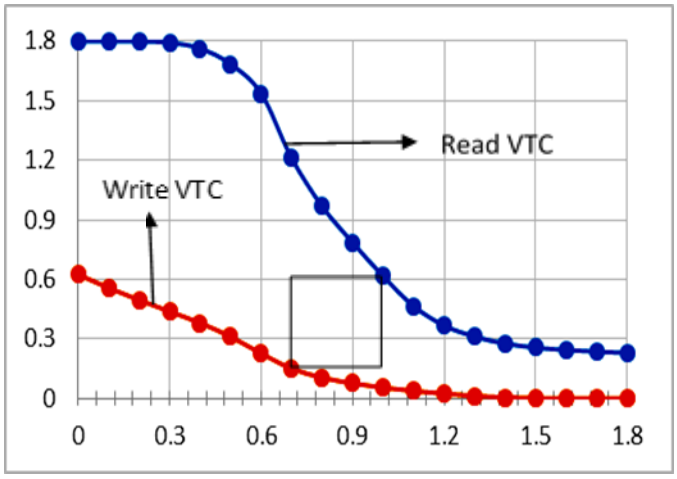


Fig-3.8: Write Noise Margin Voltage Transfer characteristic Curve (WNM)

The Write Ability depends on the Pull-Up Ratio as the Pull-up Ratio increases the write Noise Margin (WNM) also increases. And the effect of Pull-Up Ratio on to the Standby SNM and Read SNM does not affect or it may be a very less significantly effect. Pull-up Ratio does not greater than 1.8 to maintain the good write ability.

4. STATIC NOISE MARGIN

The results which observed from simulation using Tanner Tools v14.1
The Cell Ratio and Pull up Ratio of the SRAM Cell are given below:
CR= (W1/L1)/(W5/L5) = (W2/L2)/(W6/L6) (During Read Operation)
PR= (W3/L3)/(W5/L5) = (W4/L4)/(W6/L6) (During Write Operation).
Check the stability by varying the Cell Ratio 1-2 at Pull up Ratio=1 and Pull up Ratio 1-2 at Cell Ratio=1.

SNM Calculation: For measuring the SNM the length of the embedded square will equal to the SNM.
Side of the Embedded Square (S) = 0.400V = 400mV
Length of Diagonal of Embedded Square (D) =
$\sqrt{2}$*one side of the embedded square=$\sqrt{2}$*400m
SNM = D/($\sqrt{2}$) = ($\sqrt{2}$×400m)/($\sqrt{2}$), so SNM = one side of the embedded square (S).

Now, we are keeping eyes on the stability of the SRAM Cell by varying the Cell Ratio. As we have analyzed by the previous papers that by increasing the Cell Ratio the SNM also increases. The value of the Cell Ratio is increasing by increasing the ratio of the size of the driver transistor to access transistor. As Cell Ratio increases the speed of the circuit is also increases and the size of the circuit is also increased. This is the drawback but our major concern is on system's stability. Check the variations of Cell Ratio on Standby SNM as shown in table 1.

Check the variation of cell ratio on the hold stability and here we can see that as cell ratio increases the hold snm also increases. As cell ratio increases from 1.0 - 2.0 the hold snm increases nearly about ~12.93% so this is good with respect to the system stability.

Table -1 CR vs SNM

Technology(nm)	CR	SNM(mV)
45nm	1.0	232
	1.2	240
	1.4	249
	1.6	250
	1.8	258
	2.0	262

Now, check the variations of Cell Ratio on Read Stability (RSNM) and here we can see that as Cell Ratio increases the Read Stability also increases. As Cell Ratio increases from 1.0 - 2.0 the Read Stability increases nearly about ~101.47% so this is the good sign in respect of stability.

Table-2 CR vs RSNM

Technology(nm)	CR	RSNM(mV)
45nm	1.0	68
	1.2	90
	1.4	100
	1.6	112
	1.8	122
	2.0	137

As previous we have checked the variation of Cell Ratio on Read Stability (RSNM). Now, we check the variation of Word Line Voltage with Variation of Cell Ratio on Read Stability. As Word Line Voltage decreases the Read Stability also increases [12]. As Cell Ratio increases from 1.0 - 2.0 and the word line voltage decreases from 1.8v - 1v. At CR= 1 and the Vwl=1.8 and Vwl=1.

The increment in the stability is about ~194.11% at CR=1 and the Vwl=1.0 and .6 and the increment in the stability is about ~60.58% at CR=2 and the Vwl= 1 and Vwl = .6 and this is very good sign in respect of stability [13].

Table-3 CR,Vwl vs RSNM

Vwl → / CR ↓	1.0	.9	.8	.7	.6
1.0	68	100	140	172	200
1.2	90	101	140	173	205
1.4	100	121	150	176	205
1.6	112	140	165	185	215
1.8	122	150	179	189	215
2.0	137	150	180	200	**220**

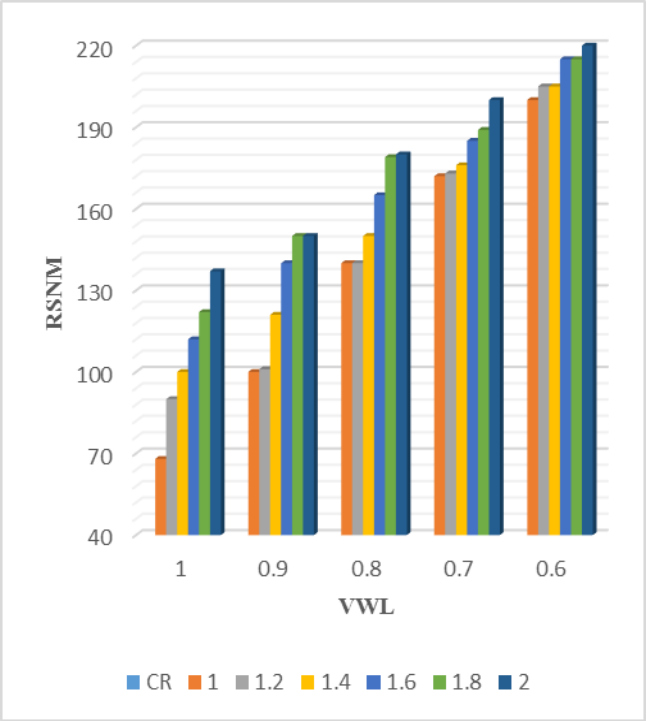


Chart-1: Variation on RSNM by varying CR and Vwl simultaneously.

5. Conclusion

In the High-Speed CMOS VLSI Design major issue is the Stability. We work on the reliability of SRAM circuits and systems. SNM, RSNM, WNM, V_{th}, V_{wl} these parameters are taken into account of SRAM Cell. In different types of analysis are directly proportional to the size of the SRAM Array Design but these parameters Vwl and V_{th} this increases the stability does not any effect on the size of the SRAM Array Design even they increases the stability of the SRAM Cell. So finally stability improves which is our major concern.

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