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Review on Modified Gate Diffusion Input Technique

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Abstract - *This paper gives an overview upon MGDI technique, in which low number of transistors are used that reduce the power consumptions and area on chip of digital circuits. In this paper full adder is introduced using MGDI technique. 2 bit comparator, full subtractor were introduced using GDI technique. Then these digital circuits were compared with traditional CMOS transistors in terms of power dissipation, number of transistors, area, speed and delay.*

Key Words: **Gate diffusion input, Modified gate diffusion input, full adder, 2 bit comparator, full subtractor, power consumption and area, delay.**

1. INTRODUCTION

In modern time, three factors- areas, speed and power consumptions are essential for increasing demand of low power and small size in handheld devices like cellular phone, laptop, palmtop, wireless modems and electronic devices etc. In past years, VLSI designers were interested with parameters such as area, speed, reliability and cost. In recent years, power consumption is being set equivalent importance. It has been proven that an increase of 10°c in the working temperature of an electronic device causes a 100% increase in the failure rate [5]. So the number of transistors used in electronic devices must be least as possible to dissipate less power and area.

A. Morgenshtein described new design GDI cell that allows reducing delay, area and power dissipation [2], [3]. GDI cell consists of 3 inputs – G (common gate input of PMOS and NMOS). P (input to drain/source of PMOS). N (input to drain/source of NMOS).

P. Balasubramanian and J. John described MGDI cell that overcomes the drawbacks of GDI-cell. It extremely akin to GDI cell but the difference is that the bulk of both NMOS and PMOS are constantly fixed to GND and V_{DD}, respectively [4], [9].

Using traditional CMOS technology digital circuits occupy large area and number of transistor count that increase power dissipation [1], [6], [7]. But using MGDI technology, area and power consumptions are reduced.

The current paper is organized into 5 sections. Section 1 gives introduction. Section 2 gives description of GDI technique. Section 3 gives description of MGDI technique. Section 4 gives brief literature survey. Finally, the paper is concluded with section 5.

2. GDI TECHNIQUE

In first look GDI cell similar to CMOS inverter but GDI cell consists of 3 inputs – G (common gate input of PMOS and NMOS), P (input to drain/source of PMOS) and N (input to drain/source of NMOS).Bulks of both PMOS and NMOS are attached to their diffusion P, N to reduce bulk effect. GDI cell is shown in fig-1[3].

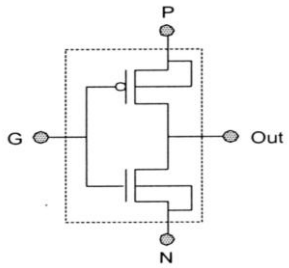

Fig-1: Basic GDI cell

GDI decreases both gate leakage current and sub threshold leakage current as compared to traditional CMOS. But its performance depreciates when used in and below 90nm technology. Fabrication of basic GDI cell is not possible in traditional p well progression. When substrate attached to drain, threshold voltage is increased and when the substrate is attached to source, body effect is destroyed in below equations [6].

$$V_{th} = V_{tho} + \gamma\left(\sqrt{|2\emptyset_F + V_{SB}|} - \sqrt{|2\emptyset_F|}\right) - \eta V_{DS} \quad (1)$$

'V_{th}' stands for threshold voltage, V_{SB} stands for source body voltage, 'V_{tho}' stands for zero bias threshold voltage, 'γ' stands for substrate bias coefficient, 'Φ_F' is fermi potential, 'V_{SB}' Source to substrate voltage, 'V_{DS} 'drain to source voltage and 'η' is drain induced barrier lowering (DIBL) coefficient [2].

3. MODIFIED GATE DIFFUSION INPUT TECHNIQUE (MGDI)

MGDI is a new technique for designing low power digital circuits. This technique is adopted from GDI technique. MGDI technique is used to reduce power dissipation, transistor count and area of digital circuits. MGDI also consists of three input terminals - G, (input of both PMOS and NMOS) P, (input to drain/source of PMOS) and N (input to drain /source of NMOS) except the bulks of PMOS (S_P) and NMOS (S_N) are constantly coupled to V_{DD} and GND, respectively [5].

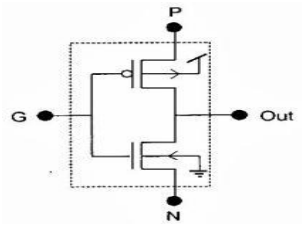

Fig-2: Basic MGDI cell

MGDI overcomes the drawbacks of GDI cell. With technology scaling, the influence of source body voltage on transistor threshold voltage gets exceeding abridged i.e. the linearized body coefficient 'γ' in below equation. Make MGDI pertinent in 65 nm technology and below [8].

On varying the values of G, P, N, S_P and S_N in MGDI cell, S_P and S_N will remain constantly coupled to V_{DD} and GND various functions are obtained, shown in the following table [5].

Table -1: Miscellaneous functions using MGI cell

G	P	N	S_P	S_N	OUTPUT	FUNCTION
A	V_{DD}	0	V_{DD}	0	A'	INVERTER
B	0	A	V_{DD}	0	A.B	AND
A	B	V_{DD}	V_{DD}	0	A+B	OR
B	A	A'	V_{DD}	0	A'B+AB'	EX-OR
B	A'	A	V_{DD}	0	AB+A'B'	EX-NOR
S	A	B	V_{DD}	0	AS'+BS	2:1 MUX

From table-1 it is noticed that different logic styles can be designed using one MGDI cell. OR gate and AND gate is designed using two transistors only, while in conventional CMOS it requires 6 transistors. The main advantage of MGDI technique is that it reduces transistor counts and area on chip that's cause of low power consumptions. So it is easy to design complex circuits using MGDI technique.

4. LITERATURE SURVEY

4.1 Full adder using MGDI cells

In the paper [6] full adder is implemented using MGDI cell. Full adder is a combinational circuit that has three inputs bits augend bit (A), addend bit (B) and carry bit (C_{IN}) from previous stage and two outputs sum(S) and carry out (C_{OUT}). Truth table of full adder is shown in table-2.

Table-2: Truth table of full adder

A	B	C_{IN}	Sum	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean expressions for Full adder are following [1]:

$$S = A \oplus B \oplus C_{IN} \quad (2)$$

$$C_{OUT} = AB + C_{IN}(A \oplus B) \quad (3)$$

Now using MGDI cell full subtractor is designed. Logic circuit and schematic of designed full subtractor is shown below in fig-7.

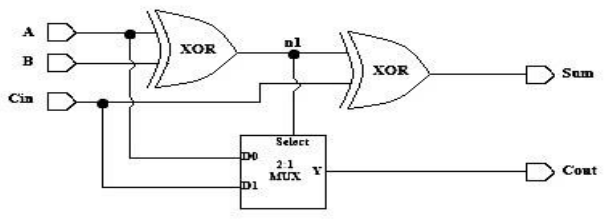

Fig-3: logic circuit of full adder

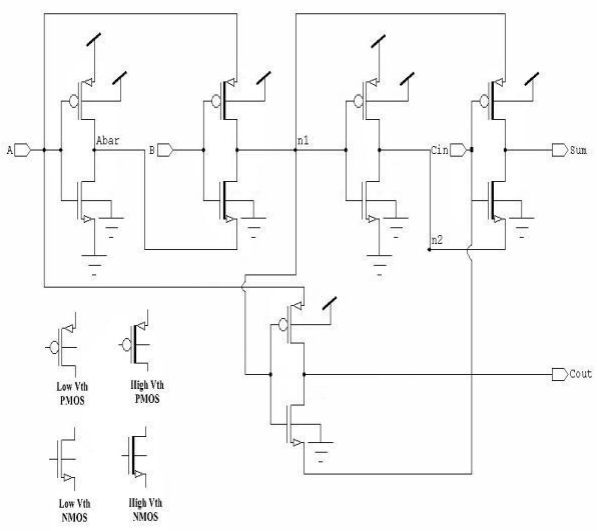

Fig- 4: Schematic diagram of 1 bit full adder

The present work proposes the design of a full adder using modified Gate Diffusion Input (MGDI) and Mixed Threshold Voltage (MVT) scheme. The current work has been conceded in 45nm technology using HSPICE whereas the layout has been designed in Microwind. Evaluations with traditional CMOS transistors, transmission gate and CPL disclosed a decrease of 82.76%, 54.54% and 73.68% in number of transistors exploited, 93.33%, 72.79% and 86.39% in surface area, 54.18%, 58.37% and 52.44% in average power consumption, 62.27%, 49.08% and 79.85% in peak power consumption, 89.73%, 89.75% and 93.15% in delay time while a magnanimous 95.29%, 95.73% and 96.74% in power delay product, respectively. Plus, a vital decline of 99.52%, 99.56% and 99.78% in energy delay product is gained compared to a full adder realized embracing the popular CMOS logic, transmission gates as well CPL, successively [6].

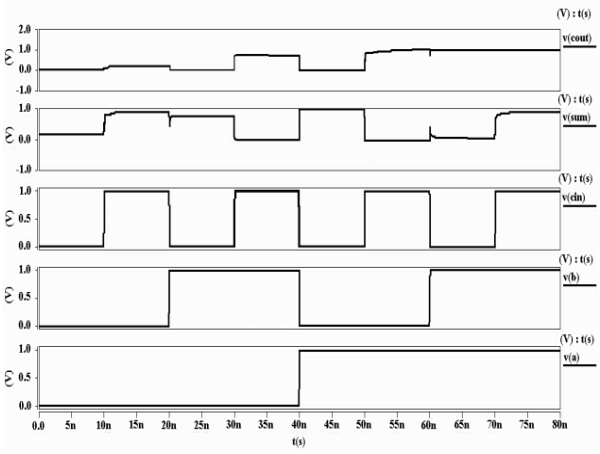

Fig-5: Waveform of 1 bit full adder using MGDI cell

4.2 bit comparator using GDI cells

In paper [7] the magnitude comparator is a fundamental arithmetic component of digital system. A magnitude comparator is used in Digital Signal Processors (DSP) for data processing, microprocessor for decoding instruction and microcontroller for controlling temperature of furnace in industry. Comparator is a combinational circuit, N bit comparator compares two N bit binary numbers A and B. The block diagram of N bit comparator is follows in fig- 6. It generates three outputs that is denoted by A=B (F_1), A<B (F_2), A>B (F_3).

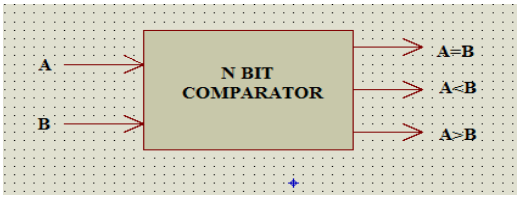

Fig-6: Block diagram of 2 bit comparator

Table-3 Truth table of 2 bit comparator

A_1	A_0	B_1	B_0	A=B(F1)	A<B(F2)	A>B(F3)
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

To determine whether A is greater than B or vice versa and then firstly check the most significant bit If most significant bit of both inputs is different, e.g. suppose most significant of A is 1 and most significant bit of B is 0 then A> B, if condition is reverse then A <B. If most significant bit of both the input is equal then go for next bit and then compare the next bit of both the input If both the inputs are same then A= B.The Boolean expressions for 2 bit comparator are following [7].

$$A = B \;:= (\overline{A_1}.\overline{B_1} + A_1B_1) + (\overline{A_0}.\overline{B_0} + A_0B_0) \quad (4)$$

$$A < B \;:= \overline{A_1}.B_1 + \overline{A_0}.B_0.(\overline{A_1}.\overline{B_1} + A_1B_1) \quad (5)$$

$$A > B \;:= A_1\overline{B_1} + A_0.\overline{B_0}.(\overline{A_1}.\overline{B_1} + A_1B_1) \quad (6)$$

Now using GDI cell 2 bit comparator is designed. Schematic of designed 2 bit comparator is shown below in fig-7.

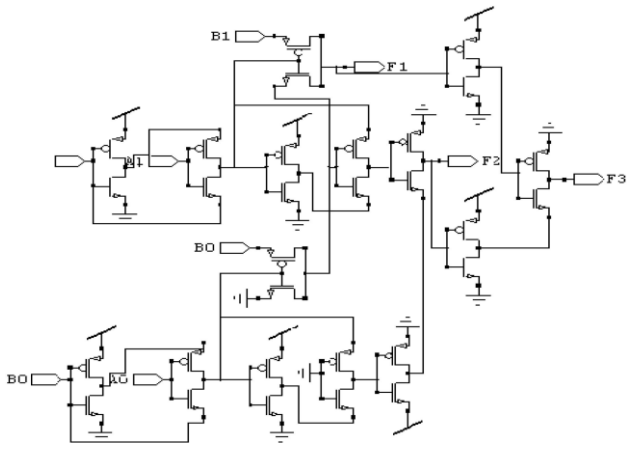

Fig-7: Schematic of 2 bit comparator using GDI cell

The performance of the proposed GDI magnitude comparator circuit with help of full adder logic has shown good performance in compare to existing conventional CMOS based design. The comparative performance of conventional CMOS and proposed GDI magnitude comparator with respect to power consumption at different range of input voltage, temperature and frequency has been discussed in the paper [7].

4.3 Full subtractor using GDI cell

In the paper [8] full subtractor is implemented using GDI cell. Full subtractor is a combinational circuit that has three inputs U (minuend), V (subtrahend), W (borrow from previous stage) and two outputs, one is D (difference) and another is B (Borrow).Truth table of full subtractor is shown below.

Table-4 Truth table of full subtractor

X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The Boolean expressions for Full subtractor are following [7]:

$$D = X \oplus Y \oplus Z \quad (7)$$

$$B = Z.(\overline{X \oplus Y}) + \bar{X}.Y \quad (8)$$

Now using GDI cell full subtractor is designed. Logic circuit and Schematic of full subtractor is shown below in fig-7 and fig-8.

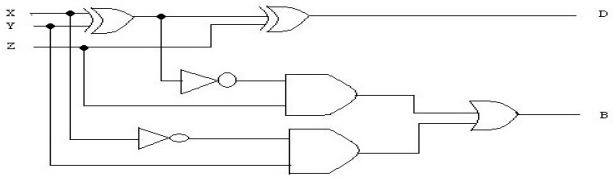

Fig-8: logic circuit of full subtractor

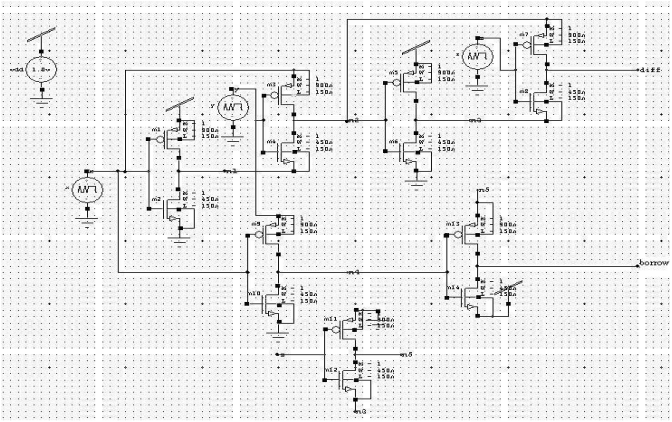

Fig-9: Schematic of full subtractor using GDI cell

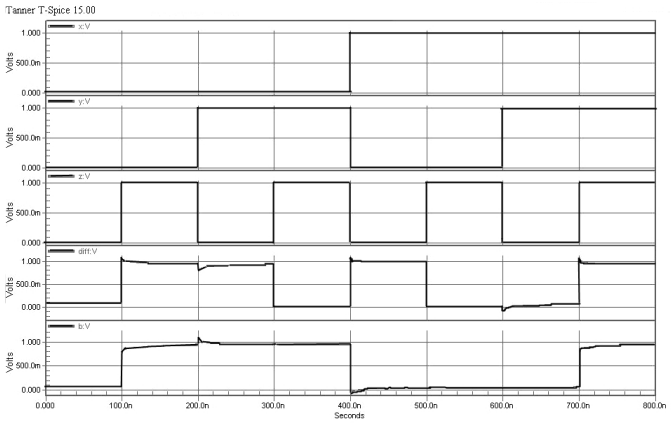

Fig-10: Waveform of 1 bit full subtractor using GDI cell

The proposed design [8] of a full subtractor using Gate Diffusion Input (GDI) procedure which on simulation has been found to consume low power in conjunction with lesser delay time and fewer transistors while maintaining proper output-voltage swing. The present work has been performed in 150nm technology using Tanner SPICE and the layout has been concocted in Microwind. Comparisons with standard CMOS, transmission gate and CPL techniques showed a reduction of 72.00%, 63.16% and 58.82% in terms of transistor count, 99.68%, 88.78% and 99.99% in terms of average power consumption, 4.85%, 84.39% and 85.68% in terms of delay time and a significant 99.95%, 98.25 % and 99.99% in terms of power delay product, respectively [8].

Furthermore, a depreciation of 97.24%, 92.42% together with 95.10% in surface area is reaped when judged against a full subtractor composed adopting the popular CMOS approach, transmission gates and CPL, proportionately [8].

CONCLUSIONS

This paper work introduces the MGDI technique and implementation of various digital circuits using GDI technique and MGDI technique. Simulation is done in Comparison between conventional CMOS, GDI and MGDI technique is shown in the case of area, transistor count and static power consumptions. Using MGDI technique, implemented logic gates and digital circuits reduced to 25% - 90% in number of transistors and due to this area on chip decreases as well as significant reduction in power consumptions. Using MGDI technique various digital circuits can implement to increase efficiency of digital circuits.

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