International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 03 | Mar -2017 www.irjet.net p-ISSN: 2395-0072

Delay Optimized Full Adder Design for High Speed VLSI Applications

Tincy Charles[1] , Mohammed Salih K K[2]

[1] Mtech Scholar, Department of ECE, GECI, Kerala, India
[2] Assistant Professor, Department of ECE, GECI, Kerala, India

---

Abstract - *The most widely used arithmetic operation in digital applications is addition. Full adder is the most important building block in digital signal processors and controllers as it is used in arithmetic logic circuit(ALU) , in the floating point unit and in case of cache or memory access address generation. As density of IC chip increases, power consumption also increases. Hence low power designs is the primary requirement in the VLSI field. Reducing delay of a digital circuit is an important topic in logic design for efficient implementation of adder. In this paper a hybrid CMOS full adder circuit designed using both transmission gate and complementary metal oxide semiconductor(CMOS) is implemented and a modified version of this full adder is proposed. Design was implemented using Cadence Virtuoso Tools in 180nm and 90nm technology. Then comparison is done against these full adders in terms of power, speed and power delay product.*

Key Words: CMOS,TG, Power Delay Product

1.INTRODUCTION

Adders are one of the major components in digital systems, as they are widely used in basic digital operations such as division, multiplication and subtraction.As addition forms the basis of many binary operations, adder circuits are of great interest in digital design. Deep submicron CMOS technologies are used to explain the challenging criteria of the emerging high-speed and low-power communication IC chips. Analyzing any digital system, we can see addition is a basic operation.

A heuristic approach, known as hybrid adder models is proposed to save power at low transistor sizes.A wide variety of adder circuits have been proposed in literature, with the purpose to fulfill the various area, power and speeds requirements of implementations[3]. Designers move their attention to design an efficient full-adder, which operates with the minimum power consumption and high speed. Power dissipation depends upon the switching activity, wire capacitances, node capacitances and control circuit size.

Full adders can be classified into static and dynamic full adders. Static full adders are reliable, require less power but on the cost of area[2]. While dynamic full adders have high speed operation, high driving capability, low power, low input capacitance and but power dissipation due to higher switching activities and they require N+2 transistors for N input logic function instead of 2N transistors required by standard adder as they use only NMOS transistors and due to absence of PMOS input capacitance is lower but dynamic full adder suffer from complexity, charge sharing and high power requirement due to high switching so a hybrid logic style will embed the both static and dynamic full adder to get better results.

2. REVIEW OF VARIOUS LOGIC STYLES

Static CMOS logic style is known for its better power efficiency,high noise margin,no static power dissipation.It is more robust for transistor sizing and voltage scaling[4].The disadvantages include higher delay and large capacitance[3].Various static logic styles include Pseudo-NMOS logic,Transmission logic,Pass Transistor logic etc.

Pseudo-NMOS logic style adder replace the pull-up block with single PMOS transistor thus reducing the number of gates. Thus it reduces the capacitance and improves the speed. The Rand asymmetrical noise margin.Transmission-Gate(TG) Full Adder uses XOR gate.It acts as a high-quality switch with low capacitance and resistance[5],[6].It is one of the members of the ratio less logic family as the DC characteristics are independent of the input levels.

Complementary Pass Transistor Logic (CPL) adder implements logic functions with NMOS-only.Its advantages include differential inputs/outputs,circuit modularity and simplicity[7]. It can be efficiently realized with small number of transistors. The disadvantages of CPL is reduced higher static power consumption and noise margin. Double Pass Transistor Logic (DPL) adder is a modified version of CPL that is suitable for low-voltage application[7].DPL has balanced input capacitances, therefore reducing the dependence of the delay on the input data. DPL also provides full logic swing due to the use of PMOS gates as well as NMOS, and the dual current driving ability of DPL compensates for the additional PMOS gates [5]. The disadvantages of DPL is

the higher number of transistors, hence higher area and higher power dissipation.

Dynamic Logic Style uses a sequence of evaluation and precharging phases to realize complex logic functions in a single PMOS pull-up network or NMOS pull-down , hence this requires less transistors and also has no static power consumption. The reduced overall capacitance results in significantly improvement in the speed. The disadvantages of dynamic logic is the high dynamic power dissipation due to clock switching. The dynamic logic has clock skew and charge-sharing problems. Various dynamic logic style include NP-CMOS,Domino and True Single-Phase Clocked Logic (TSPCL). The C2MOS latched NP-CMOS (also called NORA-CMOS) can be used in the effective implementation of pipelined circuits.

3. EXISTING FULL ADDER IMPLEMENTATION

The full adder schematic is divided into three modules. Module 1 and module 2 represent the XNOR module and Module 3 represents the transmission gate module which produces C_{out} signal [1].

The XNOR module with 6 transistors is designed to minimize the power with avoiding voltage degradation possibility. The power consumption is reduced by the use of weak inverter (small channel width transistors) formed by transistors Mp1 and Mn1. The level restoring transistors Mp3 and Mn3 is responsible for full swing of the levels of output signals.The circuit diagram for the full adder is shown in fig:1.

The output carry signal is implemented by the transistors Mp7,Mp8,Mn7 and Mn8. The input carry signal (C) reduces the overall carry propagation path significantly by propagating only through a single transmission gate (Mn7 and Mp7). The use of strong transmission gates (large channel width transistors Mn7, Mp7, Mn8, and Mp8) guaranteed further reduction in propagation delay of the carry signal.

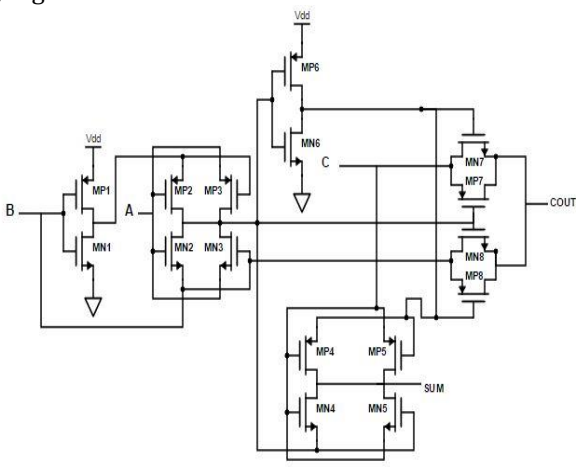

Fig-1: Circuit diagram of full adder[1]

The inverter formed by transistors Mp1 and Mn1 generate B'. This is used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. This suffers from some voltage degradation problem, and this can be removed using two pass transistors Mp3 and Mn3.PMOS transistors (Mp4, Mp5, and Mp6) and NMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module which implement the SUM. Analyzing the full adder truth table, the condition for Cout generation has been deducted as follows:

If A = B, then Cout = B; else Cout = C

4. PROPOSED FULL ADDER

The proposed full adder circuit consist of only 14 transistors and is represented by three modules. Here the transistors are reduced from 16 in the existing design to 14 transistors.The block diagram of the proposed full adder circuit is shown in fig:2. Module 1 represents fully restored CMOS XOR-XNOR cell and module 2 represent XOR module which generate SUM signal. Module 3 represent TG module which generate Cout signal.

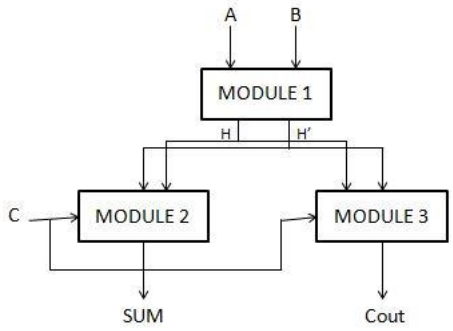

Fig-2: Block Diagram of Modified Full Adder

The schematic of proposed full adder is shown in fig:3.Module 1 is based on the cross coupled PMOS structure, but it also uses the cross coupled NMOS structure to produce the complement. These structures do not provide an output for A = B = 0 and A = B = 1, respectively, which instead is provided by the feedback MOSFETs (Mn1 and Mp3). The feedback also eliminates the threshold voltage loss associated with the structure[10-11].

Only six transistors are needed to realize this circuit and the use of inverter is eliminated. The feedback will lower the maximal operating frequency and require the MOSFETs to be ratioed when compared with the other XOR gates. To properly ratio the MOSFETs, the design effort increases. The threshold voltage drop is completely eliminated from both the outputs ,due to the regenerative feedback introduced by the pull-down (nMOS) and the pull-up (PMOS) transistors, thereby providing the full voltage swing.The operation of the above circuit must be restricted to supply voltages above

$2|V_{tp}|$.The sizing of the feedback transistors must be carefully done for proper functioning of the circuit under various operating conditions.

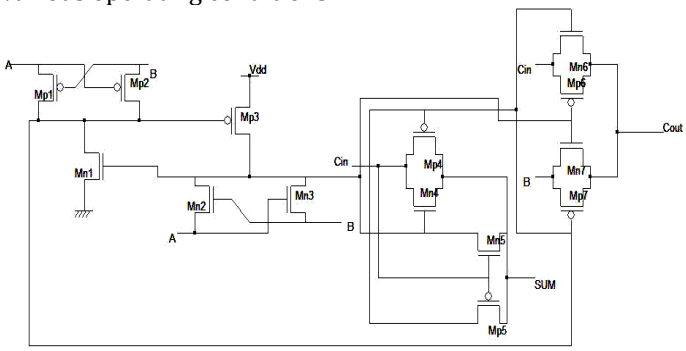

Fig-3: Schematic of Proposed Full Adder

The SUM module is designed to minimize the power to best possible extend.This module is the transmission function implementation of XOR gate.The inputs to this module are driven by the outputs of first module(H and H').The speciality of this design is its lowest average power consumption since it does not use any power or ground rails ie, absence of short circuit current.But the drawback is that the SUM signals are not capable to drive bigger loads.They have outstanding power delay product.

The third module is implemented using transmission gate logic as in fig:1[4].This is basically a multiplexer which passes either A(or B) or C, according to the value of H.The input signals A and C provides the driving power for Cout signal, since either of inputs will pass.This design is normally used where a latch or buffer follows the output of adder cell to avoid lacking power of Cout signal.

5. SIMULATION RESULTS

The full adder design in fig:1 was implemented in 180nm and 90nm by using Cadence Virtuoso software.Then the transient analysis is obtained as in fig:8.

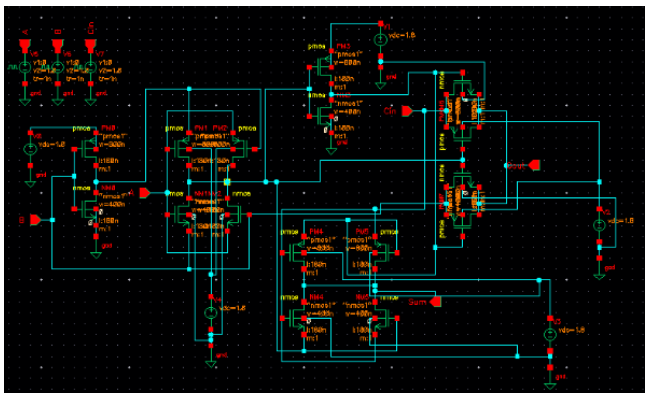

Fig-4: Implementation of Full Adder

The power consumption of hybrid full adders can be classified into static power consumption and dynamic power consumption. Static power consumption is caused from leakage and biasing currents[5-7] in most of CMOS based circuit implementations. Mostly this is lower that the dynamic power consumption. Dynamic power consumption arises because of charging and discharging of load capacitances.For 180-nm technology,circuit operated at 1.8V the total power consumption was found to be 7.598µW and for 90-nm technology,it was found to be 2.861µW.

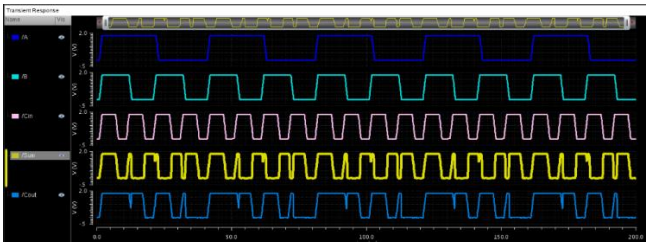

Fig-5: Transient Analysis of Full Adder

The delay was found to be 27.99ps for 180nm and 3.232ps for 90nm technology.The four bit and eight bit extension of full adder as shown in fig:6 and fig:8 were also implemented and power and delay are compared.

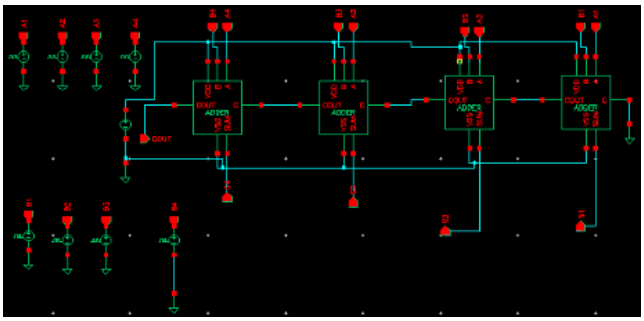

Fig-6: 4-Bit Extension of Full Adder

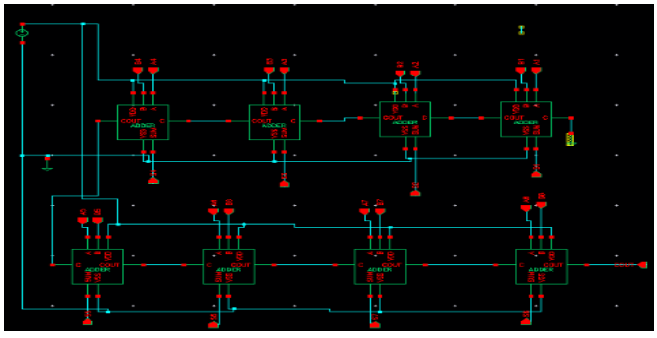

Fig-7: 8-Bit Extension of Full Adder

The modified full adder is implemented in fig:8.It is found that the average power consumption was found to be 9.058µW in 180-nm technology.This reduction in power consumption is mainly due to absence of leakage

currents.The delay was reduced significantly to 8.438ps due to the incorporation of fully restored swing logic.The simulation results were compared in Table:1.

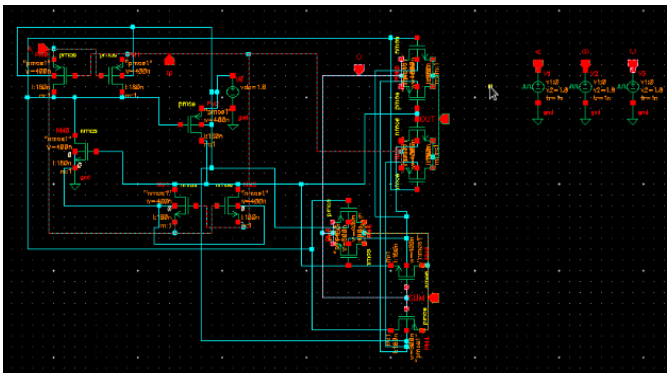

Fig-8: Implementation of Proposed Full Adder

Table -1: Comparison Results of Full Adders

Designs	Average Power(µW)	Delay(ps)	Power Delay Product(fJ)
Existing180nm full adder	7.598	27.99	0.2126
Existing 90nm full adder	2.861	3.232	0.0092
4-bit adder	25.92	11.37	0.2947
8-bit adder	53.95	11.37	0.6134
Proposed full adder	9.058	8.438	0.0764

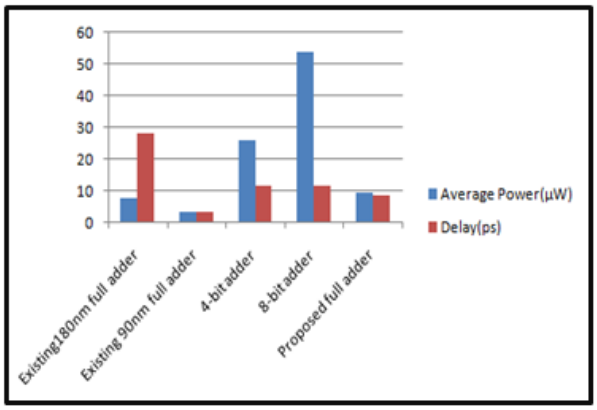

Chart -1: Bar Diagram Representation of Simulation Results

6.CONCLUSION

In this paper, a hybrid full adder is implemented in 180nm and 90nm.Both the existing and proposed designs were simulated using Cadence Virtuoso tools.It is found that the propogation delay is reduced by the use of strong transmission gates(long channel width transistors) and by incorporation of fully restored swing logic and is found to be 8.438ps.The PDP of both designs are measured and it is observed to be minimum in the case of the proposed design. The area of the proposed design is also reduced when compared in terms of transistors against the existing architecture.

REFERENCES

[1] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit", *IEEE Trans. Very Large Scale Integr. (VLSI)* Oct.2015, Volume: 23, Is- sue:10

[2] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," *in Proc. Int. Symp. Circuits Syst.*, May 2003, pp. 317–320.

[3] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low- power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[4] M. L. Aranda, R. B´aez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," *in Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE)*, Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.

[5] P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," *in Proc. World Congr. Inf. Commun. Technol. (WICT)*, Dec. 2011, pp. 240–244.

[6] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Gol- makani, "Design of new full adder cell using hybrid-CMOS logic style," *in Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2011, pp. 451–454.

[7] I. Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.

[8] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-m full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

[9] S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder circuit," in Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUiCONE), Dec. 2011, pp. 1–7.

[10] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEE Proc.-Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[11] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 1999, pp. 713–722.