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REVIEW ON OPTIMIZED AREA,DELAY AND POWER EFFICIENT CARRY SELECT ADDER USING NAND GATE

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Abstract - *In the modern digital life the increased important role of digital design invites new challenges of digital media. In the electronic field, carry select adder is one of the fastest adder used in microprocessor and digital signal processing to perform fast airthmatic operation. The structure of carry select adder require more area because its internal structure consist of two ripple carry adder (RCA) and multiplexer. The conventional carry select adder and binary to excess-1 convertor to require more area, power and redundant logic. In this proposed work significantly reduce area, power and redundant logic operation present in conventional carry select adder. The new logic formulation technique using NAND gate optimize area, it obvious to reduce the power consumption is most important area of research in VLSI design. In practice, this is advantageous since NAND gate chip are particularly easy to make and are very cheap. The NAND gate has lesser delay than NOR and it is easier to fabricate. The NAND gate have better power performance.*

Key Words: Adder, arithmetic unit, low-power design, universal gates, redundant logic, Binary to Excess-1 converter.

1.INTRODUCTION

In digital electronic, the carry select adder are most widely used in digital system and play a important role of heart for many computational circuit and other complex circuit, based on addition .it is most widely used in many data processor to perform one of the speedest adder and main component of airthmatic unit. the design of digital adder optimize area, delay and reduce the power consumption is most important area of research in VLSI system design. The low-power, high performance and area efficient VLSI system design most widely using in mobile device, multi standard and wireless receiver, biomedical instrumentation, satellite and mobile phone etc. The ripple carry adder used a simple design structure. It is connected in parallel to N number of bit. Which allow to fast design but carry propagation delay is more. carry look ahead adder is fast adder used in digital logic. Carry look ahead adder solve the problem of ripple carry adder it reduce the carry propagation delay and improve the speed but the carry look block are very complicated. A conventional carry select adder used to two ripple carry adder and provide less carry propagation delay as compare to RCA. The area and power of carry select adder can be reduce with the help of BEC-1 convertor. The basic idea of BEC-1 convertor used the transistor level. When the advantage of transistor level used to less number of transistor than the BEC.

The proposed carry select adder design optimize the area, delay and power consumption than the existing carry select adder design. It can be implemented with the help of universal NAND gate. A universal NAND gate can be used any type of Boolean function without use to other gate. The NAND gate has lesser delay than NOR gate and NAND gate chip are easy to make and very cheap. The NAND gate are easier to fabricate and this basic gate are used in all IC digital logic families. The NAND gate have better performance as compare to other gate.

2. LITERATURE SURVEY

A number of research paper and various journal and conference. We are studied and survey of existing technique. In digital electronic increase the speed of digital system. As we know different type of adder ripple carry adder, carry look ahead adder, carry select adder, conventional carry select adder, SQRT carry select adder etc.

B.Ramkumar and H.M Kittur et.al 2012 proposed low power and area efficient carry select adder. It is used to reduce area and power consumption of CSLA. This proposed work use a simple and efficient gate level modification to optimize area and power. The proposed modification 8-,16-,32-,64-b SQRT CSLA structure compared with exiting regular SQRT CSLA. The proposed design optimize area and power as compare to regular SQRT CSLA with more in delay. The proposed design of CSLA is better than the regular SQRT CSLA[1]. **Shivani Parmar and Kiratpal Singh** et.al 2013 proposes the area and power efficient carry select adder. When the carry select adder is fast adder used in many digital signal processing system and microprocessor. In proposed modified carry select adder are reduce the larger area and power consumption with small speed. The number of logic gate are used to BEC is less than the RCA design.the

modified carry select adder designed for 8b, 16b, 32b, 64b,. This design are used 90nm technology and using Xillinx Spartan-3[2]**. L. Mugilvannan and S.Ramasamy** et.al 2013 proposes the low power and area efficient carry select adder using BEC-1 convertor.

The proposed design reduce the area and power consumption as compare to the SQRT CSLA using BEC-1 convertor delay is more. In this proposed technique are used to optimize the area,delay and power than SQRT CSLA using BEC-1. This are used to reduce the number of transistor of this work offer the great benefit to reduce the area and obiviously to reduce the power consumption[3]**. Pallavi Saxena and Urvashi Purohit and Priyanka Joshi** et.al 2013 describe by the design of low power, area efficient carry select adder. In this paper proposed low power, area efficient carry select adder. An efficient modified carry select adder for 8b, 16b,32b,64b has been proposed using single ripple carry adder with cin = 0 and BEC with cin = 1 with less area and power consumption. This proposed technique are reduce the area, and power consumption of conventional carry select adder. The proposed modified carry select adder aer better than conventional carry select adder[4]. **Basant Kumar Mohanty and S.K Patel** et.al 2014 proposes the area,delay power efficient carry select adder. In this proposed technique are involved conventional CSLA and CSLA based BEC-1 convertor to study the data dependence logic and find redundant logic function. In this proposed paper reduce the all redundant logic functionof conventional CSLA and the proposed design produce the new logic formulation of CSLA. In proposed technique, before calculation final sum, which is different the conventional. It is reduce area and delay as compare to recently proposed CSLA BEC. Due to provide small carry output delay. The proposed CSLA design is good for SQRT adder. Its design are used less area and delay for the existing[5]. **S.Srinandhini and C.A Sathiyamoorty** et.al 2015 propose the design of carry select adder with reduce area and power. The proposed design reduced dala dependence and all redundant logic function present in binary to excess-1 convertor based on conventional carry select adder. The proposed design are using pass transistor logic(PTL) and gate diffusion input (GDI) are reduce the area and power. The gate diffusion input are usd to reduce the propagation delay, area and power consumption. The proposed design aer used the tanner EDA tool[6].**Asit Kumar Subudhi and Rupshree Sahu** et.al 2016 proposes on area optimized carry select adder. This proposed model are implemented in Xillinx using VHDL.power, delay and area are most important part in vlsi design. Conventional carry select adder require more area and power consumption. A proposed design simple to modified of conventional carry select adder design. It is analysed their performance in term of slice, LUT, memory usage, fan out and timing requirement. Sinces the area of proposed is very less, the power consumption is obviously less[7].

3. EXISTING LOGIC

A. Ripple carry adder:-

A ripple carry adder used a simple design. It is connected to cascade in parallel to N number of bit. A logical circuit of RCA the carry out of Cout of each stage is the input Cin of the next stage. It is called ripple carry adder because each carry bit rippled into the next stage. The ripple carry adder the sum and carry out of any next stageis not valid until the carry input occure which the time delay in addition process.

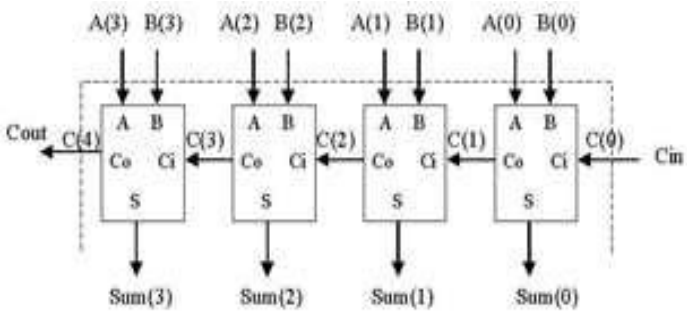

Fig 3.1 : four-bit ripple carry adder

- Ripple carry adder is not very efficient when large number bit numbers are used.
- The delay of adder increases linearly with increase the number of bit length.
- It Calculate the delay from the carry in to carry out is most important because the carry propagation chain will determine the latency of the whole circuit of RCA.

Logic equations:-

gi = ai bi.

p = ai xor bi.

ci + 1 = gi + pi ci.

si = pi xor ci

B. Binary to excess -1 convertor:-

The main idea of this work is to use BEC than using of the RCA with Cin = 1 to reduce the area and lower power consumption. The BEC logic are required fewer number of logic gate than N bit CSLA. The BEC are used to eliminate the carry propagation delay, in the other carry select are used. The 4 bit binary to excess-1 convertor consist of the XOR,

AND and NOT gate. B0,B1,B2,B3 are the input and X0,X1,X2,X3 are the output of the BEC. It reduce the power consumption and area by using gate level modification.

The Boolean expressions:-

X0 =! B0

X1 = B0^B1

X2 = B2^ (B0 & B1)

X3 = B3^ (B0 & B1 & B2)

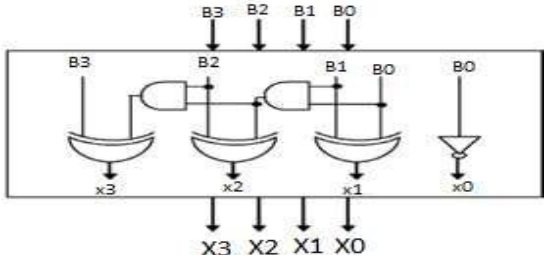

Fig 3.2 : four-bit BEC

C. Conventional carry select adder:-

A conventional carry select adder are use ripple carry adder are use ripple carry adder to generate the carry 0 and 1, before the carry arrive in the top RCA are used the logic value 0 and bottom are used logic value 1. When the multiplexer are used to select the result when carry is "0" path if previous logic 0 or the other carry "1" path if previous carry logic is 1. If the multiplexer are used to select the sum and carry.

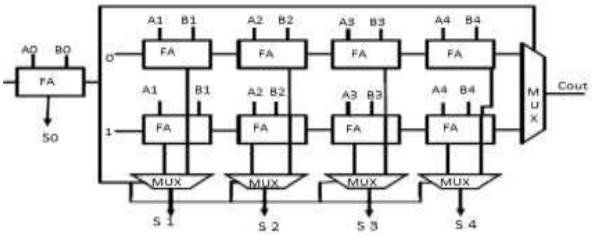

Fig 3.3: Block Diagram of Conventional CSLA

- Multiplexer required larger area.
- Have a lesser delay than ripple carry adder.
- Carry select adder are required smaller number of bits.

D. Linear carry select adder:-

A linear carry select adder is made by two ripple carry adder and multiplexer. It is consist of chaining structure with equal length of carry select adder. It is called linear carry select adder. For N bit adder, two ripple carry adder perform calculation twice, one carry is zero and other is 1. Than provide the result sum as well as the correct carry is than select with the multiplexer.

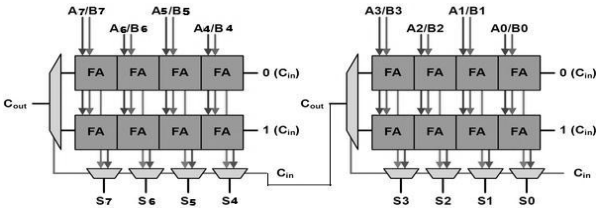

Fig-3.4: block diagram of linear 8 bit CSA

E. Square root carry select adder:-

The square root carry select adder are made by the delay through two carry chain, and the multiplexer block provide the signal to the previous stage. The square root carry select adder are also called the non linear carry select adder. The carry select adder design in these technique get the less area, delay and power consumption as copare to previous logic. It is also good for the SQRT due to less output delay. The SQRT CSLA consume less energy than the existing BEC technique.

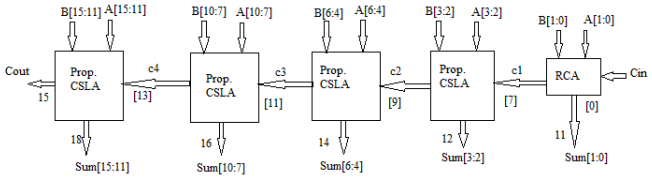

Fig 3.5 : square root carry select adder with n=16

F. Gate level technique:-

The gate level design of using carry select adder are minimize the delay and power consumption of SQRT CSLA. The gate level design are used to AND, XOR, OR, invertor and pass transistor logic, gate diffusion input. When the gate diffusion input is better than pass transistor logic. In digital electronic, a NAND gate is negative of AND gate. When the output are low(0) if input is high(1). If one or both input are low(0) the output result is high(1). The gate level design reduce the number of transistor used in existing logic.

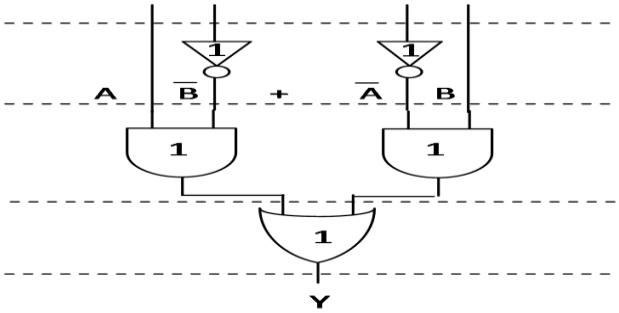

Fig3.6. delay and area evaluation of XOR

COMPARISON TABLE OF EXISTING LOGIC

TYPE OF ADDER	AREA	POWER	DELAY (us)
Regular CSLA	2016.093	35.631(mw)	4.848
BEC CSLA	1362.031	33.45(mw)	3.924
CSA Using PTL	28	3.2289e-002(w)	3.841
CSA Using GDI	26	1.0781e-003(w)	3.211
CSLA Using AND,OR,EX-OR	24	0.039(w)	2.952

4. PROPOSED METHODOLOGY

The proposed design optimized area, delay and power. Power, area and delay is most important parameter in VLSI design. The carry select adder using NAND gate optimize area, delay and power consumption. the conventional square root carry select adder has require more power. The proposed design using NAND gate to reduce the area, delay and power as compare to existing logic. In this, proposed paper identified all the redundant logic function present in existing logic. These proposed design has been reduced all redundant logic operation. The proposed design optimize area, delay and power as compare to previous design and provide new logic formulation of better area and power consumption. Also the AND,OR, and XOR gate are changed into the NAND gate. This NAND gate help to reduce the area and power consumption of the whole system. In this paper we have implemented the optimized area, delay and power efficient carry select adder using NAND gate.

5. CONCLUSIONS

In this work, we proposed a optimize area,delay and power efficient carry select adder using NAND gate with optimize the area, delay and power consumption as compare to previous work in literature. Power, area and delay is most important factor in VLSI design. The proposed work find all redundant logic function present in conventional SQRT CSLA. When conventional CSLA required more chip area and power. In the proposed work reduce all redundant logic operation and provide new logic formulation for CSLA. The proposed design using NAND gate consume less area, it obvious to use less power consumption as compared to existing work.

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