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Digital Static Timing Path Analyzer for DSCH Program

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Abstract - *Miniaturization of transistor size comprises in increasing the complexity of digital circuit design in DSM era. So, successful development of an ASIC depends on accurate modeling of its operation and designing a circuit to be logically correct is simple whereas producing an accurate timing model is critical. IC's are computer representation of the physical device so the designer's role is to design models characteristics with precise accuracy as actual silicon behaves. Timing analysis is an integral part of ASIC design flow. It is important to note that the CAD tools are designed to offer an automation of process to minimize the circuit design cycles, the designer is still a human being who controls how the tool will perform. CAD tools are also susceptible to GIGO: Garbage In Garbage Out, Phenomenon. Thus, the designers are still need to understand the nuances of design methodologies, using CAD tools to obtain optimized design. This paper describes the theory and the procedure applied for timing analysis in EDA tool i.e. DSCH which is a part MICROWIND chip design tool.*

Key Words: **Static Timing Analysis, Timing Path, Critical Delay, EDA tool etc.**

1 INTRODUCTION

As the increase in complexity of digital designs and the requirement of timing measurements in various design stages make static timing analysis critical. Each design stage utilizes static timing analysis to evaluate the system performance, and then optimizes the design accordingly. An accurate and efficient timing analysis package is crucial for the success of the whole design process. Timing is important because just designing the chip is not enough; we need to know how fast the chip is going to run, how fast the chip is going to interact with the other chips, how fast the input reaches the output etc.

There are number of chip design EDA tools that support timing analysis of the design such as PrimeTime from Synopsys, Pearl from Cadense and Chronology's TimingDesigner etc. DSCH is dedicated to provide innovative EDA solutions to mixed signal IC schematics.

We studied the problems in timing analysis feature of DSCH tools are: different timing path, understanding timing paths through image, calculation of logical path delay.

The dissertation of this paper is arranged as, in section-I overview of timing verification and in the section II path delay calculation with an example is demonstrated. In section III the basics of static timing analysis and the dearth of timing path analysis in DSCH tool is presented. In next section IV, the proposed method and the last section the results obtained as well as the extended work is described.

1.1 Overview of Timing Verification

Fig.1 shows a typical ASIC design flow. There are major parts of design flow are as: design entry, design implementation, design verification, and IC production. This is general design flow, and timing verification is part of design verification.

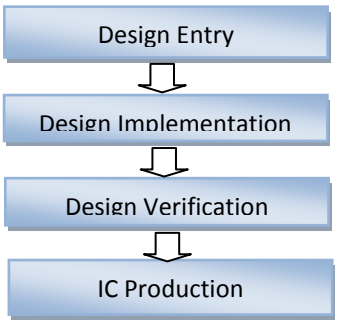

Fig.1 Typical ASIC design flow

Functional simulation is the important step after a design is completed. Functional simulation tests the functional requirement of design. Timing verification determines if the design meets the timing requirements. Dynamic timing analysis and static timing analysis are the methods for verification of timing.

Dynamic timing analysis requires a set of input vectors to check the timing characteristics in a design. It can verify the functionality as well as the timing requirement. It

can be applicable to both synchronous and asynchronous designs.

Completeness of the simulations is also an issue. Simulation cannot prove that the design is free from errors; Static timing analysis offers an alternative to gate level simulation before fabrication. Static timing verifies the design for timing violations without checking the functionality of the design. This method is faster than the dynamic timing analysis as it doesn't requires a set of input vectors.

2. Path Delay

The static timing analysis (STA) is used to measure the delay of every path in a schematic circuit design. The value of gate delays comes from the technology library file of vendor. The interconnect delay can be estimated during synthesis or extracted after physical design that is place and route [2]. The circuit shown in Fig.2 illustrates the basics of STA. Each path traverses interconnect and goes through logic gates.

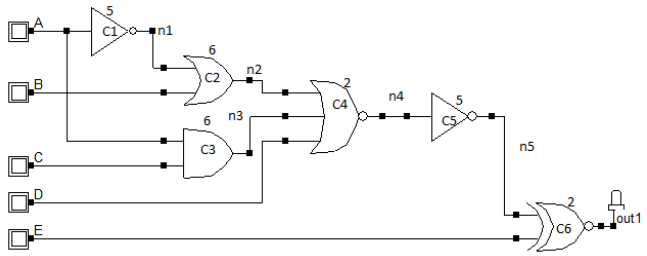

Fig.2 STA measures path delay through a circuit.

The delay through each gate and along each net is totaled to get a path's delay, which can be mathematically presented as the summation of each gate and each net as,

$$\text{Path delay} = \sum(\text{gate\_delay} + \text{net\_delay}) \quad \ldots(1)$$

The path with the maximum delay is A-Out via c1-c2-c4-c5-c6. It takes 26 time units for the output to settle to its final value. The minimum delay is from E to out i.e. 4time units. The paths shown in Fig.2 and their respective delays are listed in table 1.

Path	*Signal Route*	*Delay*
A-out	A-C1-n1-C2-n2-C4-n4-C5-n5-C6-Out	26
A-out	A-C3-n3-C4-n4-C5-n5-C6-Out	20
B-out	B-C2-n2-C4-n4-C5-n5-C6-Out	20
C-out	C-C3-n3-C4-n4-C5-n5-C6-Out	20
D-out	D-C4-n4-C5-n5-C6-Out	13
E-out	E-C6-Out	4

Table.1 Delay paths of Fig.2

The above mentioned theory and calculation of the propagation path delay is implemented in DSCH tool, the snapshot window for the circuit in Fig.2 is as,

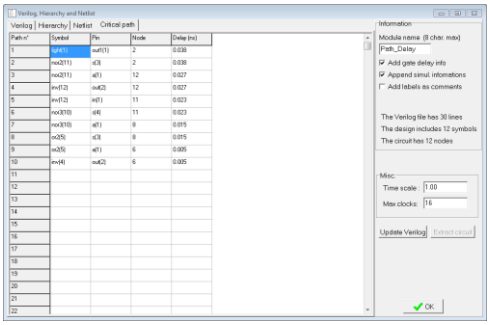

Fig.3 DSCH Path Delay for circuit in Fig.2

but the theory of STA speaks something more which is not implemented in DSCH tool.

3 Basics of Static Timing Analysis

1) What is Timing Analysis??

Before starting we should know what timing analysis is and its importance.

Reasons for performing timing analysis are:

1. Verifying that the timing requirements for the designed circuit are met.
2. To make sure that the circuit designed properly and can work properly at each step "**All Time**".
3. It helps for the component selection based on the speed of component.

It is an integral and important part of ASIC/VLSI design. **Everything can be compromised but not timing.**

Static timing analysis is a method of validating the timing performance of a design by checking all possible paths for timing violations under worst-case conditions.

It considers the worst possible delay through each logic element, but not the logical operation of the circuit.

The Way STA is performed on a given Circuit:

To check a design for violations and to perform STA there are 3 main steps:

1. Design is broken down into set of timing paths
2. Calculates signal propagation delay in each path
3. Add checks for timing violation constraints inside the design and input output interface.

Timing Paths:

Timing path can be divided as the type of signals:

- DATA Path
- CLOCK Path

Each timing path has a “Start point" and an “End point". Depending on the selection of start and end point the definition of timing path varies. [3]

DATA Path:

Start point:

1. Input port of design
2. Clock pin of flip flop/memory

End point

1. Data input pin of flip flop/memory
2. Output port of design

If we use all combination of two types of starting point and two types of end point, we can say that there are four types of timing paths on the basis of start and end point.

1. Pad to Pad
2. Pad to Setup
3. Clock to Setup
4. Clock to Pad

PATH1

Starts at the input port and ends at the output port.

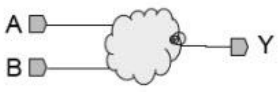

Fig.4.Input to Output

PATH2

Starts at the input port and ends at the data input of sequential element. Following figure illustrates this concept

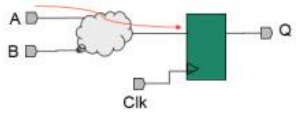

Fig.5 Input to Setup Path

PATH3

Starts at the clock pin of sequential element and ends at the data input of sequential element.

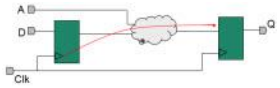

Fig.6.Clock to Setup Path

PATH4

Starts at the clock pin of sequential element and ends at the output port.

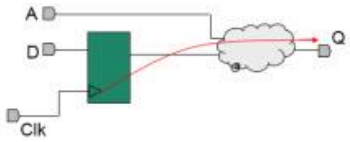

Fig.7. Clock to Output Path

CLOCK Path:

Start point:

1. Clock input

End point

1. Clock pin of flip flop/memory (Sequential Cell)

So far we have discussed the static timing analysis, the timing paths are not introduced in DSCH tool. It is our interest to add this different timing path concept in DSCH tool with the accurate calculation of propagation path delay. The proposed method and results are discussed in further section.

4 Proposed Method

With the discussed theory of STA and the timing path, the proposed the timing path analyzer window snapshot is as shown in Fig.8

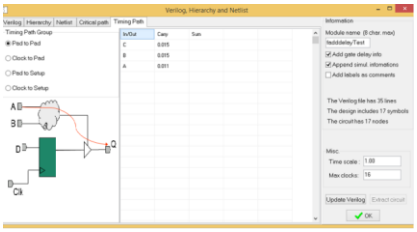

Fig.8 Proposed timing Path analyzer window snapshot

In the proposed method, the timing path concept is implemented. The timing path, Pad to Pad, for the example of full adder circuit shown in Fig.9,

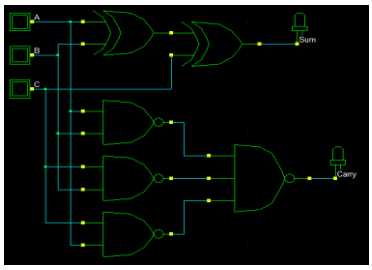

Fig.9 Full Adder Schematic

5 Results

The results obtained for Pad to Pad path selection is depicted as,

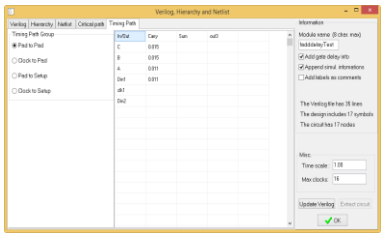

Fig. 10 Timing analysis for the circuit full adder in Fig.9

The results obtained above are for the Pad to Pad path selection, in which the calculation of path delay is made by using the equation (1). And the grid cells of result window are filled with input (Rows) and output (column) and the associated path delay are enlisted.

6 Tools and Platform

For the development of DSCH tool the Pascal computer programming language is used as there are numerous advantages of using Pascal language such as it uses an object-oriented approach, offers maintainable code and many more. Also it can be used in RAD (Rapid Application Development) tool for rapid development of an application.

7 Conclusion

The timing path concept of STA is implemented in DSCH tool, in this for path, Pad to Pad, in which the combinational logic gates are considered for traversing input node to output node. Further work would be extended to the sequential circuits, the circuit schematics containing the sequential circuit such as flip flop.

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