International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 3 | Mar -2017 www.irjet.net p-ISSN: 2395-0072

Design & implementation of 16 bit low power ALU with clock gating

Kajal shinde[1],Priya marathe[2],Pallavi Kesarkar[3],B.Lakshmipraba[4]

[1,2,3]BE Student (DYPIEMR ,Akurdi)
[4]Assistant Professor
[1,2,3,4] Dept. of Electronics & Telecommunication Engineering, DYPIEMR, Akurdi, Pune, Maharashtra, India

---

Abstract - *This project presents the need of ALU in low power concern .Out of the various methods of controlling the low power clock gating is one of the method has proven to be the most versatile. The overall scheme of implementing low power ALU has been presented .CPUs in general purpose personal computers ,such as desktops ,laptops dissipate significantly more power in the order of few watts because of their higher complexity and speed.ALU is a fundamental block of CPU .It does all the processes which are related to all arithmetic and logical operation .As these all operations become more complex, more expensive and requires more space and contributes more power consumption of that ALU is a prime concern while designing of CPU .*

Key Words: ALU, VHDL, Clock Gating, FPGA, Sparten3E

1. INTRODUCTION

Here, main aim to obtain faster device performance and the optimization for lower power dissipation .The ideal design is the one which has less power, less area but it has highest device performance .But, these parameters are contradictory with each other .So, better solution has to be specified to maintain tradeoff between these all parameters .

Now-a-days microprocessors, microcontrollers are designed to be operated at low power with a maximum speed and also in the portable devices, there is more necessity to improve battery life .ALU is the most commonly used module in the CPU during the execution of the instruction .

In this paper, using clock gating technique a 16 bit ALU is designed in VHDL language .For optimization of lower power consumption .A carry skip adder is used as a primary element of the arithmetic unit .The design is stimulated in Isim simulator and finally in Xilinx Spartan 3E FPGA .

Low Power ALU Design is based on application of clock gate to turn off the sub-module of ALU that is not in use by current executing instruction as decided by instruction decoder unit. According to, Clock Power consumes 50-70 percent of total chip power and will increase in the next coming generation of hardware designs at 32nm and below.

Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by hardware designers and is typically implemented by RTL-level HDL Simulator or gate level power analyser tools.

$$(Power = CL \times Voltage \times frequency)$$

In equation power is directly proportional to the square of voltage and the frequency of the clock.

1.1 Dynamic power dissipation

Dynamic power dissipation of CMOS circuit has two parts- dynamic switching power and short-circuit current power . Dynamic switching power is dissipated every time the logic state of the gate changes. It is represented as P = nfCLVdd2, where f is the frequency of switching, CL is the load capacitance, Vdd is supply voltage and n is the probability of switching. This power can be reduced by lowering switching frequency; however it is not desirable as it limits the speed of operation of the device. n can be reduced by reducing redundant switching activity. Vdd can also be reduced, however it leads to increased propagation delays and hence not desirable. Hence a proper tradeoff must be met between these parameters to obtain satisfactory device performance. Short circuit current power is dissipated when both the NMOS and CMOS MOSFETs are partially on, during a switching activity. In this case a direct short circuit path is momentarily formed between power supply and ground, leading to significant power dissipation. This can be controlled by regulating the slew rate and applying sharp clock edges. However, generating such a clock is difficult.

1.2 Static power dissipation

Static or quiescent power dissipation is independent of the switching activity of the circuit. This is caused due to leakage current in the device during steady state. Sub-threshold conduction is the reason for this power dissipation and can be controlled by biasing the MOSFETs well below their threshold voltages and using multiple threshold CMOS designs.

1.3 Clock Gating

Clock power constitutes a significant portion of dynamic power. In a synchronous circuit several modules are clocked at the same time. However, at any particular instant only a

single module may be functional. Hence, unnecessary clocking of the other modules lead to a lot of power dissipation. Clock gating technique is a power down methodology, which involves selectively clocking modules as and when required while keeping other inactive modules in sleep mode. Thus the power dissipation due to charging and discharging of the clock at unused gates, is avoided in this strategy. Clock gating is achieved by ANDing the clock signal with a control signal to form a gated clock, which is then applied to different components of the circuit. To which module the gated clock should be applied is decided based on the control signal.

2. WORKING

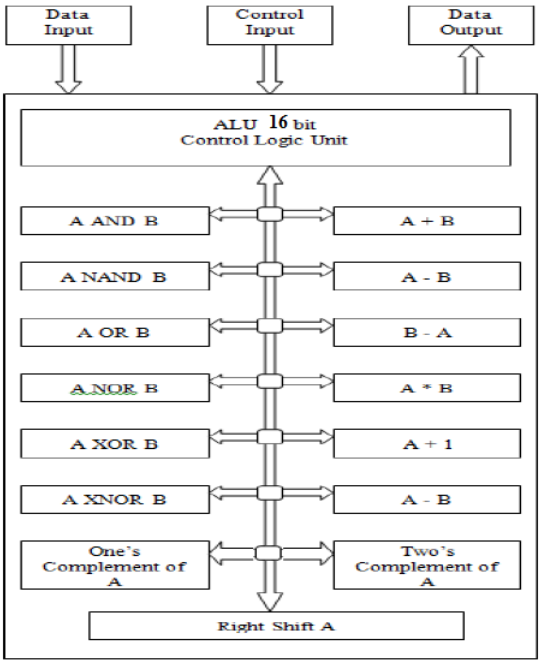

Fig 1: block diagram

2.1 Arithmetic unit

Here it is designed to perform some arithmetic operations. Some operations are addition & subtraction. The core of arithmetic unit is a variable block length carry skip adder. The maximum combinational path delay(pad to pad) from carry input to carry output has been found to be 22.005 ns which is almost same as that of a ripple carry adder, however, the power dissipation is a little lower than the ripple carry adder. The effect of using carry skip adder with variable block length to minimize carry propagation delay is more pronounced for higher number of bits. Each indivisual block is a ripple carry adder. The carry generated in each block enters the ripple carry logic along with carry generated in previous block. A bitwise XOR operation between operands is done with skip logic block & results are ANDed together to form the propagation bit.

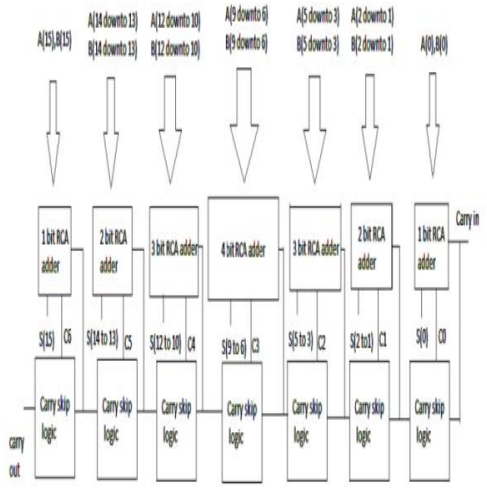

FIG 2: Structure of variable block length carry skip adder

S0	S1	Carry in	Operation
0	0	0	A+B
0	0	1	A+B+1
0	1	0	A+(not B)
0	1	1	A-B
1	0	0	A
1	0	1	A+1
1	1	0	A-1
1	1	1	A

TABLE 1: Operations performed by the arithmetic unit based on s1, s0 & carry in

2.2 logic unit

Operand A & B enter the logic unit through registers controlled by gated clock, like arithmetic unit giving it exclusively of operation only when required by ALU. The logic unit can perform four operations based on selection of s0 & s1.

S1	S0	operation
0	0	A AND B
0	1	A XOR B
1	0	A OR B
1	1	NOT B

TABLE 2: Operations performed by the logic unit based on s1,s0

2.3CLOCK GATING CIRCUIT

The clock gating circuit takes clock input & generates a gated clock based on a control signal s2. The gated clock signal is used to activate arithmetic or logic unit. Preventing unnecessary charging & discharging of clock signal in inactive modules leads to lower dynamic power dissipation.

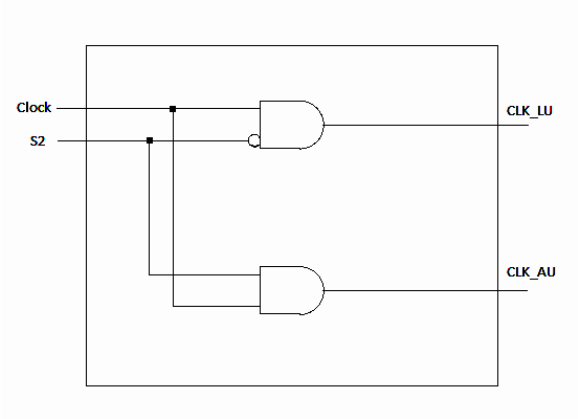

FIG 3: CLOCK GATING CIRCUIT

The master clock input is fed to circuit. When control signal input s2 is zero, clock is gated through second AND gate to arithmetic unit. Thus at a time only one gated clock output is active.

S2	ACTIVATION
0	Logic Unit
1	Arithmetic Unit

TABLE 2: Signal S2 activating different units of ALU

2.4 Output multiplexer and register

The computed outputs from the arithmetic and logic units are fed into the output multiplexer. The proper output is selected based on a control signal. This output is then sent to the output register which is clocked by either of the two gated clocks.

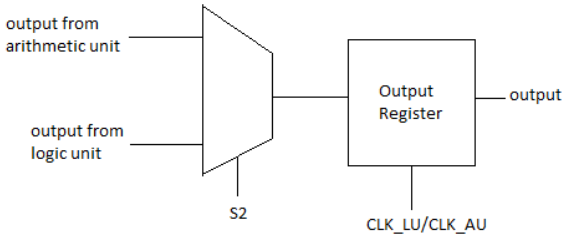

FIG 4: Structure of output register & multiplexer

When s2 is zero, the multiplexer output is taken from the logic unit and when s2 is one the output is taken from the arithmetic unit . the selected output is delivered via the output register clocked by either of the gated clocks.
Operations are performed on 16-bit input operand values namely A and B. On the basis of the value of input opcode a particular operational logic block will be enabled to perform the logic operation.The output of the logic operation is transferred to the output signal register .The operation by the ALU is performed on the edge of the input clock signal.Once the result value is generated, the next operation can be initialized only when the "Enable" input is given a logic high value followed by a logic low value.The registers and output can be reset to logic low values at any time of operation.

3.RESULT

Maximum frequency	65.19 Mhz
Total no. of 4 input LUT	107
Number of bonded IOBs	54
Number of occupied slices	94

4. ADVANTAGES, DISADVANTAGES AND APPLICATIONS

4.1 Advantages

- Reduces dynamic power dissipation of ALU by approx. 66.7%.
- Reduce carry propagation delay.
- Increased performance for high no. of bits.

4.2 Disadvantages

- Large Line Losses.
- Poor voltage regulation.
- Greater size.

4.3 Applications

- Used in portable devices such as cell phone, laptop, computers.
- Used as a multiplier and accumulator (MAC) in DSP.

5. CONCLUSION

Power consumption in modern devices are a growing concern as demands for increased battery life ,lower heat dissipation and increased device reliability is on the rise. Power reduction deals with synthesis, design at circuit level and placement and routing stages, now moved to the System Level and Register Transfer Level. This is possible due to clock gating which always switch off the inactive unit of design & reduce overall power consumption.

6. REFERENCES

1. Wikipedia"http://en.wikipedia.org/wiki"
2. Ankit Mitra," Design and implementation of low power 16 bit ALU with clock gating" **ISSN: 2278 – 1323 International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 2, Issue 6, June 2013**
3. www.google.com
4. Xilinx XST user guide.
5. M. Morris Mano, "Register transfer and Microoperations," in *Computer System Architecture, 3*rd ed. Pearson, India, pp. 106-118.