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Two-Feeder Converter Based Interline Unified Power Quality Conditioner

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Abstract *- Electronic equipment in commercial and industrial process has resulted in increasingly sensitive electrical loads to be fed from power distribution system which introduces contamination to voltage and current waveforms at the point of common coupling of industrial loads. The unified power quality conditioner (UPQC) is connected between two different feeders(lines), hence this UPQC connection is called Interline UPQC (IUPQC).*

Keywords: Distribution system, power quality, voltage sag/swell, voltage source converter, sensitive load.

1.INTRODUCTION

To improve the power quality in the power distribution system, the custom power device like voltage source converter (VSC) is used extensively in custom power applications. Due to the increasing of sensitive loads, the power quality issues are gaining more attention. Disturbance in the distribution network creates almost all the power quality problems.

A DSTATCOM is a voltage source inverter (VSI) based power electronic device. It is supported by a DC capacitor where the short term energy is stored. A DSTATCOM can compensate for unbalanced and distortion in the load such that the balanced sinusoidal current flows through the load [2]. DSTATCOM can regulate the voltage of distribution bus [3]-[4]. A DVR can compensate the distortion and voltage sag/swell in the supply side voltage so that the voltage across the critical/sensitive load is perfectly regulated [5]-[6]. AUPQC can perform both the functions of DVR and DSTATCOM [7]-[8]. Two VSCs are present in UPQC, one of the VSC is connected in series and other is connected in shunt with the same distribution feeder. Supply is provided to the VSCs by a common DC bus.

Two VSCs can also be connected to two different feeders in the distribution system. The VSC performs the operation of DVR. In [9], two separate the adjacent feeders , a configuration called IDVR has been discussed in which two DVRs are connected in series with two different feeders. In IDVR a number of voltage restorers are connected in such a way that they share a common DC link. For the selected line of distribution system the common DC link provides the series compensation.

2. SYSTEM DESCRIPTION

In this paper IUPQC is used to regulate the voltage of feeder-1 and protects the sensitive load from disturbances occurring upstream in feeder-2. In order to maintain the voltage constant in two different feeder lines we are using UPQC configuration. UPQC is connected between two independent feeders. It consists of two VSCs, one is connected in series and the other is connected in parallel with the distribution system. VSC performs both the operation of DVR and DSTATCOM. The two links of the VSCs are supplied by a common DC capacitor.

Here we are taking the various bus voltages and the analysis is carried out. The best suited IUPQC configuration is suggested for the better compensation of distribution system. Finally the transient analysis of the system with IUPQC is analyzed for different faults such as voltage sag in feeder-1, upstream faults in feeder-2 such as L, LG, LLG and LLLG and load change. The structure control and capability of the IUPQC are discussed. The efficiency of the proposed configuration has been verified through simulation studies using SIMULINK/MATLAB.

2.1 Proposed System

The fig-1 shows the single line diagram of IUPQC connected in the distribution system. It consists of two feeders, Feeder-1 and Feeder-2. Each feeders are connected to different substations. The system supplies the loads L-1 and L-2. Vs1 and Vs2 are the supply voltages . From the fig-1 we can observe that the IUPQC is connected between the two buses B-1 and B-2. The voltages of the buses B-1 and B-2 are denoted by Vt1 and Vt2. The currents flowing through the Feeder-1 and Feeder-2 are represented by is1 and is2 while the load currents are denoted by il1 and il2. Vl2 is the load L-2 voltage. The main aim of the IUPQC is to maintain the bus voltages Vt1 and Vt2 constant against voltage sag/swell and other interruptions in the two feeder lines. From this model the IUPQC can absorb the power from one feeder to maintain the voltage of the other feeder constant. This can be obtained by supplying the two VSCs by a common DC capacitor. The main objective of the proposed configuration is to: 1. To protect the sensitive load L-2 from the disturbances occurring in the system by regulating the voltage Vt2. 2. To regulate the bus B-1 voltage Vt1 against sag/swell and or disturbances in the system.

The IUPQC is a device in which UPQC is placed between two individual feeders. UPQC consists of MOSFET based back to back connected two Voltage Source Converters (VSC-1 and VSC-2) supplied by a common DC bus. VSC-1 is connected in shunt with the Feeder-1 and VSC-2 is connected in series with the Feeder-2.

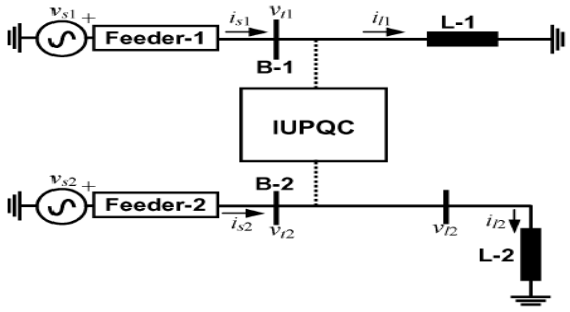


fig-1: Single line diagram

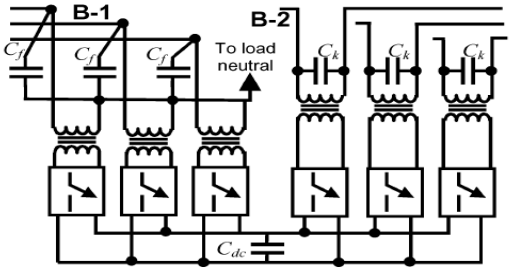


fig-2: Complete structure of IUPQC

The fig-2 shows the complete structure of three-phase IUPQC with two such VSCs. The secondary winding of the shunt connected transformer, VSC-1 is connected in star to the neutral load. The secondary winding of series connected transformer VSC-2 is connected in series with the bus B-2 and the load L-2. Due to the switching operation , the current harmonics are generated. In order to prevent the flow of these harmonics the AC filter capacitors Cf and Ck are connected in each phase. The IUPQC are controlled independently by six inverters.

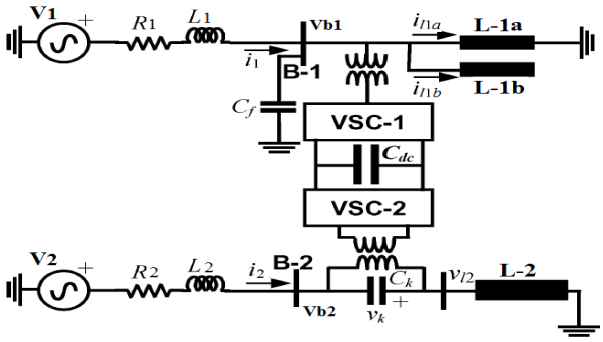


fig-3: IUPQC connected in the Distribution system.

IUPQC connected in the distribution is shown in the fig-3. Rs1, Ls1 and Rs2, Ls2 are the two feeder impedances. Two feeders supplies the loads L-1 and L-2. The load L-1 is again divided into two loads L-1a and L-1b . Where L-1a is the unbalanced part and L-1b is the non-linear part. The currents drawn by these two loads are i1la and i1lb. The load L-2 is the sensitive load which requires regulated and uninterrupted voltages.

2.2 Voltage Source Converter

The structure of VSC is shown in the fig-4. Here each switch is made up of semiconductor devices such as IGBT or MOSFET and anti-parallel diodes are connected to each. The main aim is to produce the AC output waveforms from the DC supply. The length of the Feeder-1 must be twice than that of the Feeder-2.

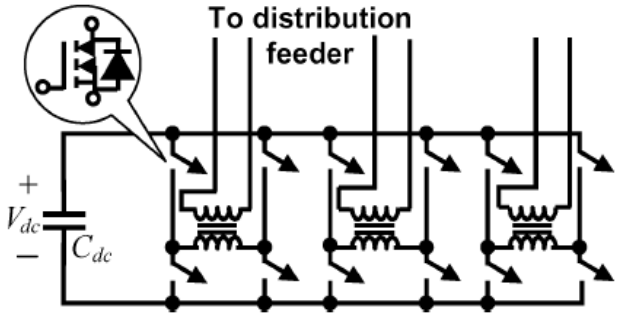


fig-4: Structure of VSC

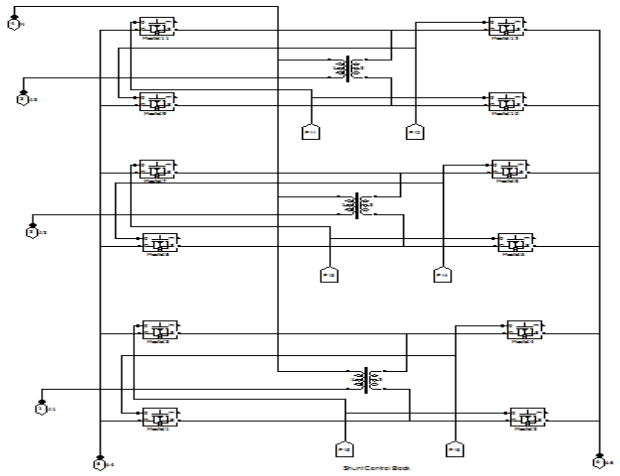


fig-5: Simulink model of VSC

The fig-5 shows the simulink circuit for shunt VSC of IUPQC. It consists of twelve MOSFET switches , out of which four is connected to each phase. For each phase two types of pulses are generated by PWM controller. Two valves operate at each pulse. Say (2 and 12) for first pulse and (1 and 11) for next pulse. At every 60 degree the new valve gets triggered and for 180 degree the valve gets closed. The operation of series VSC is same as that of shunt.

To simplify the simulink design each phase are separately connected to a 1-phase transformer. In this paper we are using the MOSFET as a switch because it has operating frequency up to 1Mhz and the voltage and current ratings of about 500v, 140A. We are not using the IGBT because its operating frequency is only up to 50Khz.

3. GATING SIGNAL GENERATION

3.1 IUPQC Control Strategy

The objective of DVR and active filters is to mitigate the voltage sag and harmonics. The power quality disturbances such as flicker , sag, swell, harmonics, spike, impulsive and momentary interruptions can overcome by UPQC. The main thing is the generation of the control signals. Now we have to generate the reference voltage/currents for compensation and compensating voltage/currents based on reference voltage/currents.

3.2 IUPQC Series Control

Series converter is operated in current control mode. In order to provide the isolation between the load and the supply, the voltage source is introduced between them. The voltage deviation such as sag and swell are compensated by voltage source converter.

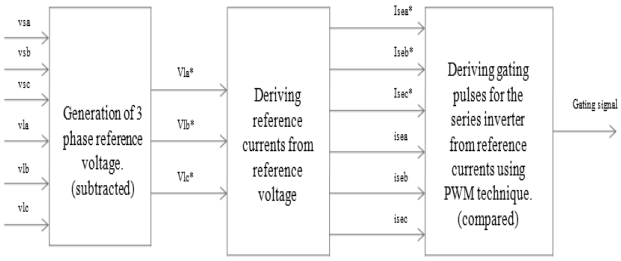


fig-6: Generation of gating signal in series control

By subtracting the three phase load voltages (V1a, V1b, V1c) from the three phase supply voltages (Vsa, Vsb, Vsc) the three phase reference voltages (V1a*, V1b*, V1c*) are generated. From these reference voltages we can obtain the three phase reference load currents (i1a*, i1b*, i1c*). The reference voltages are applied in series with the load. To the common DC link the series inverter acts as a load. The energy of the DC link is exhausted by the series inverter during sag.

The impedance Z so includes the impedance of insertion transformer. The currents (isea*, iseb*, isec*) are ideal currents to be maintained through the secondary winding of insertion transformer in order to inject voltages (V1a, V1b, V1c), so that the desired task of compensation of the voltage sag can be accomplished. The currents Iref (isea*, iseb*, isec*) are compared with Iact (isea, iseb, isec) in PWM current controller. As a result six switching signals are obtained for the MOSFETs of the series inverter as shown in the fig-6. The firing signals enables the series inverter to generate the required injection voltage.

3.2 IUPQC Shunt Control

In order to eliminate the harmonics at the load end and charge the capacitor to the required value the shunt control is used. This involves the generation of the required compensating currents.

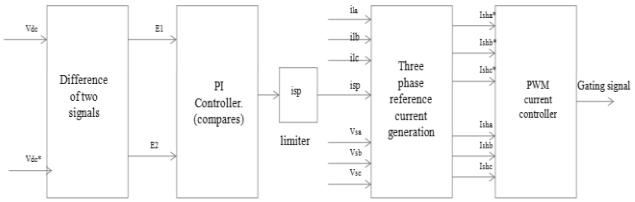


fig-7: Generation of gating signal in shunt control

There are two methods for finding compensating current. They are direct method and indirect method. The direct method is used in the present study. The PI controller compares the DC capacitor voltage with the reference DC capacitor voltage to generate the current Isp. Isp is the magnitude of the three phase reference current. These currents are passed to the three phase reference current generation block. This block computes the reference supply currents in order to drive the shunt VSC. The gating signals are generated by the PWM controller.

4. IUPQC DESIGN CONSIDERATIONS

4.1 Calculation of DC Capacitor (Cdc) And Filter Capacitor (Cf and Ck)

During fault conditions the storing devices have to be provided with the backup energy. This energy is supplied by the capacitor during L-L-L-G faults.

The total power supplied by three phase is given by:

Total 3-phase power = $\sqrt{3}$ VL IL COSØ

=1.09 MW

Where, VL = line to line voltage = 11kV

IL = current through the feeder= $\frac{VL}{ZS^2}$

Cos φ= power component and

$$\Phi = tan^{-1}\left[\frac{XS^2}{RS^2}\right] = tan^{-1}\left[\frac{30.73}{3.07}\right] = 81.20$$

Capacitor voltage falls below 2kV during three phase fault and power supplied by the capacitor is given by:

C=VDCIDC= 1.09 MW.

$$\frac{Vdc^2}{zdc} = 1.09M$$

$$\frac{1}{2\pi fcDC} = 1.09M/\ (VDC)2\{VDC\ Assumed\ as\ 1.6kV\}$$

From the above, taking the values of Vdc below 2kV we get DC capacitor value of Cdc= 3000μF.

To reduce the harmonics present in the AC supply, the filter capacitors Cf and Ck are used. The shunt connected capacitor (Cf) to Feeder-1 should show minimum impedance to the harmonics. Also series capacitor (Ck) connected to Feeder-2 should show maximum impedance to the harmonics. With this criteria the values may be in the range of Cf>20μF and Ck< 50μF.

Table-1: IUPQC system parameters.

SYSTEM PARAMETERS	
Quantities	**Parameters**
System frequency(f)	50 Hz
Voltage source Vs1	11 kV (L-L, rms), phase angle 0°
Voltage source Vs2	11 kV (L-L, rms), phase angle 0°
Feeder-1(R_{s1}+2πL_{s1})	Impedance: 6.05 + j36.28 Ω
Feeder-2(R_{s2}+2πL_{s2})	Impedance: 3.05 + j18.14 Ω
Load L-11: Unbalanced RL Components	Phase-a: 24.2 + j60.50 Ω Phase-b: 36.2 + j78.54 Ω Phase-c: 48.2 + j94.25 Ω
Load L-12: Non-linear load Components	A three phase diode rectifier that supplies a load of 250 + j31.42 Ω
Load L-2: Sensitive load Components	72.6 + j54.44 Ω

Table-2: IUPQC parameters.

IUPQC PARAMETERS	
Quantities	**Parameters**
System frequency	50 Hz
VSC-1 Single Phase transformers	1 MVA, 3/11 kV, 10% leakage reactance
VSC-2 Single Phase transformers	1 MVA, 3/11 kV, 10% leakage reactance
Resistance	R_{f1} =6.0 Ω, R_{f2} = 1.0 Ω
Leakage reactance	2πfL_{f1}=12.1 Ω 2πfL_{f2}=12.1 Ω
Filter capacitor (C_f)	50 μF
Filter capacitor (C_k)	30 μF
DC Capacitor (C_{dc})	3000 μF

4.2 Theoretical Analysis

The bus B-1 voltage is held constant by VSC-1. The fig-8 shows the equivalent circuit of VSC-1. The term u1Vdc is the output voltage of the inverter, Vdc is the capacitor voltage and u1 is the switching action equal to ±n1 which is the turns ratio of transformer of VSC-1.

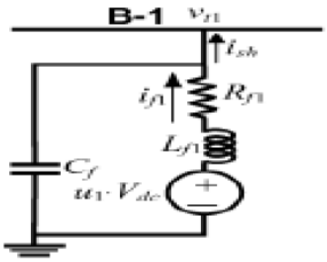


Fig-8. The proportional circuit of the VSC-1

Rf1 and Lf1 are the inverter losses and leakage inductance of the transformer.

Characterizing the state vector as,

$$X^T = [V_{t1}\ i_{f1}] \text{.....(1)}$$

The state space model for the VSC-1 is written as

$$X_1 = F_1 x_1 + G_1 Z_1$$
$$Y_1 = V_{t1} = H_{x1} \text{.....(2)}$$

Where

$$z_1 = \begin{bmatrix} u_{1c} \\ i_{sh} \end{bmatrix} H = [1\ 0], G = \begin{pmatrix} 0 & \frac{1}{C_f} \\ \frac{-V_{dc}}{L_{f1}} & 0 \end{pmatrix}$$

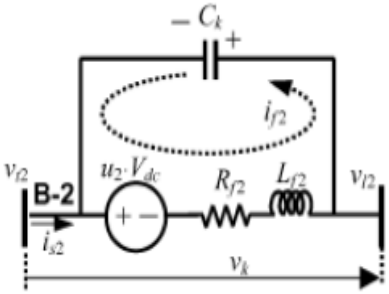
The system is discrete and the input-output is written in the form as

$$A_1(z^{-1})Y_1(k) = B_1(z^{-1})u_{1s}(k) + C_1(z^{-1})\eta_1(k) \text{.....(3)}$$

Where η1 is a disturbance which is equivalent to ish.

To balance the power in the system the phase angle δ1 is adjusted. The proportional control of DC capacitor voltage is given by

δ1= Kp (Vdc avg - Vdc ref)... ...



(4)

Fig-9: The identical circuit of the VSC-2

The fig-9 is the proportionate circuit of VSC-2. Where Vdc avg is the average voltage across the dc capacitor over a cycle, Vdc ref is its set reference value and Kp is the proportional gain.

Characterizing a state and input vector separately, as

$$X^T = [V_{t12}\ i_{f2}] \text{.....(5)}$$

What's more, the state space model for VSC-2 is given as

$$X_2 = F_2 x_2 + G_2 Z_2$$
$$Y_2 = V_{t2} = H_{x2} \text{.....(6)}$$

Where F2and G2 are matrices that are like F1and G1. The discrete-time input–output equivalent of fig-8 is given as

$$A_2(z^{-1})Y_2(k) = B_2(z^{-1})u_{2c}(k) + C_2(z^{-1})\eta_2(k) \text{.....(7)}$$

Where η2is a disturbance which is equivalent to ish2. The main purpose behind VSC-2 is to keep voltage Vl2 steady over the sensitive load. Let 2 V*l2 be the reference load voltage. At that point by applying Kirchhoff's voltage law we get y2ref and is given by

$$Y_{2ref} = V^*_{12} - V_{t2} \text{.....(8)}$$

The peak reference voltage y1ref is taken as 9kV and its point Kp= - 0.25.

4.2 Performance with IUPQC

Initially the DC capacitor is uncharged and at the zero time interval both the feeders and the IUPQC [9] are connected. From the fig-9 we can see that with a peak of 9kV the three phase bus 1(B1) voltage Vt1 is perfectly balanced. The current in the Feeder-1 i.e. is1 is also balanced when Vt1 is balanced. The required system voltage is injected by the converter VSC-2. As a result , the voltage Vt2 of load L-2 is perfectly sinusoidal with a peak of 9kV.

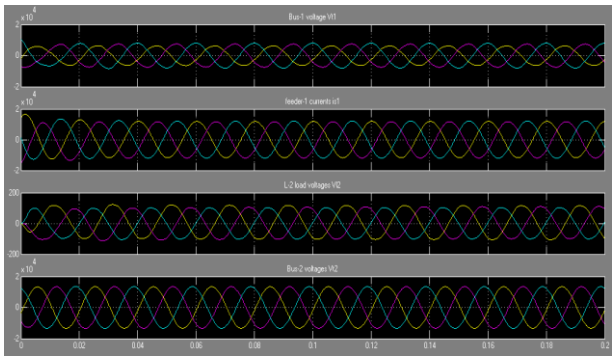


Fig-10: System parameters with IUPQC: B-1 Bus voltage Vt1, Feeder-1 current is1, L-2 load voltage Vt2, Bus-2 voltage Vt2.

The fig-11 shows the waveforms produced in the absence of IUPQC. Due to the presence of unbalanced and non-linear load L-1, the voltage is both unbalanced and distorted. The load L-11 causes an unbalance in current, while load L-12 causes distortion in current.

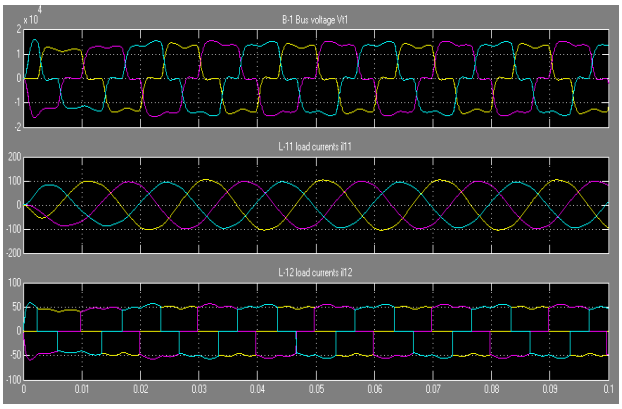


Fig-11: System parameters without IUPQC: B-1 Bus voltage Vt1, L-11 load current i11, L-12 load current i12.

5. IUPQC PERFORMANCE EVALUATIONS

The performance of IUPQC has been evaluated for various disturbance conditions:

- Voltage sag in Feeder-1.
- Performance Limits.
- Upstream fault in Feeder-2. (L-G, L-L-G, L-L-L-G).
- Unbalanced due to load change.

5.1 Voltage Sag in Feeder-1.

The temporary drop in voltage is referred to as voltage sag. The circuit is made turn ON and turn OFF for a time period of 0.15s to 0.25s with the help of circuit breakers. The nominal peak value of the supply voltage Vs1 is 9kV and is reduced to 6.5kV.

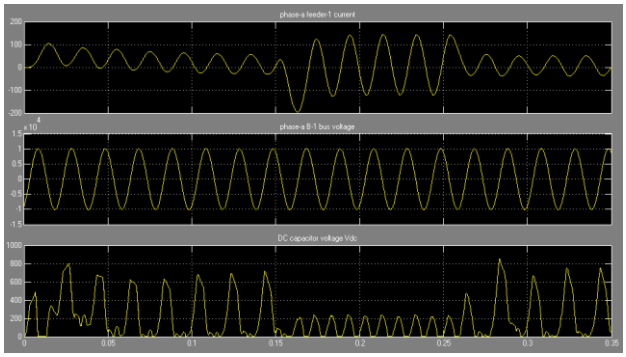


Fig-12: System response during voltage sag in Feeder-1: phase-a Feeder-1 current in A, phase-a B-1 bus voltage in kV, DC capacitor voltage (Vdc) in kV.

Only the phase-a waveforms are shown in the fig-12 and the other two phase are similar. We can see that as soon as the voltage sag occurs, the DC capacitor voltage Vdc drops. If the bus voltage remains constant, the load power also remains constant. The power coming out of the source has reduced since the source voltage Vs1 has dropped. The Vdc drops in order to provide the balanced power to the load. Vdc and phase angle δ1 returns to their steady state as soon as the sag is removed. The feeder current increases in order to supply the same load power at the reduced source voltage.

5.2 Performance Limits.

Observe the fig-3, let the phase voltage of the system be:

$$V_{s1} = V_1 \angle 0^0 \text{ and } V_{t1} = V_2 \angle \delta_1 \quad \text{.....(9)}$$

The Feeder-1 current is given by

$$I_{s1} = \frac{V_1 - V_2 \angle \delta_1}{R_{s1} + jX_{s1}} \quad \text{.....(10)}$$

Where $X_{s1} = \omega L_{s1}$, ω is the fundamental system frequency in rad/s. Therefore the real power per phase entering the bus B-1 is given by:

$$P_{t1} = R_e\{V_{t1}^* I_{s1}\} = R_e\left\{V_2 \angle -\delta_1 \left(\frac{V_1 - V_2 \angle \delta_1}{R_{s1} + jX_{s1}}\right)\right\} \quad \text{.....(11)}$$

$$= \frac{1}{R_{s1}^2 + X_{s1}^2}\left[(V_1 V_2 \cos\delta_1 - V_2^2) R_{s1} - V_1 V_s X_{s1} \sin\delta_1\right]$$

Solving the above equation (11), we get :

$$R_{s1} \cos\delta_1 - X_{s1} \sin\delta_1 = \frac{P_{t1}(R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}}{V_1 V_2} \quad \text{.....(12)}$$

The basis for the performance limit computation is the equation (12). Let us consider both VSCs which are lossless (i.e. the load L-1 entirely consumes the average power which is entering the bus B-1). It is assumed that the entire power is supplied by source Vs2, which is completely required by load L-2. Since V2 (9) is held constant, the load power will remain constant. So for a particular values of source voltage V1 the right hand side of equation (12) is constant. Let this constant be γ.

$$\gamma = \frac{P_{t1}(R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}}{V_1 V_2}$$

Let the feeder impedance be:

$$Z_{s1} = R_{s1} + jX_{s1} = |Z_{s1}| \angle \emptyset_1, \text{ where, } |Z_{s1}| = \sqrt{R_{s1}^2 + X_{s1}^2}$$

So that the reactance and the feeder reactance can be written as :

$$R_{s1} = |Z_{s1}| \cos\emptyset_1 \text{ and } X_{s1} = |Z_{s1}| \sin\emptyset_1$$

Therefore δ_1 from the equation (12) can be written as :

$$\delta_1 = \cos^{-1}\left(\frac{\gamma}{|Z_{s1}|}\right) - \emptyset_1 \quad \text{.....(13)}$$

We know that the line-to-line bus B-1 voltage of 11kV is 1.47 MW (from Tables 1 and 2). For all the three phases the power is supplied equally since the bus B-1 voltage is balanced. Now we choose P_{t1} as 0.49 MW. From the equation (13) we calculate the values of δ_1. As long as the following condition is satisfied, the equation (13) will produce a real solution.

$$\gamma \leq |Z_{s1}|$$

Where γ is equal to $|Z_{s1}|$, δ_1 becomes equal to $-\emptyset_1$. Which is -80.53^0. So source voltage drops to 5.49kV.

By reducing the reference magnitude of bus B-1 voltage V2 or reducing load L-1, the source voltage problem can be solved.

5.3 Upstream Fault in Feeder-2.

A. L-G fault:

The performance of IUPQC is tested for L-G fault that occurs at bus B-2 in Feeder-2. With respect to the ground the phase-a is effected for a time interval of 0.15s to 0.35s. The turn ON and turn OFF is performed by circuit breakers. At a time period of 0.15s, the L-G fault occurs in Feeder-2. such that phase-a of bus B-2 voltage becomes zero. The power fed by the Feeder-2 to the load L-2 is reduced as soon as the fault occurs.

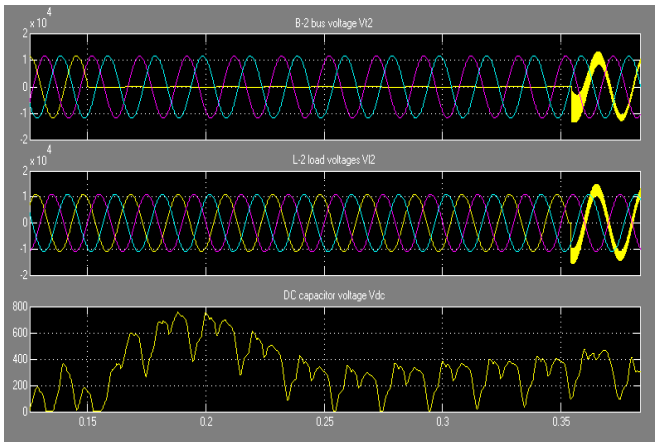


Fig-13: L-G fault in Feeder-2: B-2 bus voltage Vt2, L-2 load voltage Vt2, DC capacitor voltage Vdc.

The Dc capacitors starts to supply the power to the power requirements of the load L-2. Hence the Vdc drops from 3.8KV to 2.7kV. In fig-., we can see that the load voltage is balanced throughout the fault period.

B. L-L-G fault:

In the fig-14 the L-L-G fault occurs at the time period 0.15s. The voltages of both the phase-a and phase-b becomes zero at 0.15s. Even though the L-L-G fault occurs, the load voltage L2 remains balanced. The Dc capacitor voltage now drops from 3.75kV to 2.65kV. It is enough to regulate both the load voltages.

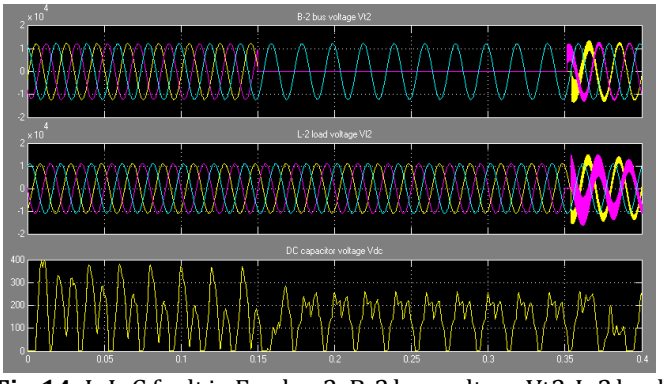


Fig-14: L-L-G fault in Feeder-2: B-2 bus voltage Vt2, L-2 load voltage Vt2, DC capacitor voltage Vdc.

C. L-L-L-G fault:

In the fig-15 L-L-L-G fault occurs at a time period 0.15s. The voltages of all the phase-a, phase- b and phase-c becomes zero at 0.15s. Even though the L-L-L-G fault occurs, the load voltage L2 becomes balanced. To meet the power requirement of the load L2, the Dc capacitor starts supplying this power momentarily. The Dc capacitor voltage now drops from 3.8KV to 2.7kV.

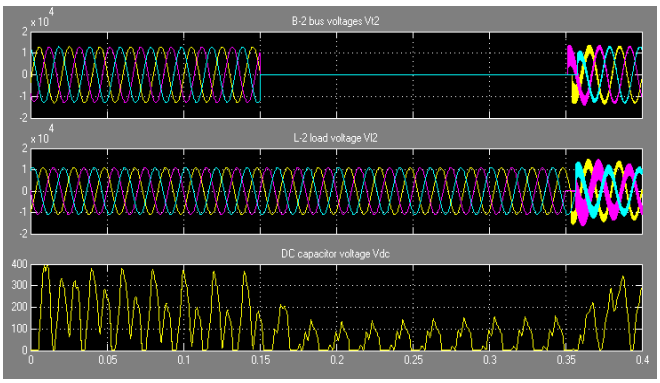


Fig-15: L-L-L-G fault in Feeder-2: B-2 bus voltage Vt2, L-2 load voltage Vt2, DC capacitor voltage Vdc.

5.3 Unbalanced Due to Load Change.

To produce change in load, the impedance is halved at 0.15s by increasing the unbalanced RL load L-11 to twice. Circuit breaker are used to turned ON and turned OFF at a time period of 0.15s to 0.25s. The non-linear load L-12 is un-altered. The DC link voltage is reduced and attain a new steady state as soon as the load increases. The bus B-1 voltage remains unchanged.

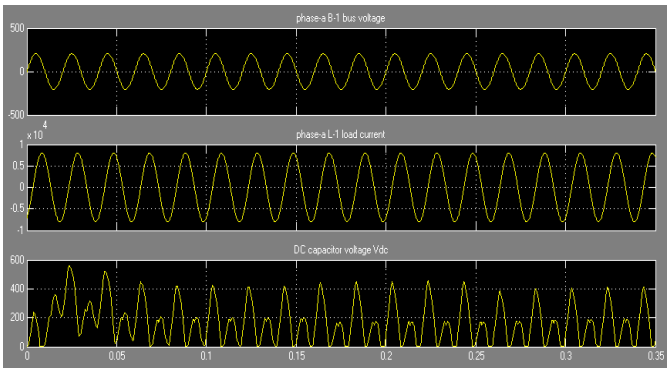


Fig-16: Unbalance due to load change: phase-a B-1 bus voltage, phase-a L-1 load current, DC capacitor voltage Vdc.

6. CONCLUSION

In this paper the control and operation of IUPQC have been demonstrated to mitigate the various power quality issues like voltage sag in Feeder-1, upstream faults in Feeder-2 and unbalanced due to load change. Here we are using two different feeders supplied by two different sub

stations. The device is connected between these two feeder lines. Feeder-1 consists of load L-1 which is non-linear and unbalanced. Feeder-2 consists of load L-2which is sensitive. The main purpose of this design is to protect the sensitive load from disturbances occurring upstream and to regulate the voltage at the terminals of Feeder-1. It has been demonstrated that in case of a voltage sag, the VSC connected plays an important role, as it gives the measure of real power required by the load. The IUPQC can mitigate the voltage sag of about 0.33p.u. (i.e. 9kV) in Feeder-2 and 0.6p.u.(i.e. 9kV to 5.5kV) in Feeder-1 for a long duration. The designed IUPQC is capable of handling the system in which the loads are distorted and unbalanced. In an interconnected distribution system, the IUPQC can be used as a versatile device to improve the power quality.

From this paper, we can observe that the various disturbances occurring in Feeder-1 or Feeder-2 can be protected by using IUPQC. The device works satisfactorily as far as the Vdc is at the reasonable level. The Feeder-1 draws the real power which is ensured by the angle controller to hold the DC link voltage constant. For voltage sag or fault in the Feeder-2, the real power is passed by the VSC-1 through the Dc capacitor to regulate the voltage Vt2 in VSC-2. Finally when the Feeder-1 or Feeder-2 fault is lost, both the VSCs supplies the power required by the loads. The switches of VSC must be rated such that the total power transfer must be possible through them. This may result in increasing of cost of the device. However, the benefits can offset the expense.

The sensitive load is fully protected against interruption and voltage sag/swell. Sensitive load results in severe economic loss which is a part of process industry. By charging the higher tariff for the protected line, the cost can be recovered within 5-10 years. Several customers can also be protected against voltage sag/swell by supplying the regulate bus B-1 voltage. The IUPQC has been shown to compensate for several of these events successfully.

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