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LOW POWER AREA EFFICIENT ARITHMETIC AND LOGICAL CONTROL UNIT USING REVERSIBLE LOGIC

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Abstract - *In this project we are designing a 8 bit arithmetic and logical unit with the help of reversible logic. This ALU consists of 10 operations, 4 logical and 6 arithmetic operations. The logical operation include and, or, ex-or and ex-nor. The arithmetic operation performed by this gate includes set, clear, increment, 1's complement, 2's complement and transfer of input. Reversible logic is gaining interest in the recent years due to its less power consuming and less heat dissipating characteristics. Unlike the irreversible gates that dissipates energy, the reversible computation reduce heat dissipation. The loss of information is associated with loss in physics is requiring that one bit information lost dissipates "KT ln2 of energy". In order to overcome the loss of information we go for reversible computation. The parameters that define an optimum reversible logic based ALU are low quantum cost, reduced garbage outputs and minimum number of reversible gates used. Based on the above constraints of the reversible logic we have designed a ALU with single reversible logic gate namely RC-1 gate. This design is developed using Xilinx 13.4suite, verilog software. It is designed so as to perform 8 bit inputs for both logical and arithmetic operations.*

Key Words: RC-1 gate, reversible computation, garbage outputs, quantum cost; arithmetic and logic operations.

1.INTRODUCTION:

The recent research in VLSI technology is the reversible logic to reduce the power dissipation is the major area of concern. The reversible logic is associated with the combinational circuits without the delay or flip-flops. This was first brought out by Landauer who discovered the power dissipation in conventional or irreversible gates. He stated that only one of the inputs out of 2 given input is given to the output information and the other bit is dissipated. This power loss is major disadvantage in conventional gates. Bennet gave a mathematical proof to this power dissipation is in the form of *KT ln 2*. This led to the development of reversible logic. The concept of the reversible logic focuses on the equal number of input and outputs. In case of reversible logic each input gives an unique output as per quantum mechanics and so as to be mapped as one to one. This kind of output can be useful to get the inputs given and also reduce the loss of power. Quantum mechanics play a vital role in the construction of reversible logic or the quantum gates.

1.1 REVERSIBLE LOGIC:

Reversible are circuits that have one to one mapping between vectors of inputs and outputs, thus the vector of input states can be always reconstructed from the vector of output states. Reversible circuit can realize unbalanced function only with additional inputs and garbage output. In conventional logic gate the 2 inputs form a single output, which leads to the power dissipation in the form of heat. This was found by Landauer and the scientist Bennet proved it to be true by defining the loss of heat in terms of *KT ln 2 joules*. The reversible logic is formed in order to reduce this dissipation in the way that both the inputs are involved to give 2 sets of output that is believed to t the same. It also provides the unique output and output can be used to retrieve the inputs as they are one to one mapped.

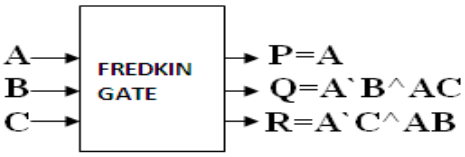
1.2 REVERSIBLE LOGIC GATES:

A reversible logic gate is an n-input n-output logic devices with one-to-one mapping. This helps to determine the outputs from inputs and also inputs can be uniquely recovered from outputs. A reversible circuit should be designed using minimum number of reversible logic gate. Reversible logic gate consists of garbage output and quantum cost. Garbage output refers to the number of unused output present in a circuit, which cannot be avoided as these are very essential to achieve reversibility. Quantum cost refers to the cost of the circuit in terms of cost of primitive gate (1*1 or 2*2).

1.3 BASIC REVERSIBLE LOGIC GATE

1.3.1 FREDKIN GATE:

Fredkin gate is 3*3 reversible gate. The figure shows the input and output of the gate. The quantum cost of fredkin gate is 5. It is used as parity preserving gate and universal reversible gate.

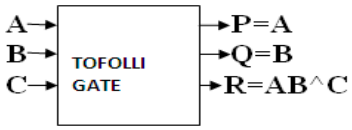


TRUTH TABLE:

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

1.3.2 TOFOLLI GATE:

Tofolli gate is a 3*3 reversible gate. The input vector and output vector are shown in the figure. The quantum cost of tofolli gate is 5. It is suitable for universal gate operations.

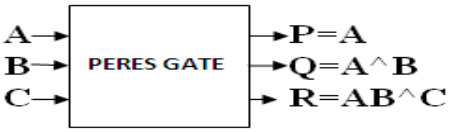


TRUTH TABLE:

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

1.3.3 PERES GATE:

Peres gate is a 3*3 reversible gate. The input and output vectors are shown in the given figure. The quantum cost of the peres gate is 4. Two peres gates can be used for the design of full adder.

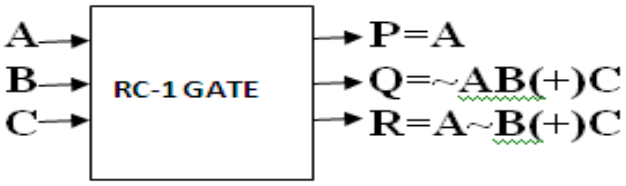


TRUTH TABLE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

1.3.4 RC-1 GATE:

Rc-1 gate is 3*3 reversible gate. The input and outputs are shown in below figure. The quantum cost of the gate is 4. Due to its less quantum cost it is used for this proposed design. It can be used as a one bit comparator



TRUTH TABLE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

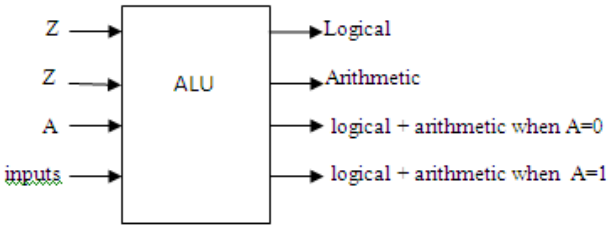


fig (i). General block diagram of reversible 8 bit ALU

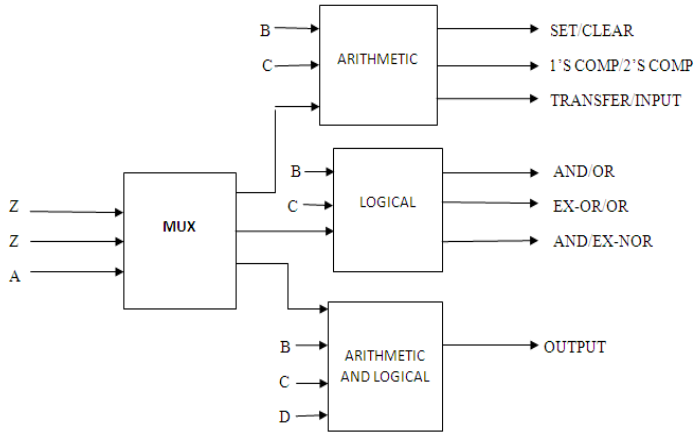


Fig (ii) Detailed block diagram of reversible 8 bit ALU

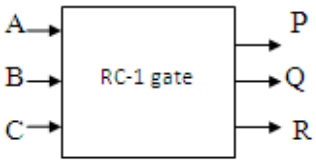
2. PROPOSED WORK

2.1 ARITHMETIC AND LOGICAL UNIT

The ALU consists of a 3 input multiplexer and a 2 RC-1 gate to perform arithmetic and logical operation in case of 8 bit. This multiplexer performs the action so as to select the combination of input. When the input of the mux is given as Z_0' Z_1' when the 'a=0', then the multiplexer produces a output to select only the arithmetic operation. When the input of the mux is given as Z_0' Z_1 when the 'a=1', then the multiplexer produces a output to select only the logical operation. When the input of the mux is given as Z_0 Z_1' when the 'a=0', then the multiplexer produces a output to select only the arithmetic and logical operation when the input A=0. When the input of the mux is given as Z_0 Z_1 when the 'a=1', then the multiplexer produces a output to select only the arithmetic and logical operation when input A=1. The block diagram and the detailed diagram of the ALU is shown below.

2.2 ARITHMETIC OPERATION

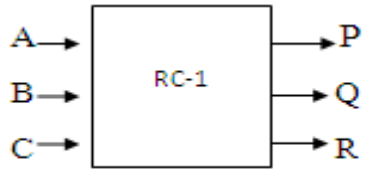
The arithmetic operation is performed using a RC-1 gate. The 3*3 reversible gate performs the following operations they are set, clear, transfer of one input,1's complement,2's complement and increment operations for both 1 and 8 bit.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

2.3 LOGICAL OPERATION

The logical unit consists of a RC-1 gate to perform logical operations such as AND, OR, EX-OR and EX-NOR.



A	B	C	P	Q	R	Q'
0	0	0	0	0	0	1
0	0	1	0	1	1	0
0	1	0	0	1	0	0
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	0	1	1	1	0	0
1	1	0	1	0	0	1
1	1	1	1	1	1	0

2.4 TABLE OF OPERATIONS

The below table shows the total operation of the proposed work. It is all built using a RC-1 gate. This table is given for 1 bit operation. The similar is used for the * bit operations.

Z_0	Z_1	A	B	C	D	Operation performed	Type of operation
0	0	0	X	X	X	Clear, 1' complement , transfer of input	Arithmetic
0	0	1	X	X	X	Set, 2's complement, Increment of a input	Arithmetic
0	1	X	X	X	X	AND, EX-OR,OR,EX-NOR	Logical
1	0	0	X	X	X	Clear, 1's complement, transfer of a input AND ,OR EX_OR	Arithmetic + logical
1	0	1	X	X	X	Set, 2's complement,increment,OR,AND, EX-OR	Arithmetic +logical

Fig(iii) Table operations performed by the ALU

2.5 HARDWARE AND SOFTWARE:

This design is implemented using FPGA trainer kit of the family of Spartan 3E.The details regarding the hardware used is given below.

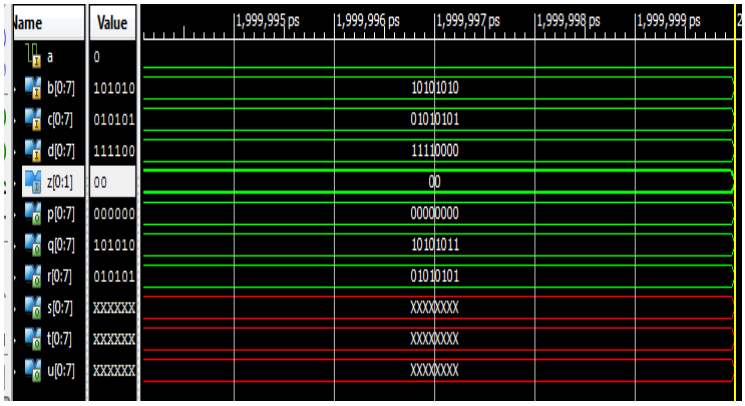
Type	Name
Family	Spartan 3E
Device	XC3S500E
Pack	PQ208
Speed	-4
Simulation tool	XST (VHDL/verilog)
Simulator used	Model sim XE VHDL

Program was developed using XILINX software in order to develop this design. All the bit operations from 1-, 4- and 8- bit operations were performed and verified for the results.

3. SIMULATION RESULTS

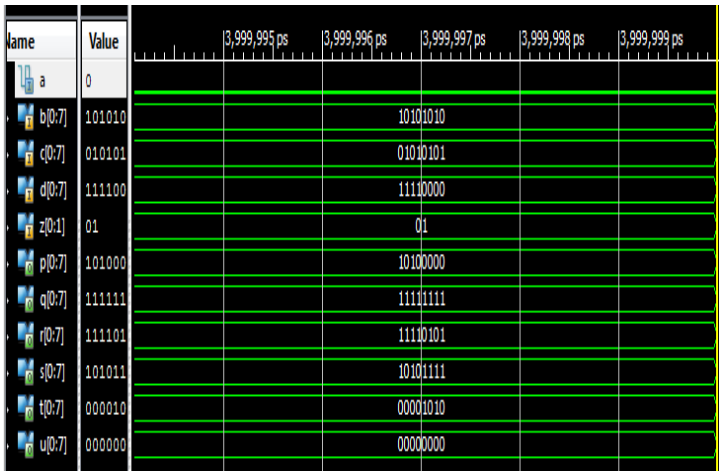
Simulation results are the result of the proposed design. The below are the simulation results of the ALU obtained for inputs b=10101010, c=01010101and d=11110000 for the following conditions.

For z=00 and a=0, the results obtained for 8 bit inputs are arithmetic.

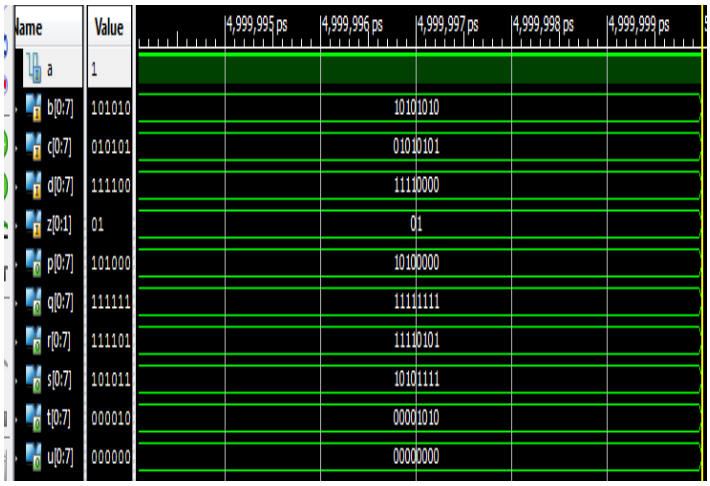


For z=00 and a=1,the results obtained are arithmetic

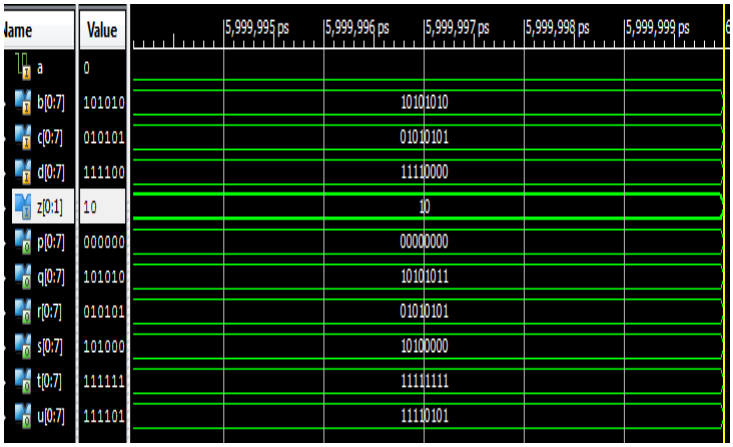
For z=01 and a=0, the result obtaied are logical.



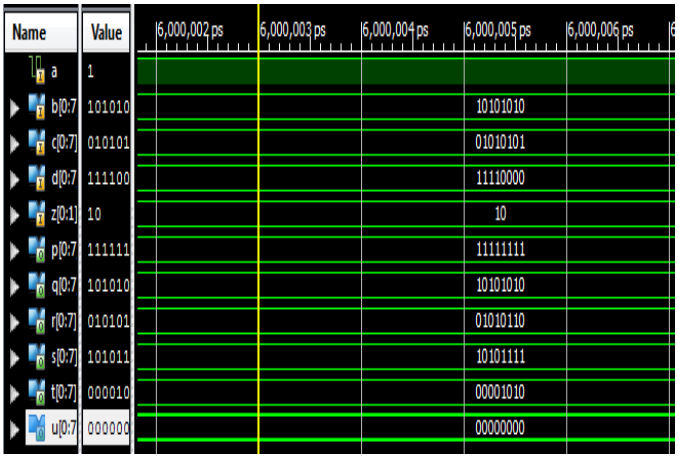
For z=01 and a=1, the results obtained are logical.



For z=10 and a=0, the results obtained are a combination of arithmetic and logical but its when a=1 of arithmetic and d=0 of logical.



For z=10 and a=1, the results obtained are a combination of arithmetic and logical but its when a=0 of arithmetic and d=1of logical.



4. CONCLUSION

4.1 COMPARISION WITH EXISTING WORK:

The proposed model has a great advantage over the existing design as it can be completed using a single gate namely, RC-1 reversible logic gate. This gate can be used as to perform the arithmetic, logical and multiplexer operation without any garbage output. It can also be used as adder subtractor of fewer garbage outputs than the others. This can simultaneously reduce the power consumption and also reduce the manufacture of other gate in large amount. The quantum cost of this RC-1 gate is 4 which is the least and this kind of design can give very few garbage outputs. Unlike other gate that perform 10- 16 operations for a 8 bit ALU this proposed design gives only 10 outputs but with zero garbage outputs which makes the design more efficient

ACKNOWLEDGEMENT

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