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Review On Design Of Digital FIR Filters

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Abstract - *The digital finite impulse response (FIR) is widely used in many digital signal processing (DSP) systems, ranging from wireless communication to image and video processing. Digital FIR filter is primarily composed of multipliers, adders and delay elements. Several techniques have been reported in the open literature to implement digital FIR filters using Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). This paper presents various approaches of designing the FIR filter using Xilinx ISE tool.*

Key Words: **FIR filter1, DSP systems2, FPGA3, ASIC4, Xilinx5, etc.**

1.INTRODUCTION

Filtering is one of the fundamental steps in many digital signal processing (DSP) applications such as video processing, image processing and wireless communication. Basically there are two types of filters- Analog and Digital. Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communications channel, signal detection and analysis in radar application. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. The architectures possess different attributes in the form of speed, complexity, and power dissipation[1].

A filter is frequency selective network, which is used to modify an input signal in order to facilitate further processing. Digital filters have the potential to attain much better signal to noise ratio than analog filters. The basic operation of digital filter is to take a sequence of input numbers and compute a different sequence of output numbers. There exists a range of different digital filters. FIR and IIR are two common filters forms. A drawback of IIR filters is that the closed-form IIR designs are preliminary limited to low pass, band pass, and high pass filters etc. Secondly FIR filters can have precise linear phase. Also, in case of FIR filters, closed-form design equations do not exist and the design problem for FIR filters is much more under control than the IIR design problem.

Adders, multipliers and Delay element are the key block used in the in the implementation of digital FIR filter. Basically, FIR filter performs a linear convolution on a window of N data samples which can be mathematically expressed as follows:

$$y(k)=\sum w(n).x(k-n) \quad \text{for } 0\leq n\leq N-1$$

The direct form of implementation of an FIR filters can be readily developed from the convolution sum as shown in fig1. Direct form FIR filters are also known as tapped delay line or traversal filters. N-tap filters consist of N delay elements, N multipliers and N-1 adders or accumulators. The impulse response of the FIR filters can be directly inferred from the tap coefficient h.

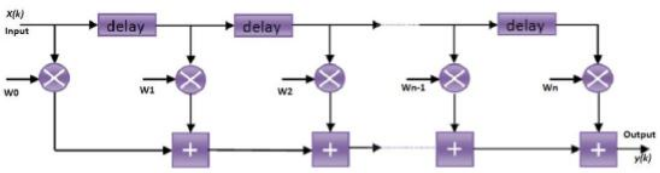

Fig-1:-Block diagram of digital FIR filter

This paper describes the review work on design of digital FIR filters using different designing approaches and its implementation results obtained through Xilinx.

2. LITERATURE REVIEW

The research paper on the design of FIR filters are published in various journals and presented in many conferences. Here the paper selected describes the design of FIR filters using VHDL or Verilog language. Some of the paper represents the modular design approach of the FIR filters and which is implemented in spartan-3E FPGA/Xilinx Virtex-5 FPGA.The evaluation result shows good area/power efficiency and flexibility by using different architectures for application. .Most papers have used microprogrammed FIR filters design approach .

Abdullah A.Aljuffri, Aiman S. Badawai , Mohammad S.Bensaleh, Abdulfattah M.Odeid and Sayed Manzoor Qasim [1] in paper entitled "FPGA implementation of scalable micro programmed FIR filter architectures using Wallace tree and Vedic multipliers". In this paper used Wallace Tree and Vedic multipliers for implementation of 8-tap and 16-tap sequential and parallel micro programmed FIR filters architectures which shows in fig. 2 and fig. 3 respectively.

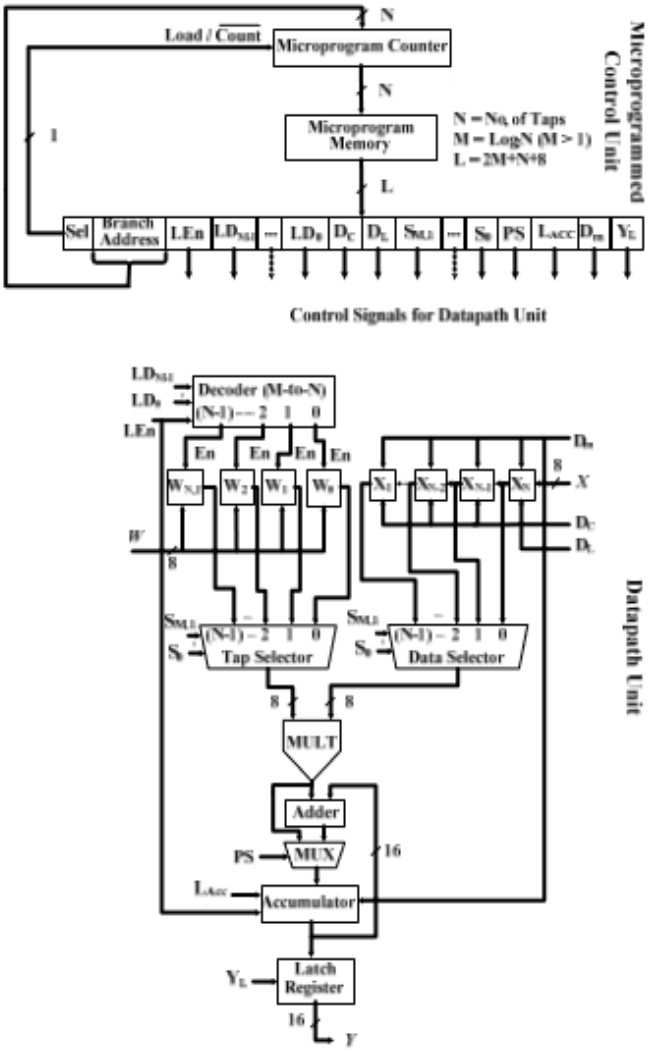

Fig-2: Architecture of sequential micro programmed FIR filter

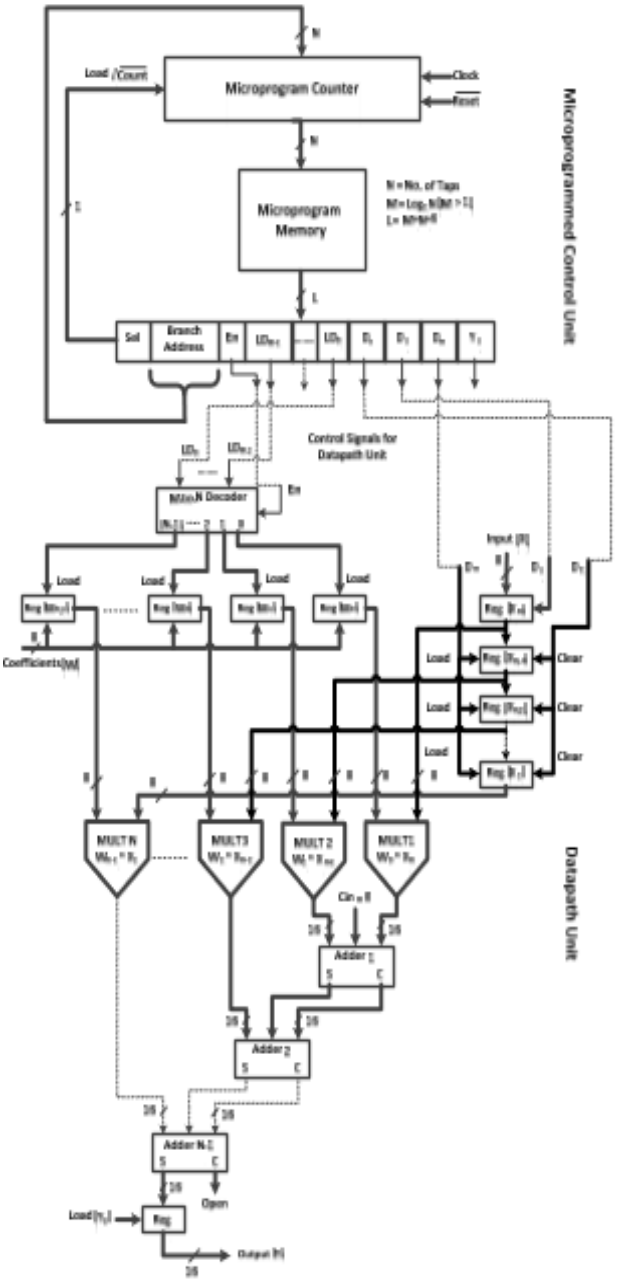

Fig-3: Architecture of parallel micro programmed FIR filter

The designs are realized using Xilinx virtex-5 FPGA. Synplify pro tool used for synthesis, translation, mapping and place and route process and Reports are generated by CAD tool. Performance analyze base on parameter such as minimum period, slice LUTs and maximum operating frequency. The sequential FIR filters architecture designed using Wallace Tree multiplier seems to be more efficient as compared to Vedic multipliers. For 8-tap FIR filter using Wallace Tree have minimum period 11.448 ns and maximum operating frequency 87.4 MHz And for 16-tap FIR filter using Wallace

Tree have minimum period 10.491 ns and maximum operating frequency 85.3 MHz .

A. Aljuffri. M. M. AlNahdi, A.A.Hemaid , O. A. Alshaalan, M. S. BenSaleh, A.M. Obeid and S. M. Qasim [2], in paper entitled, "ASIC realization and performance evaluation of scalable micro-programmed FIR filter architectures using Wallace tree and Vedic multiplier". In this paper, Wallace tree and Vedic multiplier are used for efficient realization of 8-tap and 16-tap sequential and parallel scalable micro-programmed FIR filter architectures. The designs of FIR filter are coded in VHDL. Lfoundary 150nm standard-cell based technology is used for the hardware realization of the proposed designs in ASIC. Synopsys Design Compiler is used for the gate-level synthesis. Analyze the performance based on area, Slice LUTs and critical path delays. Wallace tree multiplier using CSA (Carry Skip Adder) has minimum area and delay while Vedic using KSA (Kogge-Stone Adder) has maximum area and delay. For 8-tap FIR filter have period 6.62 ns for 8-tap filter have period 6.62 ns and area 29496 μm^2. For 16-tap FIR filter have period 6.63 ns and area 47463 μm^2 .

Sushma .S and Shobha .S [3] in paper entitled, "Design and implementation of sequential micro programmed FIR filter using efficient multipliers on FPGA". In this paper 8-tap sequential FIR architecture is implemented. Implementation of 8-tap sequential digital FIR filter is presented Using Wallace Tree and Vedic multiplier which is Coded in VHDL. The designs are realized using Xilinx Virtex-5 FPGA. FPGA Resource utilization of Wallace Tree and Vedic multiplier has improved. Analyzed the performance based on the parameter minimum period, slice LUTs and maximum frequency. Implementation result have maximum operating frequency 217.68 MHz, minimum period 4.595 ns and slice LUTs 99 [3].

Pramod Kumar Meher and Abbes Amira [4], in paper entitled, " FPGA realization of FIR filters by efficient and flexible systolization using Distributed Arithmetic". This paper present the realization of 8-tap and 16-tap Digital FIR filters by systolic decomposition of distributed arithmetic (DA). Implemented on Xilinx Virtex-E XCV2000E FPGA using hybrid combination of Handel-C and parameterizable VHDL cores. Analyze the performance on the basis of maximum operating frequency. Implementation is found less area-delay complexity. Implementing 8-tap FIR filter give maximum operating frequency 74.025 MHz and for 16-tap FIR filter 67.222 MHz .

S. C. Prasanna and S. P. Joy Vasantha Rani [5], in paper entitled, "Area and Speed efficient implementation of symmetric FIR Digital filter through reduced parallel LUT Decomposed DA approach .In this paper, implement 16-tap symmetric FIR filter using Reduced parallel LUT decomposed DA (Distributed Arithmetic) approach which is implemented over Xilinx virtex-5 FPGA device-XC5VSX95FT-1FF1136. The proposed design reduces the no. of LUTs. This design Support upto the maximum operating frequency of 607MHz and requires lesser clock period than high throughput DA based design. It offers 60.5% less delay than systolic DA based design .

Rakhi Thakur and kavita khare [6], in paper entitled, "High Speed FPGA implementation of FIR filter for DSP Applications". This paper presented on high speed FPGA implementation of FIR filter. FPGA offers higher sampling rate and lower cost than ASIC. This paper describes an approach to the implementation of digital filter based on FPGA which is coded in VHDL. Analyze the performance base on the parameter such as minimum period is 4.255 ns and maximum frequency 235.026 MHz The result presented requires low area and total memory usage is 147920 kilobytes .

Mahesh Golconda and Maruti Zalte [7], in paper entitled, "Comparative analysis of Multiplier and Multiplier-less method used to implement FIR filter on FPGA". In this paper, 8-tap FIR filter is implemented using multiplier and multiplier-less method. In multiplier method, Modified Booth and a Modified Booth with Wallace tree multiplier is designed, While in multiplier-less method, distributed arithmetic and distributed arithmetic with partition is used. Designs are coded in verilog. The code is simulated in Model Sim and synthesized in Xilinx 14.7. Modified Booth with Wallace Tree method has the least delay 8.957 ns among all the other methods. Distributed arithmetic with partition which is a multiplier less method had a greater delay than multiplier methods but covers the least area i.e. 165 slice LUTs. As the area is less, power dissipation is also less than others .

Table -1: overall analysis of literature review for 8-tap FIR filter

Comparison table shows the comparison of various approaches of designing the sequential, parallel and symmetric Digital FIR filter. Analyzed the performance based on the parameter such as minimum period, maximum operating frequency, area and slice LUTs.

FOR 8-TAP					
REF. PAPER NO.	TEHNIQUE	MIN. PERIOD (NS)	MAX. OPERATING FREQ .(MHZ)	SLICE LUTS	AREA (μM^2)
SEQUENTIAL					
[1]	Wallace tree	10.143	98.6	147	-
[1]	Vedic multiplier	10.660	93.8	230	-
[2]	Wallace tree	6.62	-	-	29496
[2]	Vedic multiplier	6.92	-	-	35158
[3]	Wallace tree and Vedic multiplier	4.595	217.68	99	-
[7]	Modified booth	10.221	-	565	-
[7]	Modified booth with Wallace tree	8.957	-	263	-
[7]	DA	18.235	-	2532	-
[7]	DA with partition	16.854	-	165	-
PARALLEL					
[1]	Wallace tree	17.552	57.0	699	-
[1]	Vedic multiplier	17.680	56.6	1217	-
[1]	Vedic multiplier	17.680	56.6	1217	-
[2]	Vedic multiplier	27.80	-	-	96190
SYMMETRIC					
[4]	Distributed Arithmetic (DA)	-	74.025	-	-

Table -2: overall analysis of literature review for 16-tap FIR filter

FOR 16- TAP					
REF. PAPER NO.	TEHNIQUE	MIN. PERIOD (NS)	MAX. OPERATING FREQ .(MHZ)	SLICE LUTS	AREA (μM^2)
SEQUENTIAL					
[1]	Wallace tree	10.491	85.3	180	-
[1]	Vedic multiplier	11.000	90.9	246	-
[2]	Wallace tree	17.552	57.0	699	-
[2]	Vedic multiplier	6.96	-	-	52508
PARALLEL					
[1]	Vedic multiplier	11.000	34.1	2490	-
[2]	Wallace tree	50.32	-	-	126310
[2]	Vedic multiplier	52.22	-	-	192311
[5]	High throughput DA based (r=1)				
[5]	Systolic DA based	4.17	239	-	-
[5]	Reduced parallel LUTs decomposed DA approach	1.646	607	-	-
SYMMETRIC					
[4]	Distributed arithmetic	-	67.222	-	-

3. CONCLUSIONS

The review on paper shows various approaches of designing the Digital FIR filter. The performance analyzed based on the parameter such as minimum period, maximum operating frequency, area and slice LUTs. From the comparison of the review papers in above table it is concluded that the design of digital FIR filter by using Wallace tree and Vedic multiplier having less delay and moderate operating frequency but increases the area. Booth has moderate delay but it reduces the partial products which gives design of high speed digital FIR filter. DA based approach having more delay as compared to other approach. Thus this review gives brief idea that by designing the digital FIR filter in VHDL, the filter can be made more efficient and its speed can be increased. Hence it can be used in more application, making it more flexible and upgradable.

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REFERENCES

[1] Abdullah A.Aljuffri, Aiman S. Badawai, Mohammad S.Bensaleh, Abdulfattah M.Odeid, Sayed Manzoor Qasim, "FPGA implementation of scalable microprogrammed FIR filter architectures using wallace tree and vedic multipliers,"proc.of 2015 IEEE international conference.

[2] A. A. Aljuffri. M. M. AlNahdi, A.A.Hemaid, O. A. Alshaalan, M. S. BenSaleh, A.M. Obeid and S. M. Qasim , "ASIC realization and performance evaluation of scalable microprogrammed FIR filter architectures using wallace tree and vedic multipliers," Proc. Of 2015 IEEE Intl. conf.on Environmental and electrical engineering (EEEIC),pp.1-4,june 2015,accepted.

[3] Sushma .S and Shobha .S, "Design and implementation of sequential microprogrammed FIR filter using efficient multipliers on FPGA," Int.journel of information technology and computer engineering ,Special Issue:NCRASET-16.

[4] Pramod Kumar Meher ,Abbes Amira, "FPGA realization of FIR filters by efficient and flexible systolization using Distributed Arithmatic,"IEEE Transactions On Signal Processing .

[5] S. C. Prasanna and S. P. Joy Vasantha Rani , "Area and Speed efficient implementation of symmetric FIR Digital filter through reduced parallel LUT Decomposed DA approach, circuits and systems ,2016 ,7,1379-1391,Received 25 March 2016;accepted 22 april 2016;published 9 june 2016.

[6] Rakhi Thakur and kavita khare, "High Speed FPGA implementation of FIR filter for DSP Applications," International Journal of Modeling and Optimization , vol.3,No 1,February 2013.

[7] Mahesh Golconda and Maruti Zalte, "Comparitive analysis of Multiplier and Multiplier-less method used to implement FIR filter on FPGA," International journal of technical research and application e-ISSN:2320-8163,volume 4 Issue 3(May-June, 2016), pp.370-375.

[8] T.D.sawarkar, Lokesh Chawle, N. G. Narole, " Implementation of 4-tap sequential and parallel Micro-programmed based Digital FIR filter architecture using VHDL," International journal of innovative research in computer and communication engineering (An ISO 3297: 2007 certified organization) vol. 4, Issue 4, April 2016.