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DESIGN OF BRIDGELESS HIGH-POWER-FACTOR BUCK-CONVERTER OPERATING IN DISCONTINUOUS CAPACITOR VOLTAGE MODE.

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Abstract - *In this paper, a new bridgeless single phase ac–dc power factor correction (PFC) rectifier based on buck topology operating in discontinuous capacitor voltage mode (DCVM) is proposed. The bridgeless topology and the presence of only one or two semiconductor switches in the current flowing path during each interval of the switching cycle result in lower conduction losses compared with the conventional DCVM buck PFC rectifier. The DCVM operation offers additional advantages such as zero-voltage turn-off in the power switches, zero-voltage turn-on in the output diode, and continuous input current. Hence, the electromagnetic interference noise emission is minimized. The converter achieves high power factor naturally with low total harmonic distortion in the input current. All the simulation works is carried out in MATLAB/SIMULINK and the results are presented.*

Key Words: ***Discontinuous capacitor voltage mode (DCVM), electromagnetic interference (EMI), power factor correction (PFC), total harmonic distortion (THD).***

1.INTRODUCTION

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2 [1]. Discontinuous inductor current mode (DICM) and discontinuous capacitor voltage mode (DCVM) are typically suitable for low-power applications; however, both topologies have, in general, inherent PFC properties unlike continuous current mode (CCM) topologies. Active PFC techniques based on basic dc–dc converter topologies have been developed for high power factor (PF) and low input current harmonic ac/dc rectification [2], [3]. However, conventional PFC rectifiers allow the current to flow through two bridge diodes in addition to the switching component of the converter. This results in higher conduction losses increasing the thermal stresses of the converter. In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits where the current flows through a minimum number of switching devices compared with the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced, and higher efficiency can be obtained and cost savings. Recently, several bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft switching techniques or coupled magnetic topologies [4]–[10].

However, all of these rectifiers operate in DICM and suffers from high switch current stress causing higher conduction losses. In addition, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. Interleaving two bridgeless boost converters can significantly minimize the input current ripple and doubles the transferable power [11]. However, besides the complex control, interleaving PFC boost converters have low efficiency at low power levels due to high component count. Thus, for universal input line and for low-power applications (<300 W), all of the reported topologies in [4]–[11] suffer from having low efficiency at low input line (Vac = 90 Vrms) due to the high input current, which produces higher conduction losses in the circuit components. Operating the converter at the boundary of DICM/CCM with variable switching frequency [12] can improve the efficiency at low line at the expense of complex control. On the other hand, the buck PFC is an attractive solution for universal input voltages at power levels (< 300 W). The buck PFC can achieve high efficiency over the entire universal input line voltage range with distorted input current that comfortably passes the limits imposed by IEC 61000-3-2 requirements [1]. In addition, the ability of the buck PFC converter to generate output voltages less than the line peak voltage has beneficial effect on the performance of the downstream dc/dc output stage because it allows a more efficient design for the dc/dc stage by using lower voltage-rated semiconductor devices. In [13], a bridgeless buck PFC

rectifier operating in CCM with clamped current- mode control is proposed. High efficiency is achieved over the entire load, and input voltage ranges at the cost of complicating the control circuitry.

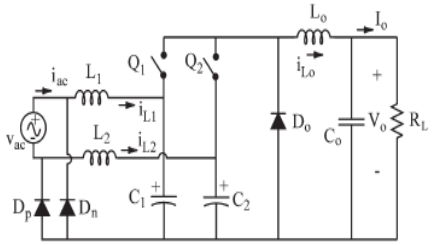

Fig. 1. Proposed bridgeless DCVM PFC topology with two active switches.

The drawbacks of complex control associated with CCM operation and high current stress associated with DICM operation can be overcome by operating the converter in DCVM mode. This operation mode offers soft turn-off switch capability; the soft turn-off capability allows using insulated-gate bipolar transistor (IGBT) as the switching device that typically has higher turn-off losses due to the tail current of IGBT. In addition, continuous input current can be obtained with converters operating in DCVM; hence, the input filter size is minimized, and the electromagnetic interference (EMI) noise emissions are reduced. Several DCVM topologies with inherent PFC capability have been published in the literature [14]–[18]. However, all of these topologies utilize a full bridge rectifier as a front end that results in lower efficiency. In this paper, a new bridgeless buck converter operating in DCVM mode is presented. Unlike the PFC boost converter, the proposed converter has the same advantages as the conventional full-bridge PFC buck DCVM converter such as inherent inrush current limitation during startup and overload conditions, lower input current ripple, lower diode reverse recovery losses, and less EMI noise. Compared with the conventional full-bridge PFC buck DCVM converter, the proposed converter has lower number of simultaneously conducting semiconductor components; hence, the conduction losses and the thermal stresses on the semiconductor devices are further reduced, and the circuit efficiency is improved. It should be mentioned here that the main drawback of the DCVM operation is the switch voltage stresses, which increase with the load current. Thus, the proposed converter is intended for low-power applications. For high-power applications, then fixed duty-cycle variable frequency control should be used to compensate for load variations in order to avoid an additional increase in the switch voltage stress.

II. PROPOSED BRIDGELESS CONVERTERS

Figs. 1 and 2 show the two proposed bridgeless DCVM PFC buck converters. Fig. 1 shows the first topology, which utilizes two power switches (*Q*1 and *Q*2). The two switches can be driven by the same control signal, which significantly simplifies the control circuit. Note that *Q*1 and *Q*2 are single quadrant switches; hence, a diode is added in series with the switch. The second topology utilizes a single switch instead of two switches, as shown in Fig. 2. Compared with the conventional full-bridge DCVM buck topology, the structure of the proposed topology utilizes one additional inductor and one capacitor that are often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared with a single inductor. In addition, unlike DICM PFC converters, the continuous input current results in low conducted EMI noise, which reduces input filtering requirements dramatically. The return diodes *Dp* and *Dn* always provide low-impedance current path for the return current.

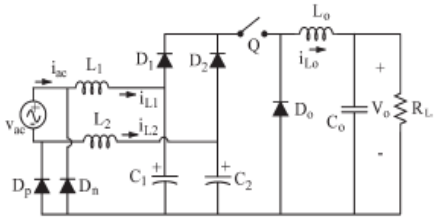

Fig. 2. Proposed single-switch bridgeless DCVM PFC topology.

III. PRINCIPLE OF OPERATION AND ANALYSIS

The converter of Fig. 1 is analyzed. The analysis assumes the proposed converter operates at a steady-state condition in addition to the following assumptions.

1) The input signal is a pure sinusoidal voltage.
2) Inductors L1 and L2 are large enough such that the current through them can be considered constant over one switching cycle Ts.
3) The low-frequency energy storage element Co is large enough such that the output voltage Vo can be considered constant during the half-line cycle of the line frequency fL.
4) The input capacitances C1 and C2 have low capacitance values to operate in DCVM. During the positive half-line cycle, L1-C1-Q1-Lo-Do are active through diode Dp, which connects the input ac source to the output ground. During the negative half-line cycle, L2-C2-Q2-Lo-Do are active through diode Dn, which connects the input ac source to the output ground. Due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-cycle of the input voltage. The circuit operation in DCVM can be divided into three distinct operating stages during one switching period Ts, as shown in Fig. 3. The topological stages of the proposed converter over a switching period Ts can be briefly described as follows.

Stage 1 [0 ≤ t ≤ D1Ts]: in this stage, switch Q1 is turned on, and capacitor C1 is being discharged. The switch current iQ1 is equal to the output inductor Lo current iLo, whereas iC1 = iL1 − iLo at the condition iLo > iL1. During this stage, the

diode Do is reversed biased by the voltage across capacitor C1. This interval ends when the voltage across the input capacitor VC1 linearly decreases to zero.

Stage 2 [D1Ts ≤ t ≤ DTs]: in this stage, switch Q1 is still turned on and the input capacitor C1 stays discharged. The switch current iQ1 is equal to the input current iL1. The output stage diode Do starts conducting. The diode current during this stage is equal to iLo − iL1. This stage ends when Q1 is turned off.

Stage 3 [DTs ≤ t ≤ Ts]: this stage starts when switch Q1 is turned off. The input capacitor current iC1 is charged by the input current iL1; hence, the input capacitor voltage VC1 linearly increases and reaches a maximum of VCM at the end of the switching cycle t = Ts. During this interval capacitor, C1 is being charged with a constant current (iL1).

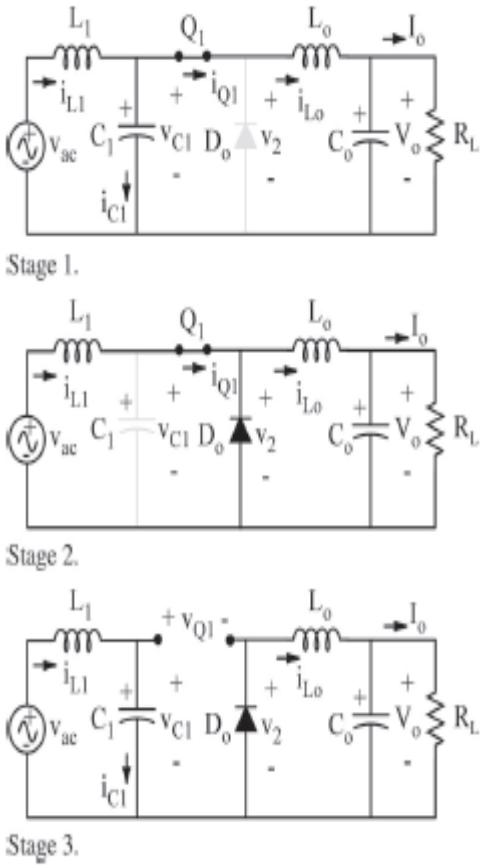

Fig. 3. Topological stages over one switching period *Ts* during positive half line cycle.

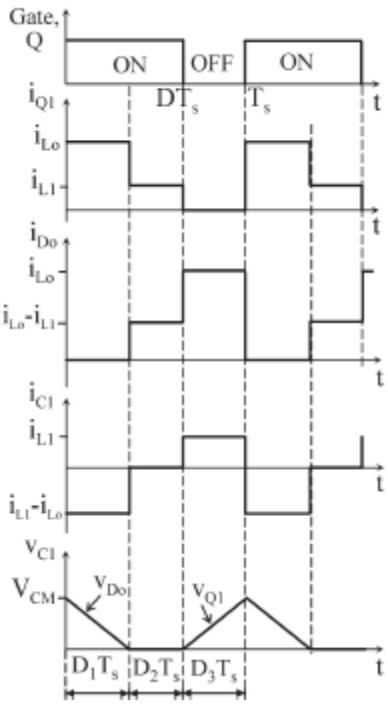

Fig. 4. DCVM waveforms over one *Ts* for the converter of Fig. 1.

IV. PERFORMANCE ANALYSIS

The output voltage , Power factor(PF), total harmonic distortion(THD)of the proposed converter during, sudden changes in load were analysed in this section.
Simulation results shows converter operation at different load conditions, Total harmonic distortion (THD), and PF values are improved in the proposed bridgeless topology. MATLAB simulation was utilized to perform the simulation for the analysis.

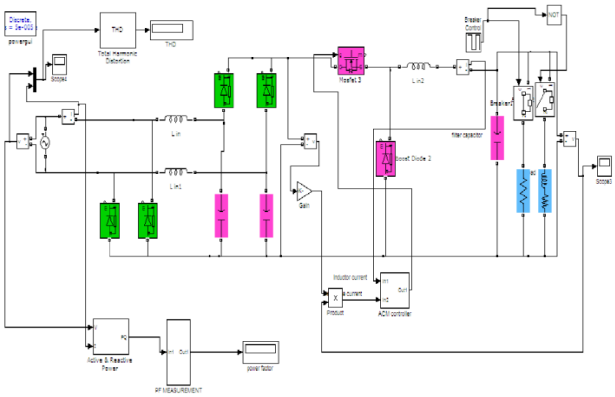

Fig. 5.MATLAB/SIMULINK diagram of the proposed bridgeless DCVM buck PFC converter.

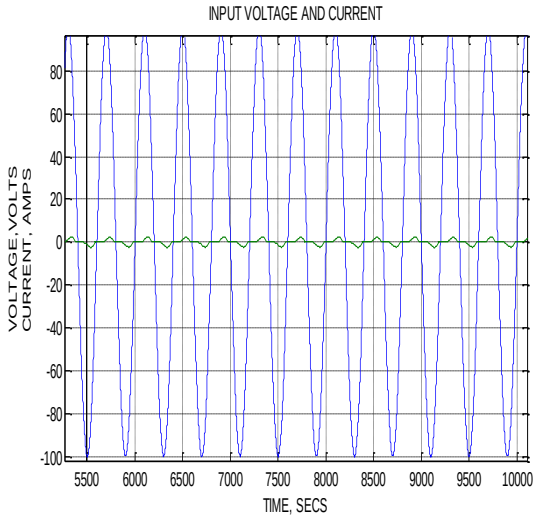

Fig. 6.Input voltage and current waveforms(100 V_{ac})

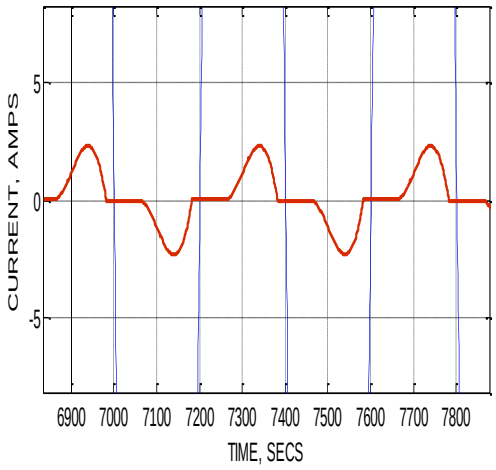

Fig. 7.Input current waveforms(2 Amps)

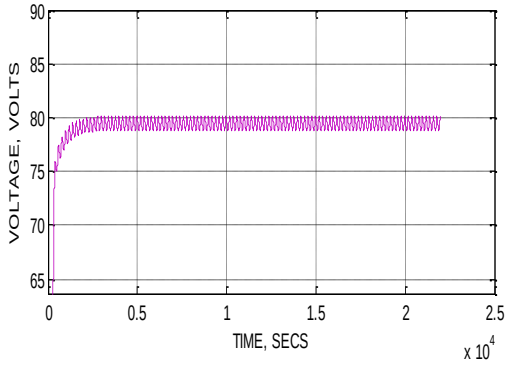

Fig. 8.Simulated voltage waveform of the converter across the load (V_o=80volts, R=100 ohms)

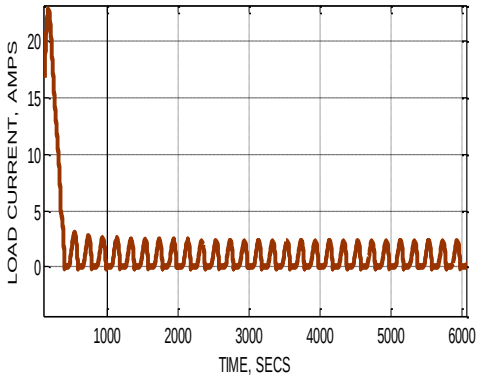

Fig. 9.Simulated load Current waveform of the converter (I_L=2 Amps, R=100 ohms)

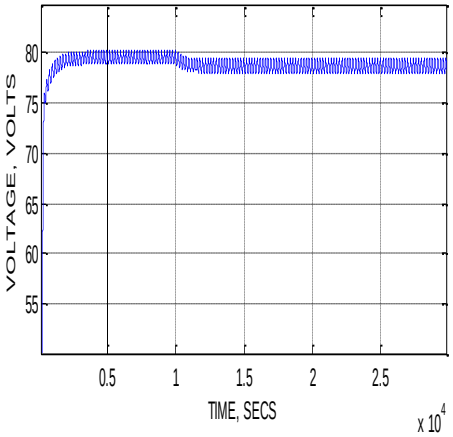

Fig. 10.Simulated voltage waveform of the converter across the load during sudden change in load from 100 ohms to RL load of 1000 ohms and 3mH (V_o=79Volts)

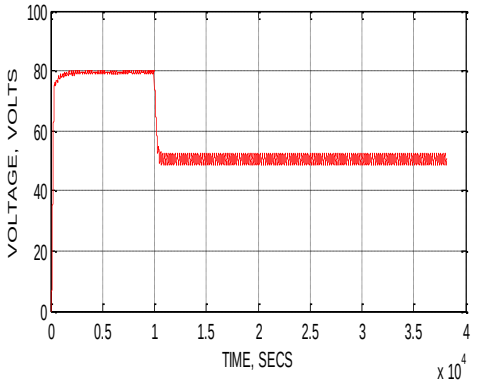

Fig. 11.Simulated voltage waveform of the converter across the load during sudden change in load from 100 ohms to R load of 10 ohms (V_o=50 Volts)

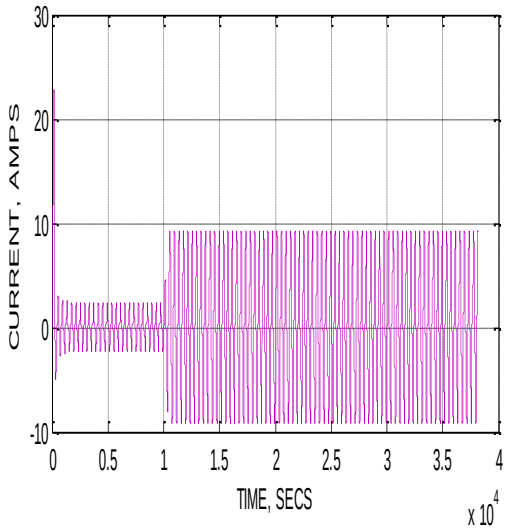

Fig. 12.Variation of current drawn from the supply when the load changes from 100 ohms to 10 ohms.

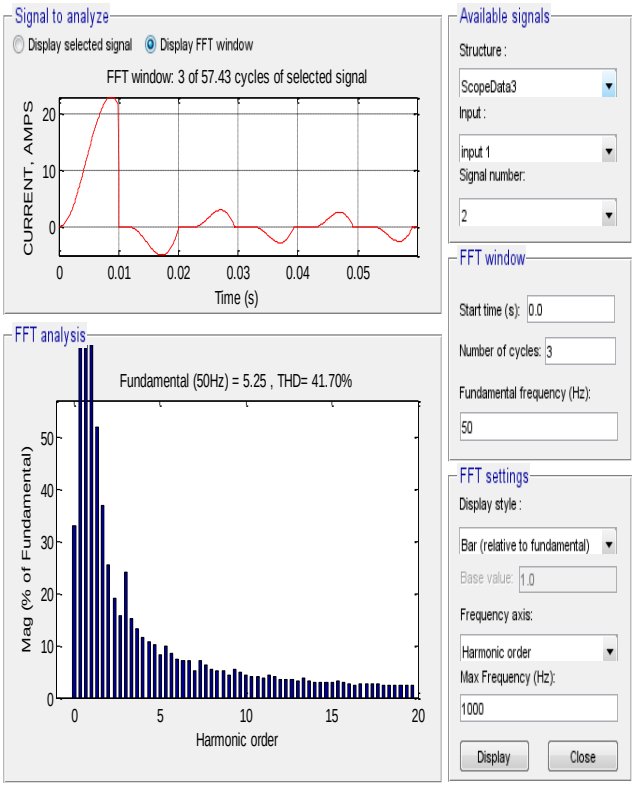

Fig. 13.FFT analysis (THD=41.70%).

V. CONCLUSION

A single-phase bridgeless step-down buck PFC converter topology operating in DCVM has been introduced. The proposed converter can achieve natural PFC with low line current harmonic distortion while ensuring zero-voltage switching for the active switches and the dc side diode. The simulation results verify the advantage of DCVM topology of soft switch turn-off and continuous input current. The efficiency, power factor and THD of the converter have been improved versus the full-bridge DCVM topology. The proposed topology complies with the international standards, i.e., EN 61000-3-2. The new topology has been verified via MATLAB SIMULINK.

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