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Designing of Asynchronous Viterbi Decoder for Low Power Consumption using Handshaking Protocol: A Technical Review

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Abstract - *This paper gives a review on various methods used for designing of Asynchronous Viterbi Decoder for low power consumption using different handshaking protocol. It gives an idea about various decoding techniques for reducing reoccurring memory operations and repeating switching activity. This paper describes the synchronous and asynchronous design methodology of Viterbi Decoder for low power consumption. Here it also states the different handshaking protocol for making Asynchronous Viterbi Decoder to Synchronize and to communicate with different units of Viterbi Decoder for low power consumption. This paper also gives a brief idea about various decoding techniques for designing of Viterbi Decoder.*

Key Words: Asynchronous Viterbi decoder, Handshaking Protocol, Convolutional Encoder.

1.INTRODUCTION

Viterbi decoding has the advantage of the fixed decoding time. Now a days about one billion cellphones are using Viterbi decoder, and it is the most probably the highest number in any application. The current consumer of VA processor is digital video broadcast systems. A Viterbi decoder with convolutional decoding is a FEC technique used for a channel that transmits corrupted signals. The FEC adds some redundant bits to increase the capacity of the channel.

A famous approach adopted in the Viterbi Decoder design is Asynchronous or the timing strategy as it saves power as it have to generate global clock for the system. In Viterbi decoder is decoded by the following two well known methods known as the (TBM) and (REM). The switching activity problem of Viterbi Decoder can be reduced by combining TB and REM that is (HREM). Further (MTHREM) has been employed for low switching activity.

2. TECHNICAL REVIEW

In this paper[1] the comparative study of asynchronous and synchronous design methodology is done. This paper describes the different decoding techniques for Viterbi decoder which reduces the switching activity and number of memory operations. It states the handshaking protocol to make synchronous system asynchronous to communicate with the various units of VD.

Paper [2] describes reconfiguration for FPGA cells are done. FPGA consumes high static and high dynamic power. So to reduce this static and dynamic power LEDR Architecture is used. In this system if any device is not in use or the transistors are not active then they are set at sleep mode immediately. The functional unit are set to low leakage mode to reduce the power. LEDR is two phase dual rail encoding in which spacer not necessary. Low power consumption and high throughput is achieved as number of signal transitions are reduced. Power analysis is carried out and is found out as 7mWatt.

In this paper [3] a low power designing of FPGA is done using two types of encoding. LEDR encoding at input side and 4-Phase Dual Rail Encoding is at output side, as first method gives high through and reduced power consumption and second method gives reduced area. As FPGA clock network consist of significantly more registers and thus it consumes more power. So to solve this clock problem, here asynchronous FPGA's are proposed. The number of input output blocks and LUT's are reduced in proposed method and delay is increased here. The conventional logic block has the problem of detecting the data. Here the data is detected at inaccurate timing hence power consumption increases. So in this architecture this problem is overcome and power reduction achieved.

A new AFPGA's architecture is described in given paper [4] to reduce the power consumption. As FPGA have more registers for high programming and complicated switching blocks. The dynamic power consumed by switching block and clock signal is dominant. So asynchronous bit-serial

architecture is given here to reduce the power consumption. To make operation independent of data-path length LEDR encoding is used here and expresses its area efficient implementing system. In this paper 90 nm CMOS technology is used to implement asynchronous field programmable VLSI system and as compared to dual rail and 4-phase encoding the transistors count for each cell in FPVLSI is only 13% large. And power consumption per unit cell is 58%.

This paper [5] implements high throughput and moderate area of constraint length K=3, and code ret R=1/2 hand decision parallel Viterbi decoder. The ACS delay latency is reduce using designing ACS unit with the help of new look ahead carry adder and digital comparator. The advantage of REM and TBM are combined for reducing the required area and decoder latency Viterbi Decoder. The described decoder operates at 250 Mhz. The proposed ACS architecture have 67.07% improved latency deduction when we compared it to conventional ACS architecture and output is Gbps and improvement in area is 73.03% to 92.46% is achieved.

In this paper[6] gives in VLSI integrated circuit used in mobile communication systems reducing the power consumption has become a fundamental design goal. Thus Asynchronous design is becoming more attractive than that of Synchronous as it achieves high speed and low power consumption. Given paper focuses on design of VLSI architecture of Viterbi Decoder using low power VLSI technologies with self time controlled and voltage switch logic techniques. Here Request-Acknowledge Handshake pair controls the communication within the decoder blocks and signals to ensure that valid data is ready and it has been accepted after designing the simulation results gives 90% power reduction using asynchronous design comparison with synchronous design.

In this paper [7] the comparison of existing DI 2-phase protocol in reference with speed, power and coding efficiency is given for practical implementations. Now a days, communication protocols are receiving tremendous attention. The given energy saving 2-phase protocol are LEDR, LETS and TrasEnc. Here comprehensive comparison encoder/decoder is performed with respect to static power, dynamic energy and propogation delay. Results shows that LEDR has the most lightweight and fastest implementation.

In this paper [8] gives the interconnection implementation foe delay insensitive variations and LEDR encoding. In LEDR complete decode and detectioning circuit is fast, and simple. Because the decoding and level based detection and not based on transition. Here LEDR encoding is chosen as compared to normal decoding. Thus communication latency of the LEDR interconnect reduced to half when compared to conventional LEDR interconnect. Its current mode signaling implies it to achieve more speed by not using pipelining and repeaters. And thus the throughput of the 1GBPS for one pair of wire is 5mm of total length of the wire.

In this paper[9] the four-phase dual-rail encode and LEDR encode is combined for presenting asynchronous FPGA. To achieve small area and less power for functional units 4-phase dual-rail encoding is used here and for achieving high throughput and less power for data transfer LEDR encoding is used here. In this paper the given fabrication of FPGA is done using the e-shuttle 65 mm CMOS processor & operated in 870MHz. Here the results achieved shows implies that the power consumption of the system is reduced to 38% for workload of 15%.

In this Paper[10] the LETS that is delay insensitive data encode technique used in global communication is evolved. LET$ is the generalizing technique of LEDR that is it was non-return to zero encode scheme. Here one out of the given two wires changes the information of data bit per transaction. It has the potential power and throughput advantage. Its advantage is because of few railing switches and non return-to-zero plane. In this paper 1-out of-4 LETS codes have been proposed and hardware completing detection technique is introduced. Finally the simplest way for generation of such code is given.

3. CONCLUSIONS

Here in this literature survey the different methods are given to design asynchronous Viterbi decoder for low power consumption. It also compares the asynchronous with synchronous methodologies and gives different techniques for Viterbi decoder. To avoid the unnecessary memory operations the reduced switching activity techniques and different handshaking protocol are given in this literature survey. The ACS and SMU units of Viterbi decoder consumes more power, so we have to take care for optimization of these units. And for this we have to consider some points such as switching activity, bandwidth, timing, throughput, overhead etc. This literature survey concentrates on the LEDR handshaking protocol. It enhances the throughput of coding and it is delay insensitive.

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BIOGRAPHIES

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