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REVIEW PAPER ON 32-BIT RISC PROCESSOR WITH FLOATING POINT ARITHMATIC

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Abstract - *The paper proposes 32-bit RISC processor with floating point arithmetic for high speed and low power consumption .It is having five stage pipelining which is designed using VHDL. Number of instruction are designed for this processors. We use 5-stage pipelining which involves instruction fetch module, instruction decode, module, execution module, memory i/o and write block.*

Key words: ***RISC processor, Floating point arithmetic, VHDL, Xilinx, Instruction set.***

1.INTRODUCTION

1.1 Processor

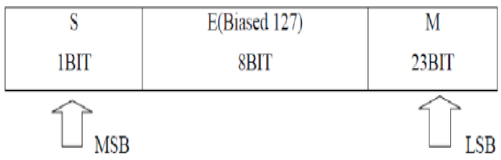
A processor is the logic circuitry that responds to and processes the basic instructions that drive a computer. The term processor has generally replaced the term central processing unit (CPU). The processor in a personal computer or embedded in small devices is often called a microprocessor. Types of processors according to the Instruction set:-

1.1.1 CISC (Complex instruction set computing): The CISC concept is an approach to the Instruction Set Architecture (ISA) design that emphasizes doing more with each instruction using a wide variety of addressing modes, variable number of operands in various locations in its Instruction Set. As a result, the instructions are of widely varying lengths and execution times thus demanding a very complex Control Unit, which occupies a large real estate on Chip[9].

1.1.2 RISC (Reduced instruction set computing) : The RISC Processor have reduced number of Instructions, fixed instruction length, more general purpose registers, load-store architecture and simplified addressing modes which makes individual instructions execute faster, achieve a net gain in performance and an overall simpler design with less silicon consumption as compared to CISC.RISC design ideally suited to participate in a powerful trend in the embedded Processor market - the "system-on-a-chip". The most common RISC microprocessors are ARM, SP ARC, MIPS and IBM's PowerPC. Some CPUs have been specifically designed to have a very small set of instructions – but these designs are very different from classic RISC designs, so they have been given other names such as minimal instruction set computer (MISC), or transport triggered architecture (TTA), etc. Despite many successes, RISC has made few inroads into the desktop PC and commodity server markets, where Intel's x86platform remains the dominant processor architecture .Outside of the desktop arena, however, the ARM architecture (RISC) is in widespread use in smartphone, tablets and many forms of embedded device. It is also the case that since the Pentium Pro (P6) Intel has been using an internal RISC processor core for its processors. While early RISC designs differed significantly from contemporary CISC designs, by 2000 the highest performing CPUs in the RISC line were almost indistinguishable from the highest performing CPUs in the CISC line[9].

1.2 Floating Point

In computing, floating point is the formulaic representation that approximates a real number so as to support a trade-off between range and precision. A number is, in general, represented approximately to a fixed number of significant digits (the significant) and scaled using an exponent in some fixed base; the base for the scaling is normally two, ten, or sixteen.



Floating-point operations are useful for computations involving large dynamic range, but they require significantly more resources than integer operations. A floating-point system can be used to represent, with a fixed number of digits, numbers of different orders of magnitude: e.g. the distance between galaxies or the diameter of an atomic nucleus can be expressed with the same unit of length. The result of this dynamic range is that the numbers that can be represented are not uniformly spaced; the difference between two consecutive represent able numbers grows with the chosen scale[9].

2. *LITERATURE REVIEW*

In literature review, review was done on low power, less delay and maximum operating frequency techniques related to RISC processor design. The various papers referred are as given below:

In 2016 Sarika U. Kadam, S.D. Mali, designed "Design of RISC Processor using VHDL". The proposed 16-bit RISC processor is designed using a parallel programming language called VHDL. It is simulated and synthesized using Xilinx ISE 13.1i. Pipelining is used to make processor faster. In Pipelining instruction cycle is divided into parts so that more than one instruction can be operated in parallel. Number of instructions are designed for this processors. Multiplier is also designed using ADD instruction. All instructions are simulated successfully. Simulation results show that the proposed processor is working correctly. The proposed processor has a delay of 4.744 ns and operating frequency of 210.775 MHz. When the proposed work compared with previous processors, it can be seen that proposed processor has less delay[1].

Swati Joshi, Sandhya Shinde, Amruta Nikam,"32-bit pipeline Risc Processor in VHDL using Booth Algorithm",. The aim of paper is to design instruction fetch unit and ALU which are part of RISC processor architecture. Instruction fetch is designed to read the instructions present in memory. ALU is in the execution stage of pipelining which performs all computations i.e.arithmetic and logical operations. Xilinx 8.1i is used to simulate the design using VHDL language .This paper proposes ALU which performs operations such as addition, subtraction, AND, OR, NOT, XOR etc. successfully. ALU provides correct results according to Opcodes and operands provided. ALU designed in this paper is used in execution stage of pipelined processor. Instruction fetch unit works correctly when provided with address it fetches correct instruction from memory. It is used to read instruction from memory which is the first step of pipelined processor. The designed fetch unit and ALU are used in pipelined RISC processor[2].

Vishwas V.Balpande ,Vijendra P.Meshram,Ishan A. Patilm,Sukeshini N.Tamgadem,Prashant Wanjari, "Design and Implementation of RISC processor on FPGA", In proposed paper 16-bit RISC processor is designed using VHDL programming. Four stage (viz. instruction fetch stage, instruction decode stage, execution stage and memory/IO - write back stage) pipelining is used to improve the overall CPI (Clock Cycles per Instruction). Hardwired control approach is used to design the control unit as against micro-programmed control approach in conventional CISC processor. Structural hazards are dealt with the implementation of prefetch unit, data hazards are dealt with forwarding and control hazards are dealt with flushing and stalling. The design is modeled and simulated using VHDL and then implemented on FPGA successfully. The maximum frequency of operation on the Xilinx's Spartan-II FPGA iS 26-MHz[3].

Soumya Murthy, Usha Verma, "FPGA based Implementation of Power Optimization of 32 Bit RISC Core using DLX Architecture," By using fetch, decode, ALU, comparator, GPR memory, execute, pipelined RISC processor core is developed using DLX architecture. Using low power
technique i.e. verilog HDL modification a lower version of the processor is designed to reduce power consumption of the core. Lower version of the processor is designed to reduce power consumption of the core. The overall optimization achieved from HDL technique is 13.33%[4].

Mohit N. Topiwala, N. Saraswathi, "Implementation of a 32-bit MIPS Based RISC Processor using Cadence," In this paper, design of 32-bit MIPS based RISC processor is implemented successfully with pipeline functionalities. Every instruction is executed in one clock cycle with 5-stage pipe lining. This design shows the implementation of MIPS based CPU capable of handling various R -type, J-type and I-type of instruction and each of these categories has a different format. These instructions are verified successfully through testbench. Designing Forwarding unit and

hazard detection unit to overcome the data dependencies was critical task and it was implemented successfully. The design is implemented using Verilog-HDL and synthesized using Cadence RTL complier using typical libraries of TSMC 0.18 urn technology. Design of MIPS processor is optimized both in timing and area. Also complete ASIC flow till RTL to GDS II have done using Cadence SoC Encounter, and analyzed the complete physical design flow[5].

Mrs. Rupali S. Balpande ,Mrs. Rashmi S. Keote, "Design of FPGA based instruction Fetch and Decode Module of 32-bit (MIPS) processor," Through analysis of function a d theory of RISC CPU instruction decoder module , they design instruction decoder (ID) module of 32-bit CPU by pipelining. Top-down design method and VHDL language is used for describing this paper. It is easy to edit and debug .Design of Instruction fetch (IF) stage simulates, integrate and route on Quartus II 4.3.The result indicates IF stage completes function[6].

3. PROPOSED DIAGRAM

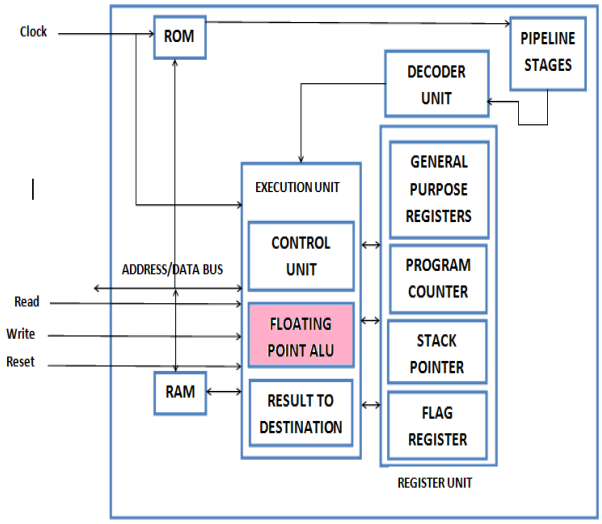


Fig-1: Proposed diagram of RISC processor with Floating Point.

4. *PROPOSED WORK*

To developed an processor based on RISC Architecture with

1. The instruction set.
2. The instruction formats.
3. The pipeline stages.

4.1 Instruction set

Instructions are more than 30.

4.2 Instruction formats

We have to assign different formats for certain instructions. This is because different instructions use different operands and hence different formats needed to be constructed for them. The following section describes four formats that are used.

a) Register Format (R-type)

b) Immediate Format (I-type)

c) Branch Type Format (J- type)

d) Input/ Output Format (I/O-Type)

4.3 Pipeline stages

Pipeline includes six stages: instruction fetch (IF), instruction decoder (ID), execution (EXE), memory/ IO (MEM), write-back (WB). Pipelining is a key feature of RISC in which processor works on different stages of instruction at the same time to execute more instructions in shorter time. The different stages of pipelines are instruction fetch, decode, execute memory and write back. Pipelining improves throughput by working on many operations at the same time. Different processors have a different number of stages of the pipeline. The length of pipeline depends on the longest stage. Pipelining gives high-performance processors.

a) Instruction Fetch(IF)

b) Instruction Decoder(ID)

c) Execution (EXE)

d) Memory and IO (MEM)

e) Write-Back (WB)

5. CONCLUSIONS

We will be designing the arithmetic unit of the RISC processor using pipelining approach. In the above reviewed papers of the MIPS (Multiprocessor Interlocked processing system) architecture is used for the fixed arithmetic values which will cause the error for the floating numbers. By the use of the floating point unit in

the CPU architecture the error will not happen. By using the R-type, I-type, J-type and I/O type of instruction sets the delay can be minimized,power consumption is optimized. As the delay is decreased the speed of the processor is undoubtedly increased. All the modules will be designed in Xilinx using VHDL language.

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