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A Single Switch High Gain Coupled Inductor Boost Converter

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Abstract-*A single switch high gain coupled inductor boost converter with closed loop control for low switch voltage stress. In this converter input energy acquired from the source is first stored in the magnetic field of coupled inductor and intermediate capacitor. In subsequent stages, it is passed on to the output section for load consumption. A passive clamp network around the primary inductor ensures the recovery of energy trapped in the leakage inductance, leading to drastic improvement in the voltage gain and efficiency of the system. Exorbitant duty cycle values are not required for high voltage gain, which prevents problems such as diode reverse recovery. Presence of a passive clamp network causes reduced voltage stress on the switch. This enables the use of low voltage rating switch (with low "on-state" resistance), improving the overall efficiency of the system. Closed loop simulation using PID controller of the converter is done with 40 V DC input and 400 W output power .*

Key Words: Coupled inductor, high voltage gain, passive clamp, switched capacitor.

1.INTRODUCTION

In recent years, the boost dc/dc converters have been widely used to step up the renewable energy sources in various industrial applications such as ESS,UPS,EV etc. In those applications, a boost dc/dc converter generally step up the voltage to the high voltage output. For that reason , to obtain a high voltage gain, many converter topologies were reported[3]-[6] for this application.

Direct voltage step up using high frequency transformer is a Simple and easily controllable converter providing high gain. Isolated current fed dc-dc converters[7]-[9] are example of this category. However, these topologies result in high voltage spikes across the switch (due to leakage inductance) and large ripple in primary side transformer current as the turns ratio in the high frequency transformer increases. Most of the nonisolated high voltage gain dc–dc power converters employ coupled inductor (to achieve higher voltage gain)[11] in contrast to a high frequency transformer used by the isolated versions . The coupled inductor-based dc–dc converter has advantages over isolated transformer-based dc–dc converter in minimizing current stress, using lower rating components and simple winding structure. Modeling procedure of the coupled inductor is described in [12]. For high power converter applications, interleaved coupled inductor-based boost converters [13]–[15] have also been proposed .

Voltage gain of the converter can be increased without increasing the duty cycle of the switch by connecting an intermediate capacitor in series with the inductor [6]. The intermediate energy storage capacitor with coupled inductor charges in parallel and discharges in series with the coupled inductor secondary.

A demerit of coupled inductor-based systems is that they have to deal with higher leakage inductance, which causes voltage spikes across the main switch during turn-OFF time and current spike during turn-ON time, resulting in a reduction of the overall circuit efficiency. The effects of leakage inductance can be eliminated by using an active clamp network shown in [9], which provides an alternate path to recover leakage energy. But active clamp network is not as efficient as a passive clamp because of conduction losses across the power switch of the active clamp network. Active clamp network consists of a switch with passive components while passive clamp network [4] consists of passive components such as diode, capacitor, and resistor. The passive clamp circuit is more popular to reduce voltage stress across the converter switch by recycling leakage energy.

To overcome such disadvantages of the conventional converters ,In this paper, we propose coupled inductor boost converter that features low switch voltage stress and high gain. To achieves high voltage through a coupled inductor connected in interleaved manner that charges an intermediate buffer capacitor and a passive clamp network to recover the leakage energy. Coupled inductor leads to the incorporation of "turns ratio" into the gain expression that leads to high efficiency without increasing the duty ratio. As compared to existing high-gain dc–dc converters, the number of passive components used in the proposed converter is less, which reduces the cost and improves the efficiency. Though the proposed converter is applicable to any low voltage source applications such as solar PV, fuel cell stack, battery, etc

2. A SINGLE SWITCH HIGH GAIN BOOST CONVERTER

The proposed converter is shown in Fig. 2.1. It is clear from Fig. 2.1 that the proposed converter consists of one passive clamp network, a coupled inductor(L1,L2),and an

intermediate capacitor apart from other components. The symbol V_{PV} represents the PV voltage applied to the circuit. S is the main switch of the proposed converter. The coupled inductor's primary and secondary inductors are denoted by L1 and L2. C1 and D1 represent the passive clamp network across L1.The capacitor C_0 is the output capacitor while D_3 is the output diode. The voltage V_0 is the average(dc)output across the load.

The intermediate energy storage capacitor C_2 and the feedback diode D_2 are connected on the secondary side.

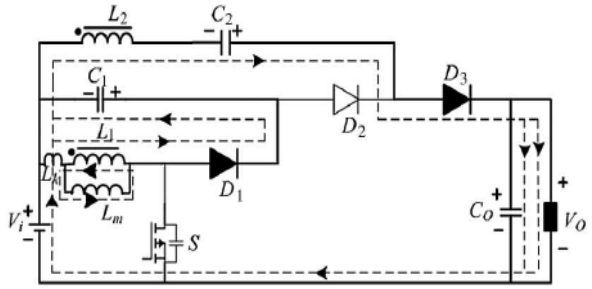

Fig 2.1. Circuit Diagram of Proposed Converter

3.MODES OF OPERATION

There are mainly five operating states for this converter.

3.1 Mode 1 [t0 – t1]: The switch (S) is turned ON at the start of the converter operation. The current flows through the switch and the primary side of the coupled inductor (L1), energizing the magnetizing inductance (Lm) of the coupled inductor. The current path is as shown in Fig. 3.1. The two diodes D1 and D3 are reverse biased, while D2 is forward biased during this mode. The intermediate capacitor C2 is charged through D2 by L2 and capacitor C1. If voltage across intermediate capacitor (C2) becomes equal to the summation of voltages across L2 and C1, diode D2 turns OFF.

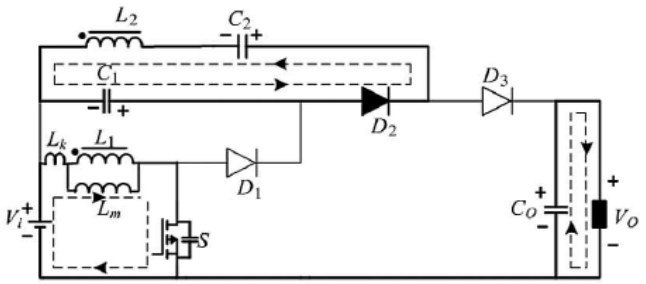

Figure 3.1 Mode 1

3.2 Mode 2 [t1 – t2]: This mode begins by turning OFF the main switch *S*. The parasitic capacitance of the switch *S* is charged by the magnetizing current flowing through the inductor *L*1. The diode *D*2 remains forward biased and current continues to flow through this. Current path in this mode is shown in Fig.3.2.

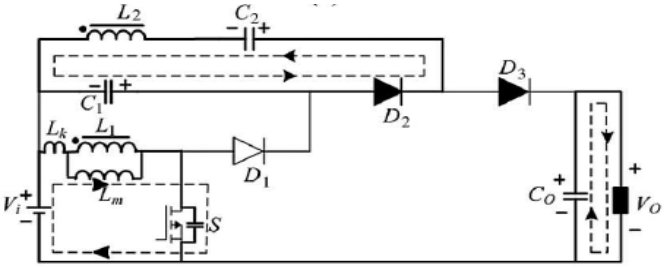

Figure 3.2 Mode 2

3.3 Mode 3[t2 – t3]: In this mode, diodes *D*1 and *D*3 become forward biased. *D*2 is reverse biased and its current becomes zero in this mode. The leakage energy stored in the primary side of the coupled inductor (*L*1) is recovered and stored in the clamp capacitor (*C*1) through *D*1. Also, the energy is transferred from the input side to the output side through diode *D*3 as shown in Fig.3.3.

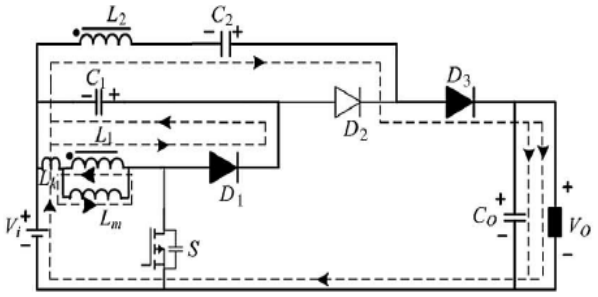

Figure 3.3 Mode 3

3.4 Mode 4 [t3 – t4]: This mode begins after the completion of recovery of the leakage energy from inductor *L*1. The diode *D*1 now becomes reverse biased while diode *D*3 remains forward biased in this mode. The current flows from the input side to the output side to supply the load as shown in Fig.3.4.

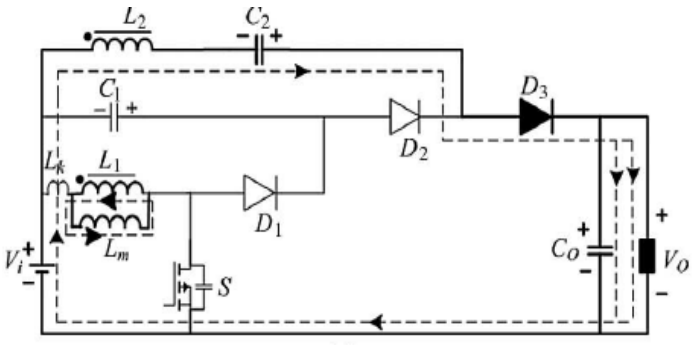

Figure 3.4 Mode 4

3.5 Mode 5 [t4 – t0]: This mode begins by turning ON switch *S*. The leakage inductor energizes quickly using the full magnetizing current while the parasitic capacitance across the switch discharges in this mode. The two diodes *D*1 and *D*2 are in reverse biased condition. The current flow path in this mode is shown in Fig.3.5. This mode ends when diode *D*3 becomes reverse biased and current flow through inductor *L*2 changes direction.

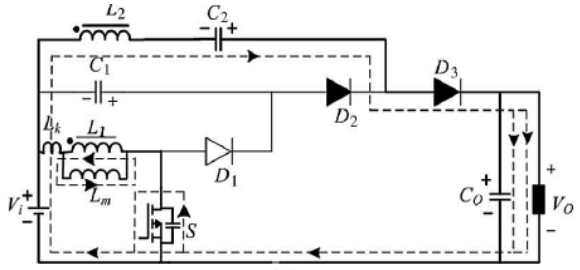

Figure 3.5 Mode 5

4.THEORETICAL WAVEFORM

The Fig 4.1shows the key operating waveforms of the proposed converter. Each switching period is subdivided into five modes and their operational modes are shown in above Figures.

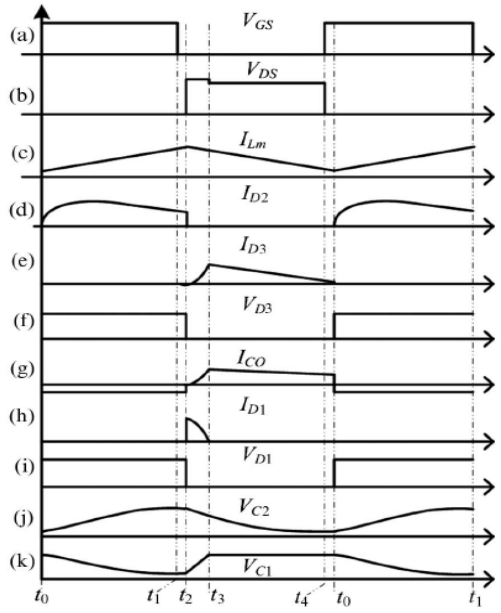

Figure 4.1 waveform of proposed converter in continuous conduction mode

5.DESIGN

When switch S is ON: The voltage across L1 is given by

$$VL1(ON) = Vi \quad (5.1)$$

The voltage across L2 is given by

$$VL2 = Vc2 - Vc1 \quad (5.2)$$

$$VL2 = n\,Vi \quad (5.3)$$

When switch S is OFF: The voltage across L1 is given by

$$VL1OFF = -VC1 \quad (5.4)$$

Applying Kirchoff's voltage law in Mode 3 yields

$$VL2 = Vi + VC2 - V0 \quad (5.5)$$

By substituting VC2 from (5.3) and (5.4) into (5.5), it becomes

$$VL2 = Vi - VL1OFF + nVi - V0 \quad 5.6)$$

Also,

$$VL1 = \frac{VL2}{n} \quad (5.7)$$

By substituting (4.6) into (4.7), voltage expression during switch OFF condition becomes

$$VL1(OFF) = \frac{(Vi + nVi - V0)}{n+1} \quad (5.8)$$

Voltage gain: By applying voltage-sec balance across L1,

$$VL1(ON)d+VL1(OFF)(1-d) =0 \qquad (5.9)$$

Substituting values of VL1(ON) and VL1(OFF) from (5.1)and (5.8), respectively, into (5.9) yields

$$V_{id}+\frac{(Vi+nVi-VO}{n+1}(1-d) \quad =0 \qquad (5.10)$$

Voltage gain,

$$\frac{VO}{Vi} =\frac{(n+1)}{(1-d)}$$

The components are designed based on the assumption that all components are ideal, voltage gain ratio is,

$$\frac{V0}{Vi} =\frac{(n+1)}{(1-d)}$$

The minimum value of the clamp capacitor C_1,

$$C_1 = \frac{I_m d_{lk}}{\Delta V_{C1} f_s}.$$

The minimum value of the Intermediate Capacitor C_2,

$$C_2 = \frac{I_m d}{n\Delta V_{C2} f_s}.$$

The minimum value of the Output Capacitor C_0,

$$C_o = \frac{I_o d}{\Delta V_o f_s}.$$

6.SIMULATION RESULTS

The closed loop Simulation of the above converter is done in MATLAB simulink using 40 V input and 400 V, 400 W output at 50 KHZ frequency. The Parameters used in Simulation are shown in Table 1

Table 1. Parameters Used in Simulation

Parameters	Values
Input Voltage	40V
Output Voltage	400V
Output Power	400W
Output Current	1A
Frequency	50Khz
Turns ratio of coupled inductor(n)	4
Clamp Capacitor C1	1µF
Intermediate Capacitor C2	47µF
Output Capacitor C0	2.5µF
Load Resistor R	400Ω

The closed loop simulation diagram of the proposed converter is shown below.

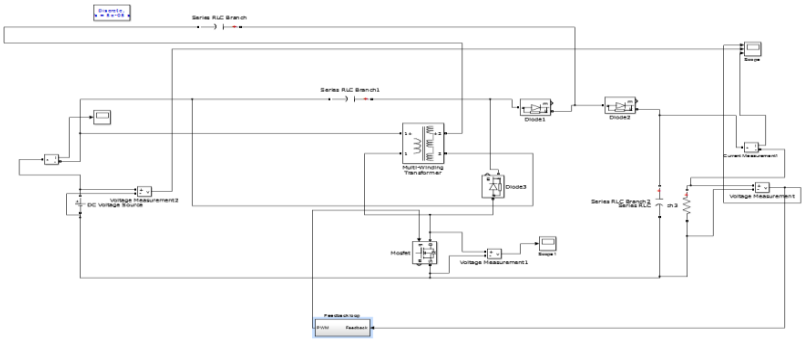

Fig 6.1 Closed Loop Simulation Diagram

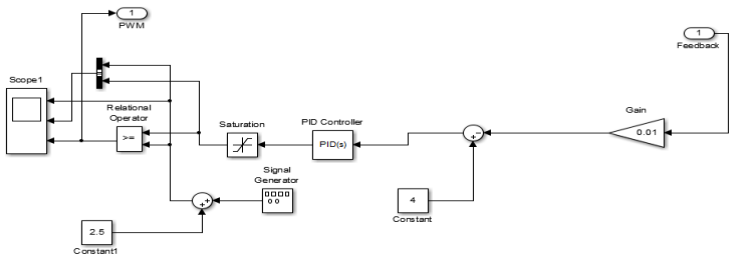

Figure 6.2 closed loop feedback of proposed converter

The simulation output waveform of proposed converter is shown below . The output voltage(400V),input voltage(40V) and Output current(1A)

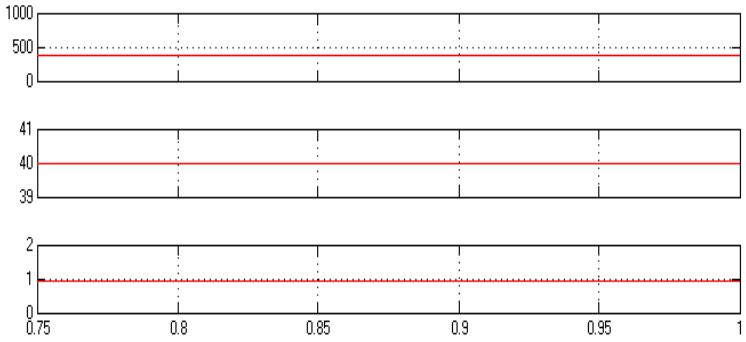

Fig 6.3 Output Voltage, Input Voltage and Output Current

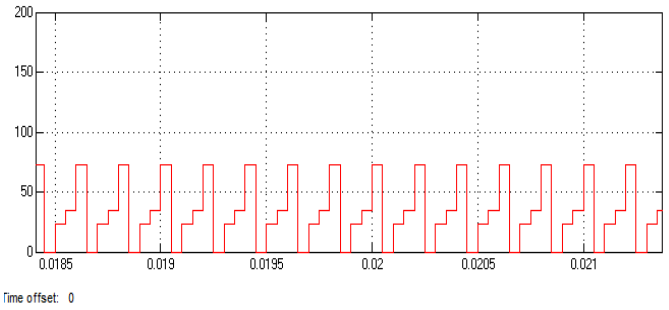

Fig 6.4 Voltages stresses across switch

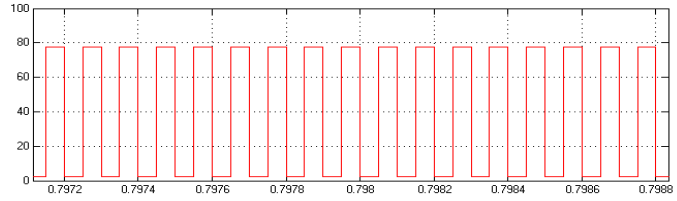

Fig 7 Voltages stresses across Diode D1

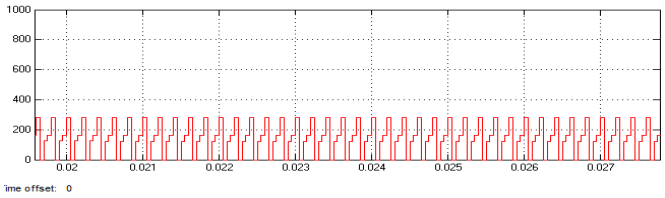

Fig 7 Voltages stresses across Diode D2

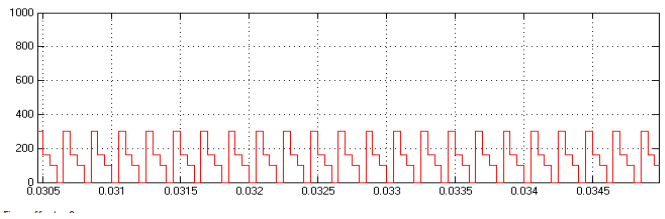

Fig 7 Voltages stresses across Diode D3

6. CONCLUSIONS

In this paper, single switch high gain coupled inductor boost converter has been proposed. In the proposed converter high voltage gain is achieved without using extreme duty cycle values, which is a big advantage over conventional step up converters and also obtained low voltage across the switch . The operation principles and relevant analysis of the proposed converter are presented in this paper.

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