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Review On Design Of Low Power Multiply And Accumulate Unit Using Baugh-Wooley Based Multiplier

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Abstract - *Multiply-accumulator (MAC) is the central unit used in digital signal processors (DSP) that are now widely found in many consumer electronic devices. MAC unit performs multiplication and accumulation process. Basic MAC unit consists of multiplier, accumulator, adder. Power consumption and low delay are important design in many digital signal processing application. This paper presents a low power pipelined MAC architecture that incorporates a 32 bit multiplier using Baugh-Wooley algorithm and carry look- ahead adder. The Baugh-Wooley multiplier is faster than the other multipliers like Array multiplier, Wallace tree multiplier, Booth multiplier.*

Key Words: **Digital Signal Processing (DSP)1, Multiply and Accumulate (MAC) unit2, Verilog HDL3, Xilinx4 etc.**

1. INTRODUCTION

In Digital Communication, DSP is an important block which performs several digital signal processing application such as Convolution, Discrete Cosine Transform (DCT), Fourier Transform and so on. Every digital signal processor contain MAC unit. Filters, channel estimation require FIR or FFT/IFFT computations that can be accelerated by MAC units. In addition to it, MAC units are used to realize non-linear function like discrete cosine transform (DCT) or discrete wavelet transform (DWT) which consist of repetitive multiplication & addition.MAC unit always lies in critical path, it determines the speed of the overall system and hence, High speed MAC is vital for real time DSP application. The critical demand for low power system requires a power efficient MAC unit. Many researchers have been focusing on the design of advance MAC unit architecture. The MAC operation is the main computational operation in all digital designs. The speed of the processor mainly depends on the speed of the MAC unit. Development of high speed and low power MAC structure is thus very important for real time processing. The generic MAC architecture consists of a conventional multiplier, adder and an accumulator as shown in following diagram.

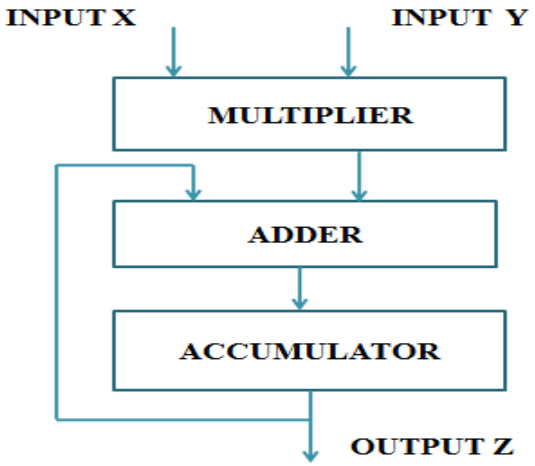

Fig-1: Block diagram of MAC unit

Where output is added to the previous MAC output result by an accumulate adder. The multiply-accumulate unit computes the product of two numbers and add that product to an accumulator.

Multiplication is an important arithmetic operation and multiplier implementations date several decades back in time. Multiplications were originally performed by iteratively utilizing the ALU's adder. As timing constraints became stricter with increasing clock rates, dedicated multiplier hardware implementations such as the array multiplier were introduced. Since then ever more Sophisticated methods on how to implement popular implementations is that of the modified- Booth recoding scheme together with a logarithmic-depth reduction tree and a fast final adder. Modified-Booth recoding has the advantage of reducing the number of generated partial products by half, compared to partial-product generation based on 2- input AND-gates. This fact decreases the size of the reduction circuitry, which commonly is a logarithmic-depth reduction tree, e.g. Wallace, Dadda or TDM. Since such reduction trees are infamous for their irregular Structures, which make them difficult to place and route during the physical layout of a multiplier, a decreased size of the reduction circuit eases and route during the physical layout of a multiplier, a decreased size of the reduction circuit eases the implementation and improves the performance of the multiplier. The multiplier is the major bottleneck that determines the performance of MAC unit. Over the years, a wide range of multiplier algorithms and design techniques have been developed to reduce the multiplier delay. A widely used multiplier implementation is the modified-booth algorithm (MBA) together with a logarithmic depth reduction tree and a final adder. Radix-4 MBA and parallel architecture MBA were later introduced for high-speed multiplication. Due to its high power dissipation, MBA multiplier is not a good choice for implementing a low power MAC unit. Another popular multiplier algorithm is Baugh-Wooley (BW) which is more power and energy efficient than MBA multiplier of equal bit width.
Another way to increase the multiplier's performance on throughput is to minimize the critical path delay by inserting an extra pipeline register, either inside the PP unit or between the PP unit and final adder.

Multiplier is the most commonly used building block in digital signal processing (DSP) applications such as finite impulse response (FIR) filters, discrete cosine transform (DCT), wavelet transforms and fast Fourier transforms (FFTs). Most of these DSP applications require efficient and low-error fixed-width multipliers, in which the bit-width size of the inputs and product is the same. A fixed-width multiplier generates only the most significant product bits which results in truncation errors. This error has to be compensated either by a constant compensation bias or an adaptive error compensation bias. Several multiplication algorithms and architectures have thus been developed in the recent years. Two of the most commonly used multipliers are Booth and Baugh-Wooley. However, Baugh-Wooley is preferred for multiplication of signed numbers, multiplications have been proposed. One of the more represented in 2's complement format. Fixed width Baugh-Wooley multipliers are fast and consume less area and power.

2. LITERATURE REVIEW

Maroju SaiKumar & D. Ashok Kumar et. al. in paper entitled "Design and Performance Analysis Of Multiply-Accumulate(MAC) Unit" presents MAC unit model which is designed by incorporating the various multipliers such as Array multiplier, Ripple carry multiplier with row bypassing technique, Wallace multiplier, and DADDA multiplier. Performance of the MAC unit is analyzed in terms of Area, delay and power. Proposed MAC unit model (DM+CSA+Acc) achieves better performance in terms of area and delay compared to that of existing model. However, there is slight increase in the power. The performance analysis of MAC unit models is done by designing the models in verilog HDL. Then MAC unit models are simulated and synthesized in Xilinx ISE 13.2 fir Virtex-6 family 40 nm technology. [1]

Thirumala Rao V., Girish Gandhi S. & Leela Mohan C. et. al. in paper entitled "Performance Evaluation of Parallel Multipliers for High Speed MAC Design" they had Presents the implementation of high speed Signed & Unsigned fast Multipliers and their comparative analysis. Proposed architecture for widely used parallel multipliers such as Booth multiplier, Wallace multiplier and DADDA Tree multiplier in order acquire their design attributes like Speed, area. The MAC implemented using the Wallace Multiplier has least delay as compared to others. The acquired design parameters of the multipliers are analyzed to design optimum speed multiply and Accumulate (MAC) unit for multimedia application like Filters, Synthesizers, Wireless communication channels etc. finally the designed multiplier has also been applied to DSP application like convolution nand their performance is analyzed in terms of area.[2]

P.A. Irfan Khan & Ravi Shankar Mishra et. al. in paper entitled "Comparative Analysis of Different Algorithm for Design of High-Speed Multiplier Accumulator Unit(MAC)" In this paper Baugh-Wooley multiplier is implemented for improving the performance of MAC unit. Baugh-Wooley multiplier is faster than Array multiplier, Wallace Tree multiplier, and Booth multiplier. Baugh–Wooley multiplier is implemented using in 180nm technology in cadence virtuoso. It reduces partial product

to MAC unit. The Baugh–Wooley multiplier faster than Wallace tree multiplier.the MAC unit Baugh–Wooley multiplier is implemented using 180nm technology cadence virtuoso. The power consumption of the MAC unit using Wallace tree multliplier is 2.265mW and with Baugh–Wooley multiplier is4.628mW. [3] Kandimalla Rajaneesh & M. Bharathi et. al. in paper entitled "A Novel High performance Implementation of 64 Bit MAC Units and Their Delay Comparison" they had implemented A Novel High performance 64 bit MAC. The MAC unit is designed using Vedic, Braun, Dadda multiplier and carry save adder hence compared with performance of Wallace multiplier and carry save adder. In gate level Verilog hdl used for coding digital circuits using tool Xilinx ISE 10.1 I and target family Spartan 3E, Device-XC3S500,speed-5,package:FG320. The synthesized for the proposed digital circuits. [4]

Magnus Sjalandar & Per Larsson-Edefors et. al. in paper entitled "High –Speed and Low –Power Multipliers Using The Baugh-Wooley Algorithm And HPM Reduction Tree" suggest Baugh-Wooley algorithm with High Performance Multiplier (HPM) reduction tree. The modified-Booth algorithm is extensively used for high-speed multiplier circuits. Once, when array multipliers were used, the reduced number of generated partial products significantly improved multiplier performance. In designs based on reduction trees with logarithmic logic depth, however, the reduced number of partial products has a limited impact on overall performance. The Baugh-Wooley algorithm is a different scheme for signed multiplication, but is not so widely adopted because it may be complicated to deploy on irregular reduction trees. They show for range of operator bit widths that when implemented in 130nm and 65nm process technologies, the Baugh-Wooley multipliers exhibit comparable delay, less power dissipation and smaller area than MB multipliers. [5]

Rakesh Warrier,C.H.Vun & Wei Zhang et. al. in paper entitled "A Low-power Pipelined MAC Architecture using Baugh-Wooley based multiplier" proposes a low power pipelined MAC architecture that incorporates 16x16 multiplier using Baugh –Wooley algorithm with high performance multiplier tree, together with clock gating the idle pipeline stages to reduce the power consumption. The power consumption of the proposed architecture is 30% to 80% less than the other contemporary MAC architecture, without compromising its computation performance. Authors proposed a high speed and energy-efficient 2-cycle MAC architecture. Proposed MAC-NEW has 37% and 23% less energy than MAC-2C and MAC-3C, respectively. Proposed 2-c architecture faster and area and energy efficient than a conventional 2-cycle MAC unit. [6]

Tung Thanh Hoang, Magnus Sjalander, and Per Larsson-Edefors et. al. in paper entitled "High-Speed ,Energy –Efficient 2-Cycle Multiply-Accumulate Architecture" they propose high-speed and energy 2-cycle MAC architecture. Their architecture is based on two's complement representation, it used guarding bits to efficiently support longer MAC loops, and it includes output saturation. By performing carry propagation only in second stage of the MAC pipeline, multiplication and accumulation have similar delays. But in contrast to previous MAC architectures that propose to only use one carry propagation stage, architecture requires no extra cycle to produce the final result. Instead it correctly produces the sum of the accumulated value and the product in each cycle. [7]

Table -1: overall analysis 8-bit of MAC unit

Comparison table shows the comparison of various approaches of designing the multiply and accumulate unit. Analyzed the performance based on the parameter such as area, delay and power.

For 8 bit				
DESIGN	PROCESS	AREA (NO. OF BIT SLICES)	DELAY (NS)	POWER (W)
Existing MAC unit model (MRBM+CSA+ACC) [1]	40nm	137	6.712	1.010
Proposed MAC unit model(1) (AM+CSA+ACC) [1]	40nm	97	8.175	1.067
Proposed MAC unit model(2) (RCAM RB+CSA+ACC) [1]	40nm	92	6.712	1.261
Proposed MAC unit model(3) (WTM+CSA+ACC) [1]	40nm	96	6.102	1.061
Proposed MAC unit model(4) (DM+CSA+ACC) [1]	40nm	103	3.6592	2.142

MAC using Booth[2]		208	2.143	
MAC using WALLACE[2]		112	1.821	
MAC using DADDA [2]		113	2.143	
MAC using Baugh-Wooley Multiplier [3]	180nm		10.09	0.0027
MAC using Wallace tree Multiplier [3]	180nm		10.68	0.0013

Table -2: overall analysis of 16-bit MAC unit

For 16 bit				
Design	Process	Area (um2)	Power (uW)	delay(ns)
Proposed 2C-MAC [6]	65nm	10730	780.4	1.71
MAC-2C [7]	65nm	12937	6900	1.91
MAC-3C [7]	65nm	13711	10300	1.312
MAC-NEW [7]	65nm	12014	8200	1.312
MAC-2C [7]	90nm	9119	1146.8	2.784
Combined MAC [8]	90nm	8714	1259.6	2.433
Proposed MAC [8]	90nm	8925	905.6	2.572

Table -3: overall analysis of 32-bit MAC unit

For 32 bit				
Design	Process	Area (um2)	Delay (ns)	Power (Mw)
VEDIC [4]	-	-	31.835	-
DADDA [4]	-	-	35.372	-
BRAUN [4]	-	-	35.444	-
WALLACE [4]	-	-	40.643	-
BAUGH [5]	65nm	45.1K	2.59	23.4
BOOTH [5]-+	65nm	52.1K	2.50	37.5
BAUGH [5]	130nm	88.8K	3.63	7.81
BOOTH [5]	130nm	108.9K	3.68	9.74

3. CONCLUSIONS

The review on papers shows different approaches of designing the MAC unit. Performance is analyzed based on the parameters such as area, delay, power. For 8 bit MAC, Baugh-Wooley Multiplier has increased delay and power is very low as compared to other techniques. For 32 bit MAC using Baugh-Wooley with HPM reduction exhibit comparable delay, less power dissipation and smaller area than Modified Booth multiplier. For 16 bit MAC, Proposed 2C-MAC has less power and less delay. By using Baugh-Wooley Multiplier the delay has been reduced .And if pipelining technique used the power consumption also very less as compared to other multiplier techniques.

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