Design of Low Power Reconfigurable IIR filter with Row Bypassing Multiplier

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Abstract - *There are two main concerns for the efficient filter implementation they are reconfiguration and less power consumption. In this paper, two new high-speed and Low power reconfigurable Hilbert transformer designs have been introducing. They are carry save adder (CSA) and ripple carry adder (RCA) based row bypassing multipliers. The less power consumption occurred by turning off the adders when the multiplier operands are zero. Additionally, the delay time can be reduced by implementing the proposed Hilbert transformers along the parallel architecture of multipliers. Arbitrary coefficients are used to reconfigure these designs dynamically but are restricted to their length and word size. The execution of both the designs is assessed as far as the range (number of cuts/slices) and speed. The outcomes portray that the CSA row bypassing multiplier based Hilbert transformer accomplishes 17% expansion in speed and 13% area lessening in comparison with RCA row bypassing multiplier based Hilbert transformer. The power dispersal of the later transformer is not as much as the previous one.*

***Key Words*: FPGA, Hilbert transformer, IIR digital filters, row bypassing, carry save adder, ripple carry adders**

I. INTRODUCTION

Rapid technological change has forced manufacturing to face a new economic objective: re configurability, i.e., the ability of reconfigurable figuring of a framework, so its conduct can be changed by reconfiguration. Today or in future digital systems there is another vital issue is the utilization of power. For a long battery life in versatile devices, for example, medical devices, low power utilization is required. Research is now focused on low power reconfigurable realizations of digital filters with the (SDR) software-defined radio technology, digital signal processing, and biomedical engineering. Recently in the literature, many digital filters like reconfigurable finite impulse response (FIR) have been proposed in the literature. It is realized that the FIR Filter expends more computational power contrasted with an unending drive reaction (IIR) filter with comparative sharpness or selectivity, especially when low recurrence shorts are required. The realization of IIR filter has an advantage when compared to the realization of FIR filter in a number of coefficients and statistical performance. In our paper, we have used one of the known IIR filter structure, i.e., Direct form II for the acknowledgment of Hilbert transformer.

The Hilbert transformer is considered as an important in the processing of a signal. It has many applications in various fields like digital communication where it is utilized for modulation, edge detection of single side-band signals and digital images. Earlier the digital filters of FIR and IIR based Hilbert transformers are developed using various approaches such as the Remez exchange algorithm, Eigen filter method and weighted least square method. Different approaches for executing the Hilbert transformer were additionally examined which includes switched-capacitor usage, neural system, and multiplier-less triangular exhibit. In any case, it is watched that these methodologies are reasonable for the fixed coefficient applications. The FPGA execution of quick Fourier change (FFT) based Hilbert change is exhibited. In spite of fact that these filters are not reconfigurable in nature the current situation, re configurability is requested. This issue is managed in this paper. Keeping in mind the end goal to design a low power reconfigurable one should concentrate on multipliers to make them productive as these are the most power taking components. Consequently, by diminishing the power utilization in multipliers a huge power can be saved. In a logic circuit, the power scattering can be recognized as static and dynamic power dissipation. The static power utilization is corresponding to the number of transistors utilized. While the dynamic power scattering relies on charging and releasing of load capacitance. The normal dynamic power dissipation equation of a CMOS gate

$$P_{avg} = \frac{1}{2}CfV_{dd}^2N$$

(1)

Where C is the capacitance of a load, Vdd is the supply voltage, f is the frequency of the clock, and N is switching activity of a clock cycle. The consumption of power can be reduced by reducing the switching activity without changing its logic circuit function.

The reconfigurable Hilbert transformers designs are proposed which are based on low power, row bypassing multipliers. These are designed using two multipliers. The multiplier design uses carry save adders and a final ripple

carries adder for its implementation. While the multiplier is based on the only ripple carry adders. The filter coefficients are directly saved into look-up-table (LUT). Multiplier accesses these coefficients. These designs are executed on Vertex-IV FPGA (field programmable gate array) board. The speed determines the performance in terms of the number of slices (area), frequency, and power usage.

The application where the coefficients of filter require change then Hilbert transformer can be utilized various fields like communication systems. The paper is structured as follows. The paper includes different sections which describe different concepts. The explanation of basics of Hilbert transformer described in section II. The types and methods of bypassing multipliers are described in section III. In Section IV, The implementation of FPGA of HT (Hilbert transformer) is explained. Example of design processes and results are compared in this section V. presented. In section VI, the total summary and conclusion are described.

2. HILBERT TRANSFORMER

We already know that there exists a relation between the discrete HT (Hilbert transformer) and complex half-band filter. The Hilbert transformer's frequency domain constraints were satisfied by complex half-band filter. The ideal Hilbert transformer response (frequency response) is defined as

$$H_{HT}(e^{j\omega}) = \begin{cases} j, & -\pi < \omega < 0 \\ -j, & 0 < \omega < \pi \end{cases} \quad (2)$$

The complex half-band filter can capacitance. by adding a shift of π /2 radians in the real half-band filter's frequency response. The G(z) of real half-band filter can be represented as

$$G(z) = \frac{1}{2}[A_1(z^{-2}) + z^{-1}A_2(z^{-2})] \quad (3)$$

Where A1 (z) and A2 (z) represents are stable all-pass filters. The complex half-band filter occurs from half-band filter on application of transformation such as frequency using

$$H(z) = jG(-jz) \quad (4)$$

The resultant complex half-band transfer function is expressed as

$$H(z) = \frac{1}{2}[A_1(-z^{-2}) + jz^{-1}A_2(-z^{-2})] \quad (5)$$

A1(−z−2) and A2(−z−2) defined as a real and stable all-pass filter. By applying the frequency transformation on G(z) which is called half-band low pass filter and have its pass band on the right half of the unit circle converts to the complex half-band filter H(z) with its pass band on the upper half of the unit circle . The realization of complex half-band filter which uses the all-pass filter is shown in Fig. 1.
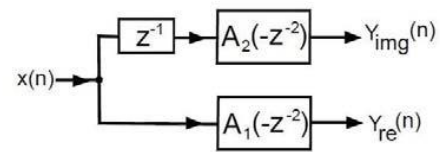

Fig. 1. Complex half-band filter realization using Allpass filter

In order to get the canonical form the direct form II structure of the all-pass filter is placed in the block of the all-pass filter in filter realization of complex half-band to Hilbert transformer. In realization of canonic structure, mainly the filter coefficients are multiplier coefficients. The required number of coefficients for the realization of the Nth order IIR filter are 2N + 1 using canonic structures.

3. LOW POWER MULTIPLIER WITH ROW BYPASSING

The usage power by a multiplier can be lowered by making the components off with the help of multiplexers when the operands of the multiplier are 0's. In conventional DSP applications, the multiplier operands are major with the zero input operands and have a percentage of 73.8. Therefore, to decrease power and increase in speed, row bypassing approaches are used in multipliers. These designs can be made by bypassing multipliers using carry save adders and ripple carry adders defined as follows.

3.1 Row bypassing multiplier based on CSA

If the yj bit is 0 (Zero) in the multiplier then adders should become inactive at the jth row which can be done by row bypassing multiplier i.e., all the bits in the xi.yj, $0 \le i \le n - 1$, should be zero, where n is represented as operand's word length. Hence, the low power can be obtained. The conventional full adder is to be modified in to turn off the adders of a particular row as shown in Fig. 2.
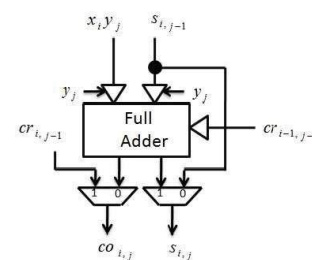

Fig. 2. Modified full adder cell

Tri-state buffers have 3 inputs they are xi, yj, and cr and the outputs are si,j and co i,j. It uses two multiplexers at the outputs to perform bypassing approach. Tri-state buffer decides to make the adders inactive when multiplier bit yj is zero. The multiplexers select correct outputs. The input vectors coefficients of Hilbert transformer might be positive or negative so we have to use the signed multiplier. So an 8 ×

8 signed Braun multiplier is used by modifying the adder cell shown in Fig. 2.

3.2 RCA based row bypassing multiplier

Row bypassing of RCA based multiplier is designed. Basically, the adder cell consists of 2 inputs and one output. So, only two tri-state buffers are used to inactive the adder's operation if the bit yj is zero in the multiplier operand. When compared to CSA only one multiplexer is required to select accurate output. Carry-save adders are faster when slow compared to carry save adders because of the longer critical path. Hence, speed can be increased by a parallel architecture of an 8 × 8 signed multiplier which is implemented using two 8 × 4 multiplier blocks. The block diagram of 8 × 8 multipliers is shown in Fig. 3. The Hilbert transformer is designed by 8 × 8 signed multiplier and utilized in this paper.
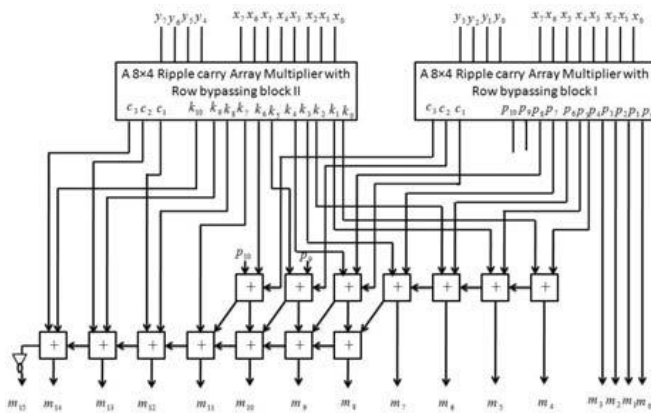

Fig. 3. Block diagram of 8 × 8 signed row bypassing multiplier using carry save adders

4. FPGA IMPLEMENTATION

The Hilbert transformer structure depicted in Fig. 1 has been actualized in two ways: utilizing CSA and RCA row bypassing based multipliers are determined in the above section. The coefficients are straightforwardly spared into LUT to make the operation speedier. One more preferred standpoint of putting away the coefficients into LUT is that similar coefficients need to spare just once and can be brought the same number of times they are required. Consequently, the less number of memory areas might be required to store coefficients. The proposed plans can be progressively reconfigured with subjective coefficients that are just constrained by their length and word estimate. The structures of Hilbert transformer are coded in Verilog HDL dialect. These structures are tried applying diverse information test vectors. An outline case of Hilbert transformer is considered in the accompanying area.

5. DESIGN EXAMPLE

In this section, the usage of Hilbert transformer is appeared by an illustration. The direct form II structure of a Hilbert transformer is executed on Xilinx Vertex FPGA. The FPGA is customized utilizing a mix of-of Xilinx core generation and Verilog (HDL) code. The info signals (input signal) are the parallel sources of info, worldwide clock, and a reset.

The determinations of real half-band filter are as per the following: stopband edge recurrence (frequency), $\omega s = 0.6\pi$ and stopband ripple, $\delta s = 0.016$. For these specifications, the transfer function of the real-half band filter is represented by

$$H(z) = \frac{1}{2}\left[\left(\frac{0.236471021 + z^{-2}}{1 + 0.236471021z^{-2}}\right) + z^{-1}\left(\frac{0.7145421497 + z^{-2}}{1 + 0.7145421497z^{-2}}\right)\right] \quad (6)$$

The resultant complex half-band filter transfer function is acquired by applying frequency transformation,

$$H(z) = \frac{1}{2}\left[\left(\frac{0.236471021 - z^{-2}}{1 - 0.236471021z^{-2}}\right) + jz^{-1}\left(\frac{0.7145421497 - z^{-2}}{1 - 0.7145421497z^{-2}}\right)\right] \quad (7)$$

Where

$$A_1(-z^{-2}) = \frac{0.236471021 - z^{-2}}{1 - 0.236471021z^{-2}}$$

and

$$A_2(-z^{-2}) = \frac{0.7145421497 - z^{-2}}{1 - 0.7145421497z^{-2}}$$

Direct form II acknowledgment (realization) of Hilbert transforms for given case is shown in Fig. 5.5.1 and its magnitude response is portrayed in Fig 5.5.2. The execution of Hilbert transformer exhibited in the illustration is actualized with the two bypassing multipliers and looked at in Table I as far as deferral (least period or delay), speed (most extreme recurrence/frequency) and dynamic power dispersal. The hardware usage of the two methodologies is abridged in Table II.
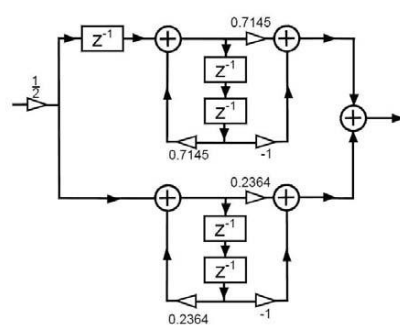

Fig. 4. Direct form II realization of Hilbert Transformer

The similar outcomes demonstrate that the power dissemination of CSA row bypassing based Hilbert transformer is 65% greater than RCA row bypassing based Hilbert transformer. The reason is all more exchanging

action or switching activity associated with the previous transformer as the number of multiplexers is almost double to the later. Though, the base time frame is diminished by 14.5% and maximum extreme recurrence is enhanced by 17% in CSA row bypassing based transformer. In this way, there is a trade-off amongst speed and power scattering. Essentially, from Table II, it is watched that range (cuts/slices) required for CSA bypassing multiplier based transformer is 13% less contrasted with the second transformer outline. The decision of the plan can be made by the application. For correlation of the speed and area of the RCA and CSA row bypassing based multipliers, numerous irregular input samples are connected in test bench and comparing comes about being watched.

The execution of the digital filters relies upon the value of channel coefficients and input samples, as the quantity of nonzero bits in coefficients expands, the hardware and power dispersal may differ. Consequently, in this work, the power, speed, and zone are considered as a normal of the combination as an average and brings about every synthesis results of the tables. For different illustrations, the examination consequences of the speed, zone, and power dispersal may change as indicated by the number of non-zero coefficient bits. Consequently, the power, speed and range estimations of the synthesis results come about are subject to the nonzero bits in filter coefficients and estimation of inputs and subsequently we have considered a normal of the synthesis brings about every result of the tables in this paper.

Type	Minimum Period	Maximum Frequency (MHz)	Dynamic Power Dissipation (mw)
CSA row bypassing based	7.792	128.334	23.13
RCA row bypassing based	9.115	109.708	13.98

Table -1 DELAY, SPEED AND THE TOTAL POWER DISSIPATION FOR HILBERT TRANSFORMER

Type	4 input LUTs			Slices			Slice flip-flops		
	utilization	Availability	Usage %	utilization	Availability	Usage %	utilization	Availability	Usage %
CSA row bypassing based	246	20480	1%	144	10240	1%	40	20480	1%
RCA row bypassing based	292	20480	1%	166	10240	1%	39	20480	1%

Table -2. HARDWARE UTILIZATION SUMMARY OF HILBERT TRANSFORMER
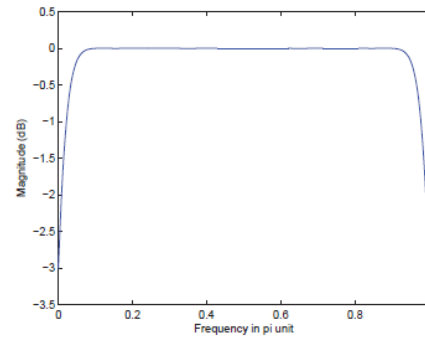
Fig. 5.Pass-band magnitude response of Hilbert Transformer

6. CONCLUSION

The effective usage of low power and a rapid Hilbert transformer is proposed. The essential power decreases are gotten by killing adders when the multiplier operands are zero. Subsequently, CSA and RCA based column bypassing multipliers are utilized to outline a Hilbert transformer. Furthermore, the ripple carries adders are fairly eased back contrasted with carrying save adders because of the more drawn out basic path. Hence, a speed of RCA row bypassing multiplier based transformer is upgraded by a parallel processing of multiplier to shorten defers time. The proposed outlines can be powerfully reconfigured with self-assertive coefficients that are just restricted by their length and word estimate. These transformers are executed and tested on Xilinx Vertex-IV xc4vsx25-10ff668 FPGA gadget family. The execution examination of the two usages is made for speed, territory and power dissemination.

For examination of the speed and region of the RCA and CSA row bypassing based multipliers, numerous irregular input samples are applied utilizing test bench for the filter coefficients given in the illustration. The outcomes show that CSA push bypassing multiplier based Hilbert transformer is better than far as speed and area while RCA row bypassing multiplier based Hilbert transformer is better than far as power dissemination. Among these, the creator can pick the ideal Hilbert transformer structure for a particular application.

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