International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 11 | Nov -2017 www.irjet.net p-ISSN: 2395-0072

Fault Modeling and Parametric Fault Detection in Analog VLSI Circuits using Discretization

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Abstract - *In this paper we proposed a method to detects faults in analog VLSI circuits using discretization. The area of fault modelling in analog VLSI circuit does not achieve the same degree as compare to digital fault model. So there is need of simple analog fault model which works effectively. As we need more application on one chip the circuitry of analog VLSI circuit becomes more complicated so it is very difficult to analyses fault in that circuit. So we give this method to analysis of fault in analog VLSI circuit. The all simulation and algorithm are made with the help of MATLAB/Simulink.*

Key Words: **Parametric faults, analog VLSI circuit, discretization, MATLAB.**

INTRODUCTION

In present scenario analog VLSI circuits are used in wide number of application such as multimedia, cellular communication, digital signal processing and data acquisition. The testing of analog VLSI circuit is a major task before designing and fabrication of any product. The fault detection in analog VLSI circuits is very difficult task due to complexity nature of analog circuits. There is no simple fault model for analog VLSI circuits as present in digital circuits. There are two types of fault model are present in analog circuits. These are catastrophic fault model and parametric fault model. In catastrophic, there is large deviation at output due to large variation in component values (due to short or open circuit). In parametric, the component value will change from nominal value to certain extent. The parametric fault cause due to change in component value due time and environment. The parametric fault sometimes cause the change in output behavior of system sometimes not. But catastrophic fault change the behavior of circuit completely. The testing of analog circuits consume 30% of total manufacturing cost of product [1]. The cost occur in analog circuits testing due to functional testing techniques, these require large number of measurements for test. In this paper we present a analog fault detector using discretization [2][3][4].

Basic Principle

A large number of analog VLSI circuits can be represented by linear state variable equations [5][6][7]. For simplicity here we take single output state variable circuit where the output of every block contain a capacitor (memory element).The state equation for the circuit is given by

$$\dot{X}(t) = A\,X(t) + B\,U(t) \qquad (1)$$

$X(t) = [x_1(t), x_2(t), \dots, x_n(t)]^T$ is state vector containing n variable.

$$\dot{X}(t) = [\dot{x}_1(t) + \dot{x}_2(t), \dots, \dot{x}_n(t)]^T$$

Here $\dot{x}_1(t)$ is derivative with time. The output of the system is given by y (t).

$$y(t) = C\,X(t) + D\,U(t) \qquad (2)$$

By taking Laplace transform we change state variable equation from time domain to frequency s domain that is given by

$$sX(s) = A\,X(s) + BU(s) \qquad (3)$$

From these equation we can derive from signal flow graph [8][9]. Here we taking example of Biquadratic Filter circuit in Fig 1. & Fig 2. Shown the circuit diagram and signal flow graph of biquadratic filter circuit. The biquadratic filter circuit contain three op-amp. First operational amplifier is inverting op-amp, second is integrator and third is lossy integrator.

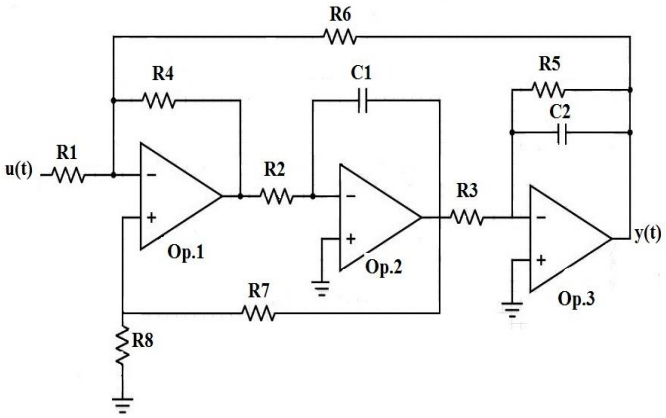

Figure 1: Circuit Diagram of Biquadratic filter

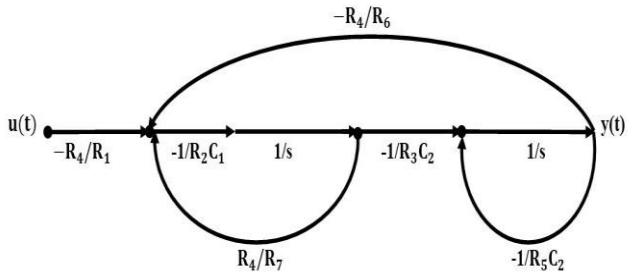

Figure 2: Signal flow graph of Biquadratic filter circuit

By using all the resistor value equal to R and all capacitor value equal to C. then we have $\omega_0 = 1/RC$.From Fig. 2 we can write state equation

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \begin{bmatrix} -\omega_0 & \omega_0 \\ -\omega_0 & -\omega_0 \end{bmatrix} \begin{bmatrix} \frac{x_1(s)}{s} \\ \frac{x_2(s)}{s} \end{bmatrix} \begin{bmatrix} \omega_0 \\ 0 \end{bmatrix} u(s) \quad (4)$$

By applying bilinear transform we get z transform from s domain. In bilinear transform

$$s = \frac{2}{t_s}\frac{z-1}{z+1} \quad (5)$$

Here t_s is sampling time.

By using equation (4) and (5) we get

$$Z_A = (2/t_s\, I - A)^{-1}(2/t_s\, I + A) \quad (6)$$

$$Z_B = (2/t_s\, I - A)^{-1}B \quad (7)$$

So that we can write

$$X(z) = Z_A z^{-1}X(z) + Z_B z^{-1}(u(z) + u(z)) \quad (8)$$

Here z^{-1} is delay. This equation can be write in time domain

$$X(t_k) = Z_A X(t_{k-1}) + Z_B(u(t_{k-1}) + u(t_k)) \quad (9)$$

Here u(t) is input for simulation of biquadratic filter circuit. And sampling rate is $1/t_s$. And sampling frequency is $f(s) = 1/t_s$.

In biquadratic filter circuit by using R=10k and C=0.02μF and by using this we get $\omega_0 = 5000Hz$ and using nyquist criterion t_s=0.0001sec.By using these parameter we find state equation in Z domain.

$$\begin{bmatrix} x_1(z) \\ x_2(z) \end{bmatrix} = \begin{bmatrix} 0.538 & 0.308 \\ -0.308 & -0.538 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.192 \\ -0.038 \end{bmatrix} (u(z) + z^{-1}.u(z)) \quad (10)$$

By applying sinusoidal input u(t)=0.1sin(2π.500t).We simulate biquadratic filter circuit.

Modeling of Faults

For the measurement of different fault occur in circuit one should have complete fault list. There are two types of faults occur in analog VLSI circuits. These are parametric fault and catastrophic fault.

Parametric faults occur in circuit due to some manufacturing defects (change in some parameter like due to doping level and due to oxide thickness). Due to parametric faults in circuit the tolerance of component will vary to certain value. In these types of faults the circuit output may or may not be changed. Because the value of component is increase or decrease to certain value. These type of fault we can remove with the help of knowing the tolerance of component (ie. If there is some change in value then how much output of system is changed).

Catastrophic faults are completely changed the output of the circuit. These cause the short circuit or open circuit. These are also called hard fault. Due to these type of fault the behavior of system changed drastically. These are random faults.

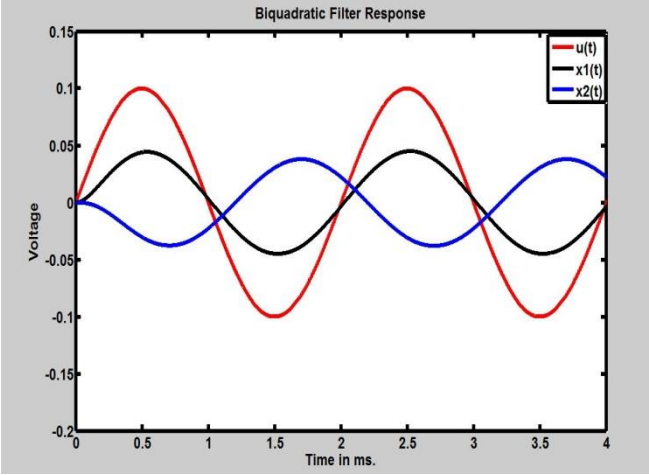

Figure 3: Biquadratic Filter simulation using MATLAB

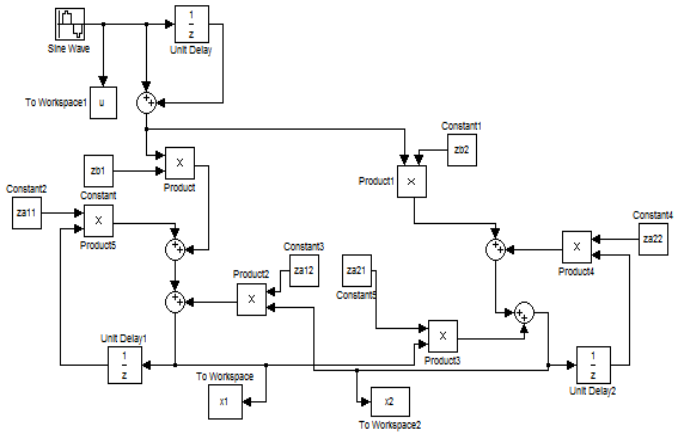

Figure 4: Biquadratic filter in discrete form (using Simulink)

Effects cause by single fault in circuit

When we simulate the circuit with fault the z domain state equation is assumed as discrete network as shown in Fig. 4. Here the coefficient of multiplier are za_{ij} andzb_i. These are the elements from $Z_A$andZ_B.Single fault is appears as with multiple faults in discrete circuit.

For example there is fault inR_5. That is the value of R_5 is changed from its original value. The original value of R_5=10k and due to fault the value is change toR_5=1k. This fault effect the entire matrices of s domain where R_5 is present. Where as it effects both in z domain that is $Z_A$andZ_B. The change in state equation due to fault occur in circuit

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \begin{bmatrix} -5000 & 5000 \\ -5000 & -500 \end{bmatrix} \begin{bmatrix} x_1(s)/s \\ x_2(s)/s \end{bmatrix} + \begin{bmatrix} 5000 \\ 0 \end{bmatrix} u(s)$$

By in z domain it is given as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \end{bmatrix} = \begin{bmatrix} 0.526 & 0.372 \\ -0.372 & -0.860 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.191 \\ -0.047 \end{bmatrix} (u(z) + z^{-1}.u(z))$$

Number of states changed due to single fault in circuit. The major cause of circuit failure is parasitic capacitance. For example here we consider capacitance C_f effect which is at negative terminal of operational amplifier first and output terminal of operational amplifier. Due to this capacitance faulty state is generated which will increase the states. Here we represent it as faulty state (x_f).

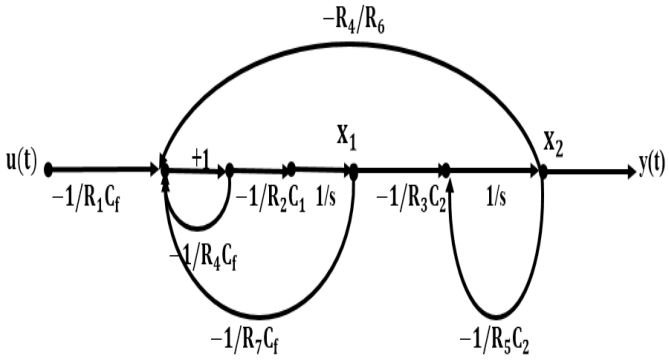

Figure 5: Signal flow graph with increased states

Due to the presence of presence of parasitic capcitance the state equation is also changed and can be written as.

$$\begin{bmatrix} x_1(s) \\ x_2(s) \\ x_3(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -5000 \\ -5000 & -5000 & 0 \\ 5000 & -5000 & -5000 \end{bmatrix} \begin{bmatrix} x_1(s)/s \\ x_2(s)/s \\ x_3(s)/s \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 5000 \end{bmatrix} u(s)$$

And in z domain are given below

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ x_f(z) \end{bmatrix} = \begin{bmatrix} 0.887 & 0.075 & -0.377 \\ -0.377 & -0.585 & 0.075 \\ 0.453 & -0.302 & 0.509 \end{bmatrix} \begin{bmatrix} z^{-1}.x_1(z) \\ z^{-1}.x_2(z) \end{bmatrix} + \begin{bmatrix} 0.047 \\ -0.009 \\ -0.189 \end{bmatrix} (u(z) + z^{-1}.u(z))$$

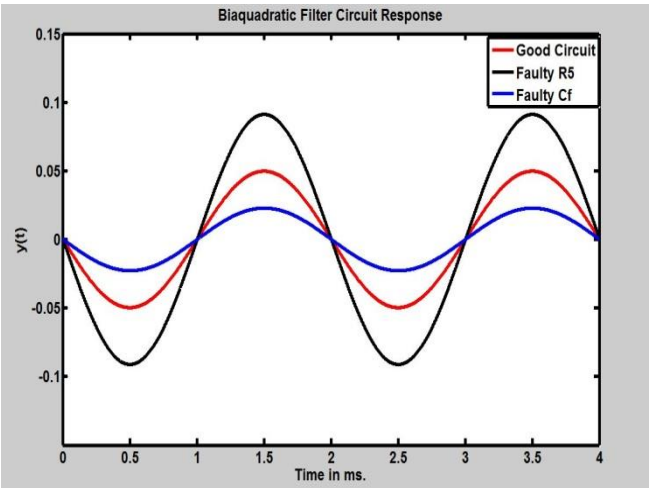

Figure 6: Response of Biquadratic filter at f=500Hz.

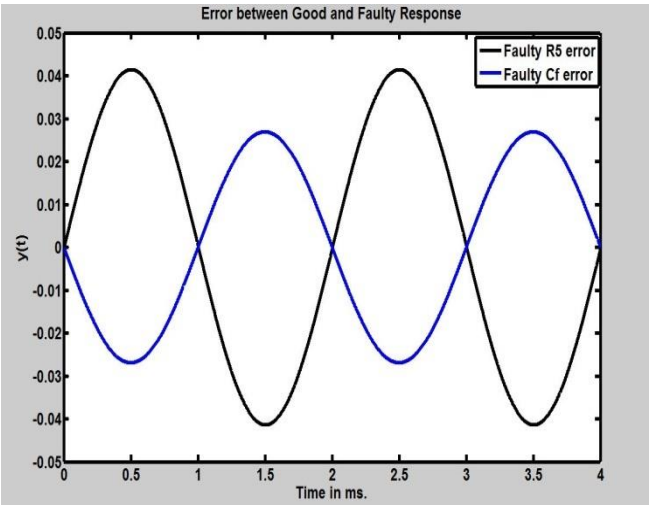

Figure 7: Error between the good and faulty response of Biquadratic filter circuit

Fault Simulation

Our approach work serially for analog VLSI not like parallel approaches. Because is not possible to detected all the faults in the circuit. Here we apply this approach to the parametric fault occur in the analog VLSI circuit that is if the value of the component is changes slightly then the output response of the circuit is changed completely. So it is very necessary to detect these fault. Here in first case we assume fault in R_5 resistor in the biquadratic filter. Then with the help of our approach we detect the response of the good and faulty biquadratic filter circuit. This approach is applicable to all types of circuit which we can convert into the signal flow graph. Our approach is simple and efficient approach as compare to the methods used now a days.

Implementation of Algorithm

The algorithm for fault modelling and detection is constructed with the help of MATLAB and Simulink [10]. The entire algorithm to compute fault in circuits is shown in Fig. 8.With the help of given algorithm we can easily detect the fault in analog VLSI circuit. In this paper we applied our algorithm to two circuit first is Biquadratic filter circuit and second circuit is leap frog filter circuit both circuit are benchmark circuit. Before the implementation of testing method, the method should be applicable to these circuit [11].

Result and Discussion

In this paper fault simulation is done on two benchmark circuit. In first circuit we consider two parametric fault in biquadratic filter circuit where as in second circuit contain only one parametric fault in Leapfrog filter circuit, both the filter are simulate at different frequency that is 500Hz for biquadratic filter and 1kHz for leapfrog filter circuit. Fig. 7 show the response of biquadratic filter circuit that is we use our algorithm to detect the parametric fault occur in circuit[12].

Table: 1 Result for Biquadratic Filter Circuit

Sr. No.	Compo-nent	Original Value	Faulty Value	Freq. (Hz)	Result
1.	R_1	10K	15K	$1.00e^{+02}$	Y
2.	R_1	10K	5K	$1.00e^{+02}$	Y
3.	R_2	10K	15K	$1.00e^{+02}$	N
4.	R_2	10K	5K	$1.00e^{+02}$	N
5.	R_3	10K	15K	$1.00e^{+02}$	Y
6.	R_3	10K	5K	$1.00e^{+02}$	Y
7.	R_4	10K	15K	$1.00e^{+02}$	N
8.	R_4	10K	5K	$1.00e^{+02}$	Y
9.	R_5	10K	15K	$1.00e^{+02}$	Y
10.	R_5	10K	5K	$1.00e^{+02}$	Y
11.	R_6	10K	15K	$1.00e^{+02}$	Y
12.	R_6	10K	5K	$1.00e^{+02}$	Y
13.	C_1	0.01µF	0.02 µF	$1.00e^{+02}$	N
14.	C_1	0.01µF	0.005 µF	$1.00e^{+02}$	N
15	C_2	0.01µF	0.02 µF	$1.00e^{+02}$	N
16.	C_2	0.01µF	0.005 µF	$1.00e^{+02}$	N

Second filter leapfrog filter is simulated with the help of our approach by assuming the fault in R_5 resistor.in this case we also assume the parametric fault in circuit. And by simulation of algorithm at 1 KHz, we detect fault in circuit.

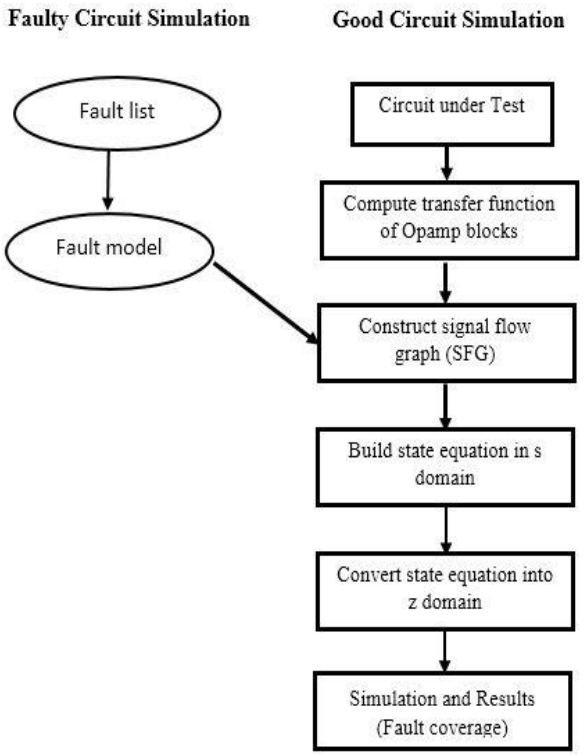

Figure 8: Algorithm used for fault simulation

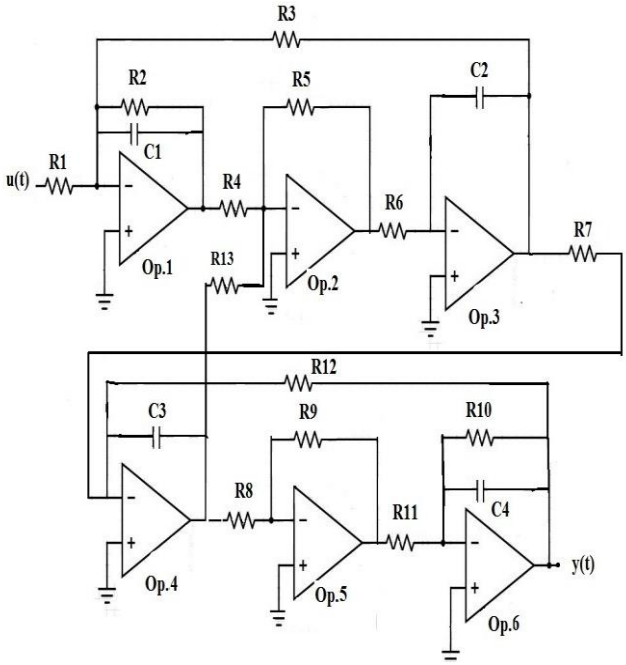

Figure 9: Leapfrog Filter circuit diagram

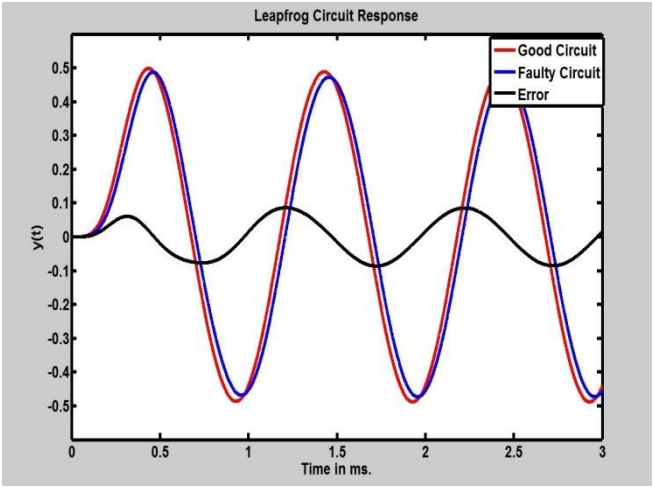

Figure 11: Response of Leapfrog Filter Circuit at f= 1000Hz

Conclusion

We proposed a new approach for fault detection in linear analog VLSI circuit. This approach is done by discretizing the circuit in z domain and sampling frequency is chosen such that we get maximum accuracy. In this paper all the simulation and calculation for transfer function ,state equation in s domain as well as z domain are done with the help of MATLAB and all model for algorithm are construct with the help of SIMULINK. This approach is very effective to linear analog VLSI and our proposed algorithm is applicable to mostly all analog VLSI circuit.

ACKNOWLEDGEMENT

We express our gratitude & appreciation to Dr. Bhopinder Singh, Dr. Subash Dubey, Dr. Sameru Sharma, Dr. M. Tariq Banday, Dr. Sarbjeet Singh, Dr. Simmi Dutta, Er Rouf Ahmed Khan, Er Bharat Mahajan, Er Major Singh, Ms.Sharda Kumari, Er. Mohit Bharti, Mr. Abhiluv Bharti and Ms.Kashish Bharti for their technical and moral support. Last but not least we are thankful to our parents for their encouragement.

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