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Design And Implementation of Different Type Of Adders Using Bit Swapping LFSR As Delay Improvement

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Abstract— Bit swapping technique is applied to conventional LFSR to reduce the number of transitions in generated test vector hence this reduces power consumption during testing. As adders form building blocks of many VLSI circuits different type of adders are considered as a Circuit Under Test and their delay are compared.

Keywords— LFSR,BIST,Ripple Carry Adder,Binary to Excess-3 Converter and Koggestone adder

Introduction

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Built In Self-Test is hardware used for testing where generated test vectors are applied to Circuit Under Test. Test vectors are generated or stored but storing of the test vector consumes memory, so test vectors are generated. LFSR is a one of the Test Pattern Generator (TPG),To have maximum fault coverage the length of test vector should be increased which results in increase of power consumption this increase in power consumption further increases heat dissipation during application of test pattern which will lead to damage of Circuit Under test, On other hand as electronic devices sizes are scaled down and becoming portable ,the reduction of power consumption has become an important issue in VLSI industry There are three types of power dissipation in CMOS Technology a)Static b) Short circuit c) Dynamic

Dynamic power dissipation consist of approximately 90% of overall power consumption it is due to switching activity. Bit swapping LFSR reduces this switching activity by decreasing number of transitions between test factors hence bit swapping LFSR forms effective solution for power consumption in testing. Adders have very important role in digital VLSI circuits. It is used to calculate adders, table indices and other applications. Performance of processor and system, in VLSI can be improved by increasing speed of adders and multipliers that is to reduce delay.

II.BIST

BIST built in self-testing is one of the design for testability methodology that detects fault in integrated circuits and it is also integrated on the same chip .This is helpful in facing testability challenges such as speed, cost and accessibility. It is less expensive as no automatic test equipment required and as it is built on same chip can access to any point on the chip and this also increases speed.

A.Blocks in the BIST:

*Circuit Under Test (CUT): CUT is a system on chip or any block or any part of the circuit that is to be tested
* Test pattern generator (TPG): Generates the text vector which are applied to CUT
* ROM: It stores the response to be compared with CUT output

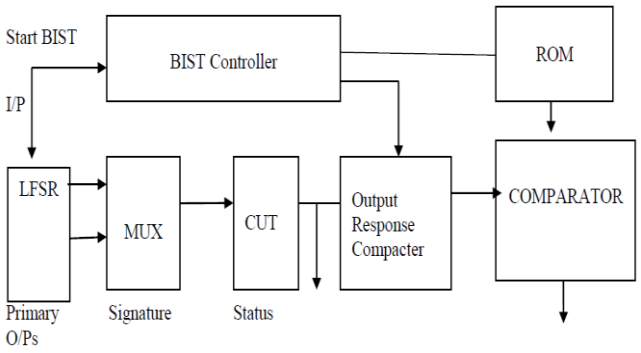

Fig1.1 Blocks in the BIST

B. Bit swapping LFSR:

Conventional LFSR is modified into bit swapping LFSR, which generates pseudo random pattern with less number of transitions between 0 and 1, which occurs in conventional LFSR. As internal switching activity is reduced hence causing less power dissipation in CUT.

Consider n-bit LFSR , the nth bit of LFSR act as selection line that will swap two neighboring bits .If the value of selection line is set 0 for swapping and n is made odd, then bit 1 will be swapped with bit 2,bit n-2 with n-1.If n is made even, then n-3 is swapped with n-2.If n is set to 1 then no swapping .If n is 8 then number of transitions without swapping is 2^8 and number of transitions with swapping is 2^6 number of transitions saved =2^8/2^6, 25% power is saved.

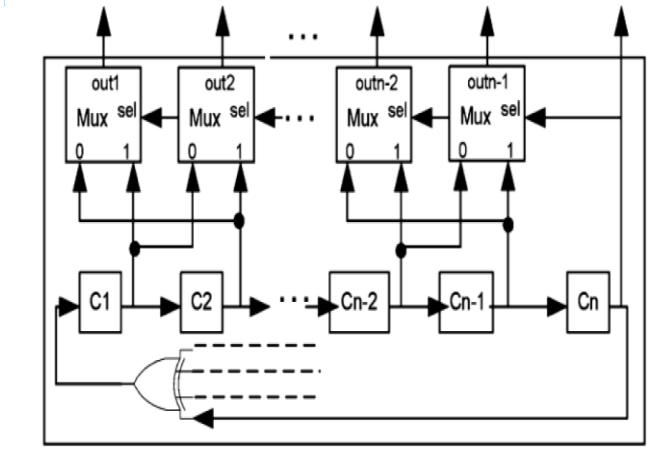

Fig1.2 Bit Swapping LFSR

III.ADDER

A. Ripple Carry Adder (RCA):

Ripple Carr Adder is formed by cascading full adder, carry output of each full adder is feed to next full adder as carry input. To get n-bit Ripple Carry Adder n full adder are cascaded. The gate delay of RCA can be calculated b inspection of full adder circuit. Since full adder should wait for carry bit to be calculated from previous full adder delay is more. As length of bit increases speed of adder decreases.

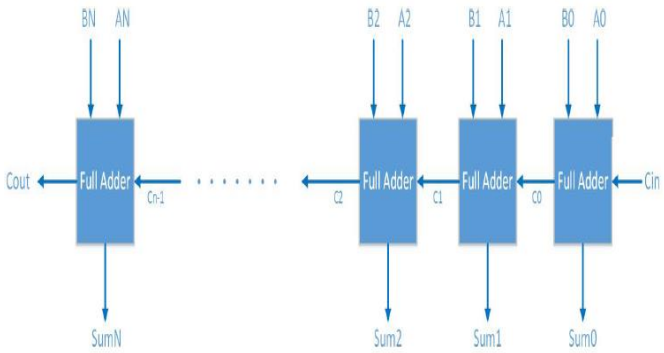

Fig1.3 Ripple Carry Adder

B. Carry Select Adder (CSA):

Carry Select Adder consist of 2 N-bit adders ,time taken to generate and propagate carry is avoided.sum is calculated by both N bit adders for value of carry as 0 and 1.Mux is required to select sum. Carry signal act as select line, depending on the value of carry sum is selected. Fig1.4 represents 8-bit conventional CSA. It consist of three 4-bit ripple carry adder (RCA).

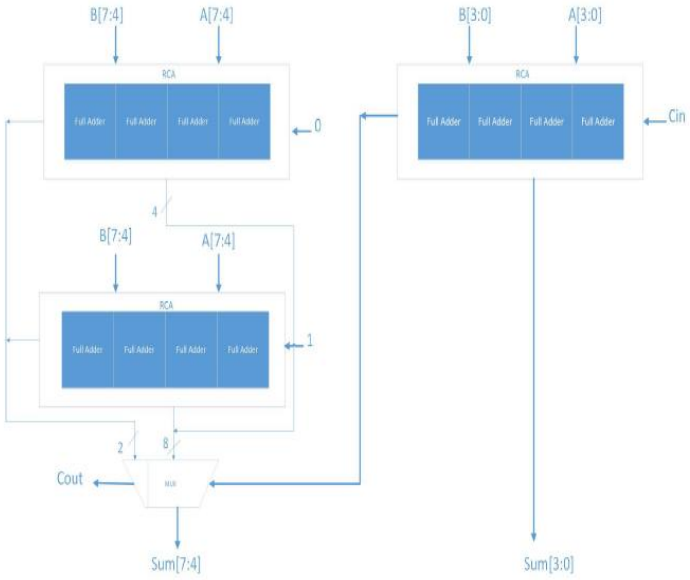

Fig 1.4 CSA with RCA

Fig1.5 represents modified 8-bit CSA. Here instead of RCA 5-bit binary excess converter to 1(BEC) and Two 4-bit Kogge-stone adder are used to calculate the sum instead of Ripple Carry Adder. This reduces delay and increases speed.

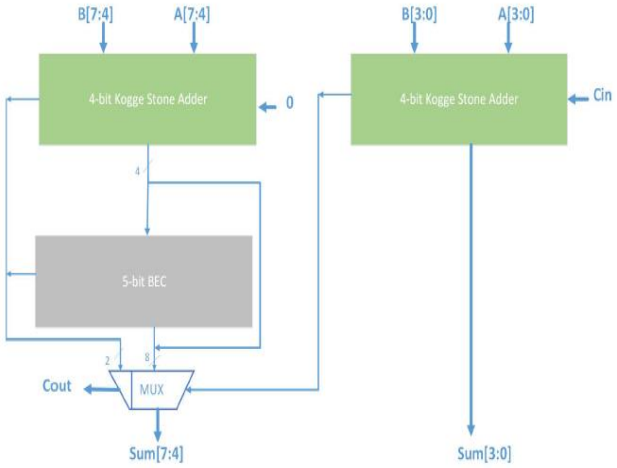

Fig1.5 CSA with Kogge Stone adder with BEC

IV.METHODOLOGY

The block diagram shown below fig 1.6 of our design consists Bit Swapping LFSR to generate 16 bit data using 2:1 multiplexer for the adder which is the Circuit Under Test (CUT).

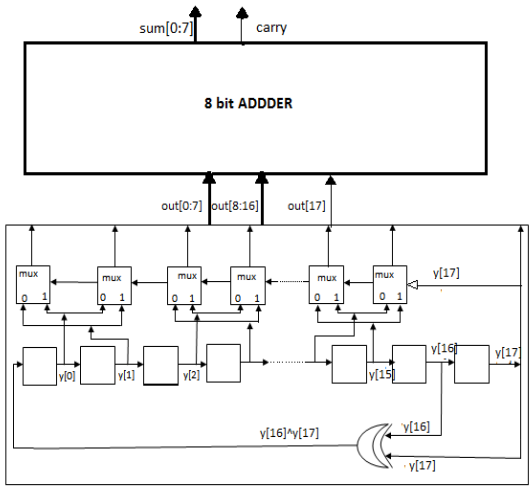

Fig 1.6 Proposed Block Diagram

The designed system presented here involves following blocks

1. Sequence generator
2. Different Adders

V. RESULTS

From table we can say that modified CSA with BEC and kogge stone adder instead of ripple carry adder, both along with Bit swapping LFSR as test pattern generator gives minimum delay. Table 1.1 shows the maximum obtained path delay comparison of different adders. Fig 1.7 represents simulation results out[0:7] , out[8:15] acts as two 8 bit addends and out[16] as carry in.

Table 1.1 Maximum obtained path delay, LUTs and IO Buffers comparison of different adders.

ADDERS	DELAY	LUTs	IO Buffers
Ripple Carry Adder	7.670ns	29	10
Carry Select Adder(Full Adder)	8.478ns	30	10
Carry Select Adder(BEC and Kogge stone adder)	6.795ns	33	10

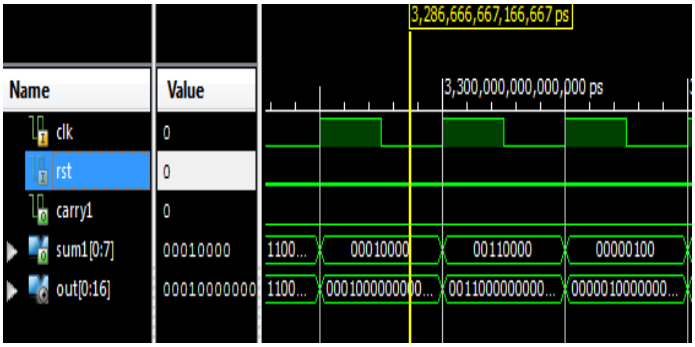

Fig1.7 Simulation Results

VI. CONCLUSION

LFSR is widely used as test pattern generator in BIST one the most efficient testing methodology. Adders are building blocks of digital circuits, speed is important characteristic of adders. In this paper different adder RCA and CSA architecture with Bit Swapping LFSR as test pattern generator which gives low power consumption compared to convention LFSR are designed. From result we can say that modified CSA BEC and kogge stone gives minimum delay.

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