A REVIEW ON WIDE BANDWIDTH LOW NOISE AMPLIFIER FOR MODERN WIRELESS COMMUNICATION

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Abstract - *Recently, the demand of Low Noise Amplifier (LNA) products for the high data rate communication system is rising. LNA transistors are used in applications where a high gain and noise rejection is needed. In the recent era, Low Noise Amplifier (LNA) products have been reported for high gain and good bandwidth for modern applications. In modern communication, Low Noise Amplifier (LNA) products are used in low noise amplifier, distributed amplifier, broadband mixer, power amplifier and active balunes. Today, technology requires high speed transmission efficiency with less power consumption and less circuitry to be used, Low Noise Amplifier (LNA) products satisfy all parameters so that review and future advancement is required to be discussed. In this paper designing, applications, issues and recent trends of Low Noise Amplifier (LNA) products are reviewed for almost all the possible work done in Low Noise Amplifier (LNA) products in past decades.*

***Key Words*: Ultra-wideband (UWB), Hetero junction bipolar transistor (HBT), high electron-mobility transistor (HEMT), MOS Varactor.**

1. INTRODUCTION

Continuous scaling of CMOS technology keeps driving the innovation of RFICs with higher integration level and lower cost. Significant efforts on the study of both devices and circuits also substantiate the wireless communication systems operating toward higher frequencies. Using the K-band (18 – 26.5 GHz) for short-range and high data-rate wireless communication and anti-collision radars is recently of great interest to both industry and academia [1]–[6].

Similar with other portable wireless applications, low-power design is a critical Issue [2]. This paper presents an ultra-low-power 24 GHz low-noise amplifier (LNA) in 0.13 CMOS technology. A peak gain of 9.2 dB and a minimum noise figure of 3.7 dB are achieved with a DC power consumption of 2.78mW only. Design of RF LNAs consists of two major parts, namely selection of transistor geometry and bias point, and also determination of circuit topology including the matching networks. The characteristics of transistors play a critical role, since the core circuit is composed of only a few transistors in most cases. In addition, a simple circuit topology is often preferred to prevent the unpredicted parasitic effects from the complicated layout.

2. REVIEW OF TECHNIQUES

To improve the performance and linearity of low noise amplifier a number of techniques are used since past decades like Wide Range Derivative Superposition Technique, Direct-Coupled Amplifier Topology, Resistive shunt feedback topology and Matching T-network sections, Forward Combining Technique, Gate-Inductive Gain-Peaking Technique, Si-Ge Bi-CMOS technology, switched multi-tap transformer and inductively degenerated. All these techniques are discussed in details in below section.

2.1Wide Range Derivative Superposition Technique

This technique presents an L-band highly linear differential low noise amplifier (LNA) in a standard 90-nm CMOS process. A wide range derivative superposition technique is used to maximize the third-order intercept point (IP3), and at the same time, minimize the third-order inter-modulation distortion (IMD3) over a wide-input power range.

2.2 Direct-Coupled Amplifier Topology

A schematic of the direct-coupled amplifier is shown in Fig. 1. This topology has previously demonstrated sub-2.5 dB noise figure and 3-dB bandwidths up to 6 GHz [l]. The direct-coupled amplifier topology consists of two gain stages. The first stage is a common-emitter amplifier comprised of a HBT transistor, Q1. The second stage is a feedback amplifier comprised of HBT Darlington connected transistors, *Q2* and *Q3,* series feedback resistor R_{ee}, shunt feedback resistor R_{f1}, bias resistor, load resistor R_{load} and output matching resistor R_{out}. Transistors Q1 and *Q3* are nominally biased at a collector current of 4mA while transistor *Q2* is biased at a collector current of 2mA. The first stage acts as a low noise common emitter amplifier stage which determines the noise figure of the overall 2-stage amplifier. The second stage Darlington feedback amplifier provides wideband gain and output drive capability. The bandwidth characteristics of the Darlington feedback stage can therefore be optimized by changing the series and parallel feedback resistors without degrading the noise figure of the overall amplifier. The shunt feedback resistor R_{f1} of the Darlington stage can be adjusted for gain bandwidth performance. R_{f1} also provides a current source for biasing transistor $Q1$ of the first stage. The shunt feedback resistor R_{f2} , connected between the emitter of transistor $Q2$ and the base of transistor $Q1$, can be adjusted to change the effective impedance looking out of the base of transistor $Q1$ toward the source and therefore, optimized for minimum noise match. In addition, R_{f2} provides shunt feedback, which impacts the gain-bandwidth response and determines the input impedance match of the amplifier. Thus, feedback resistor R_{f2}, can be adjusted to obtain optimal noise figure as well as input return-loss performance.

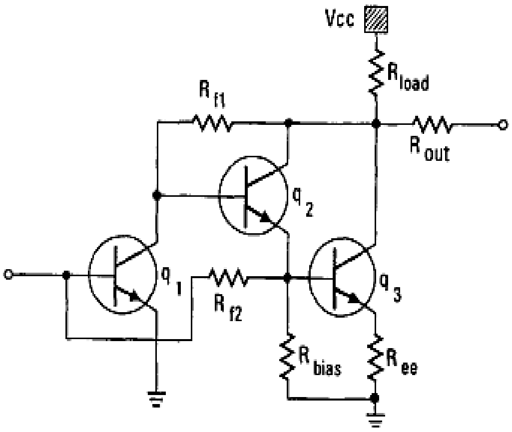

Fig -1: Schematic of the direct-coupled HBT amplifier

2.3 Resistive shunt feedback topology and Matching T-network sections

Broadband systems have traditionally employed distributed amplifier topology. The problem of achieving a broadband match to the transistor input and output impedance is overcome by incorporating the input and output capacitances of a number of transistors into artificial transmission-line structures. But recently, for UWB system, the low power consumption requirement imposes a great challenge on low power distributed amplifier design. And also for distributed amplifier, there is a 50Ω termination resistor in front of the first stage of the amplifier; this will degrade the noise performance of the distributed amplifier substantially. In the proposed solution, shown in Fig.2, the input stage of the LNA is designed by employing a resistive shunt feedback topology together with two T-network sections to match to a 50Ω antenna. At the same time this topology will improve the noise performance compared to the distributed input stage. The second stage is implemented in common source configuration to achieve the higher gain compared to common gate configuration. Current sharing design of the two stages is employed to reduce the power consumption of the proposed LNA under fixed 3-V battery. The output matching is achieved by a single transistor distributed amplifier topology, which means that the inductors absorb the output capacitance of the second pHEMT to form an artificial transmission line terminated by 50Ω to drive an external 50- load.

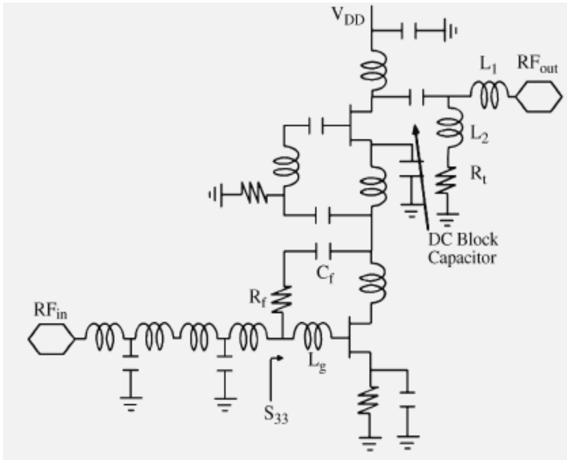

Fig -2: Simplified schematic of the wideband LNA

In order to optimize the power consumption performance and noise performance, the number of the stages of the amplifier and the bias current are determined carefully. To make sure the transistor operates in the linear region, the drain bias voltage of the transistor is at least 1.0 V. Hence with fixed 3 V battery supply, we have three scenarios;

1) one-stage amplifier design with the drain bias at 3.0 V,
2) two-stage amplifier design with current sharing bias topology and drain bias voltage of each transistor at 1.5 V as shown in Fig.2, and
3) a three-stage design, which is similar with Fig. 1 except that we add one more stage into the design and end up with the drain of each transistor biased at 1.0V. Here perfect inter-stage matching between two transistors is assumed.

2.4 Forward Combining Technique

The idea of forward combining technique is illustrated in Fig.3. The RF signals at the drain node and source node of the transistor are in anti-phase because they are derived from common-source and common-drain amplifications respectively. The signal at drain node is shifted to have 90 phase advance and the signal at source node is shifted to have 90 phase lag. These two phase-shifted signals, which are in phase, are combined together before going into the next stage circuit. Since the two signals are in phase, the overall amplifier gain is boosted. The 90 phase shifts can simply be realized by an inductor and a capacitor. The noise figure of the amplifier can also be reduced through the gain enhancement because the noise resistance R_n is inversely proportional to the square of the trans-conductance.

$$R_n = \frac{\gamma g_{d0}}{g_m 2}$$

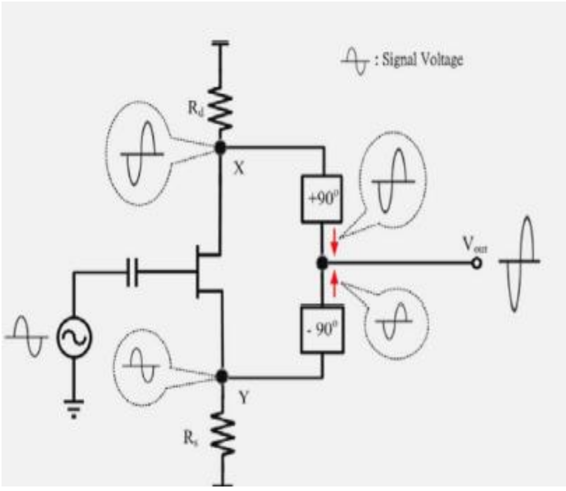

Fig -3: Illustration of forward combining technique

2.5 Gate-Inductive Gain-Peaking Technique

In this technique, only the first and second cascode amplifier stages utilize the gate-inductive gain-peaking scheme for the enhancement of maximum available gain. The last stage is in a conventional cascode structure to maintain a good isolation between the RF input and output ports. Since the gain-peaking inductor degrades the port-to-port isolation, it is worth noting the cascade effect between the first and second cascode amplifier stages. In this work, the gate inductor is tuned after the first stage design.

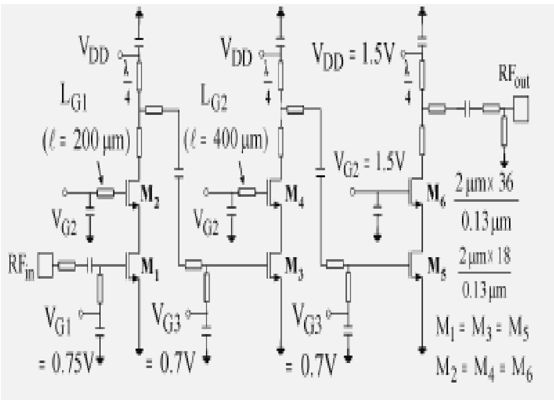

Fig -4: Schematic of the low-power, high-gain V-band LNA

2.6 Switched multi-tap transformer and inductively degenerated

The paper provides a detailed analysis and design strategy for implementing a transformer-based multimode LNA that can be dynamically configured to have a single-band, concurrent dual-band, or wideband frequency response. In the conventional narrowband LNA, shown in Fig.5, a series gate inductor is used for narrowband matching and the input impedance is given as

$$Z_{IN}(\omega) = \frac{g_m L_\theta}{C_{gs}} + j\{\omega L_1 + \omega L_s - \frac{1}{\omega C_{gs}}\}$$

where g_m is the trans-conductance of transistor.

The operating frequency is given as

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_s)C_{gs}}}$$

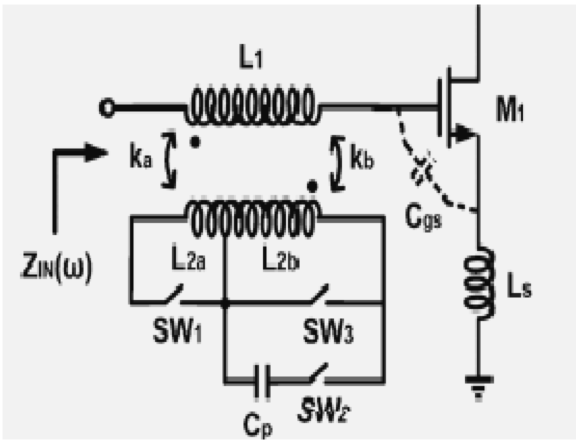

Fig -5: Multimode LNA with a reconfigurable multi-tap transformer as the gate inductor

By controlling the value of capacitance or inductance, the operating frequency of the traditional LNA could be dynamically controlled making it suitable for use in applications for single band, dual band and multiband. Changing capacitance or inductance, however, will also affect the real part of the input impedance, which will have unwanted effects on the input matching and power transfer. Therefore, the only real option for tuning the operating frequency is to control the value.

2.7 SiGe BiCMOS technology

The schematic of the two-stage LNA is shown in Fig.6. The first cascode input stage is chosen for its high power gain, improved input-to-output isolation as well as for improved impedance matching. By using such configuration, the noise performance and maximum power gain at high frequency are improved when compared with the higher single-base device (CBE) and larger parasitic capacitance triple base finger device (CBEBEBC). Simulations have confirmed an improvement in power gain by at least 1.5 dB at 80 GHz when double-base finger devices are used for the LNA design instead of triple-base finger devices. Common emitter (CE) with double-base finger device is used in the second stage for its improved linearity and broader output matching bandwidth.

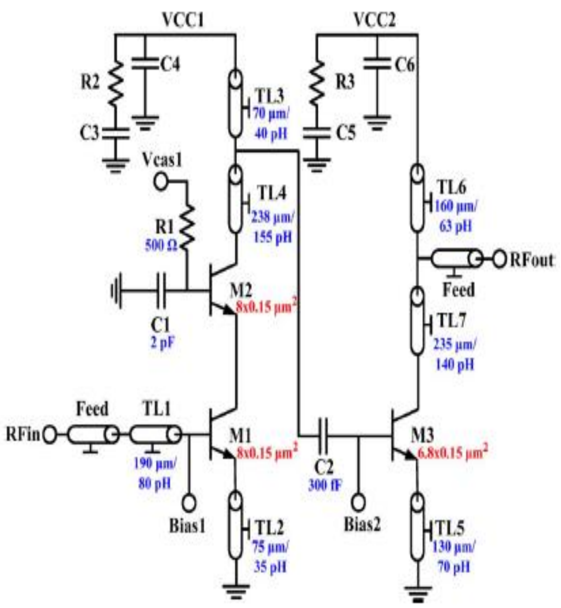

Fig -6: Schematic of the two-stage low-noise amplifier

3. CONCLUSIONS

From the review of Low Noise Amplifier (LNA), it is concluded that product is versatile used in modern applications like Wi-Max, GSM and Satellite Communication etc. Low Noise Amplifier (LNA) provides high current gain and high input impedance in a single package. LNA is used in Darlington products like HEMT, HEBT, Impedance matching network, narrow energy gap transistor used in applications like GaAs, InAs and Gap, post – pre distortion techniques, MOS Varactor technique, multi transformer technique etc, all techniques used to enhance noise rejection capability of LNA , improve gain and bandwidth, but technology requires more Noise Figure, gain, bandwidth with fast transmission of data and hence more discussion and research is demanded for Darlington product. It had reviewed LNA from origin and discusses development and finds different technologies used for implementing different designs in the global foundries.

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