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DESIGN AND VERIFICATION OF PHY INTERFACE FOR PCIe GEN 3.0 AND USB GEN 3.1 USING UVM METHODOLOGY

Richard A Prasad[1], Madhusudan Kulkarni[2]

[1]PG Scholar, Dept. of ECE, CMR Institute of Technology, Karnataka, India
[2]Assistant Professor, Dept. of ECE, CMR Institute of Technology, Karnataka, India

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Abstract - *The peripheral component interconnect bus (PCI) was developed in the early 90's. The standard followed earlier was IBM's advance Technology bus (AT), usually referred as Industry Standard Architecture Bus (ISA), IBM's Microchannel Architecture Bus (MCA), EISA (Extended Industry Standard Architecture) and VESA (Video Electronics Standard Association). Eventually PCI became a standard peripheral bus. After few years, PCI-X (Extended) was developed followed by PCI-X 2.0. The speed ceiling and the high pin count turned the interest from parallel to serial bus model. PCIe (Peripheral Component Interconnect express) is of the third generation and supports servers, systems and mobile devices. PCIe incorporates a layered architecture consisting transaction layer, data link layer and the physical layer. It also owes much to its antecedents, PCI and PCI-X. The PHY (Physical Layer) consists of two sub-blocks logical and electrical which supports duplex communication. Logical sub block has MAC (Media Access Control), PCS (Physical Code Sublayer) and the electrical sub block has PMA (Physical Media Attachment Layer). In this thesis, the work includes, design and verification of several blocks of physical layer for PCI Express and USB. The RTL is modelled in Verilog and the same is verified in UVM (Universal Verification Methodology) environment using Questasim 10.0c from Mentor Graphics.*

Key Words: **PIPE, PCIe, PHY, MAC, PCS, PMA, USB, UVM.**

1. INTRODUCTION

Connecting two or more devices such as CPU, main memory and I/O devices in the system requires buses, these busses usually carry data, address and control signals. The generation of buses is as follows:

The 1st generation buses were like VESA (Video Electronics Standards Association, commonly known as VL Bus), Micro Channel buses and ISA (Industry Standard Architecture).

The 2nd generation of buses are SPI (Serial Parallel Interface), I2C (Inter Coordinated Circuit), AGP (Advanced Graphics Port), USB (Universal Serial Bus), PCI (Peripheral Component Interconnect) and PCI-X (Peripheral Component Interconnect Extended). PCI and PCI-X are also called as Parallel PCI. These 2nd generation buses have high speed, low power consumption and low cost.

The 3rd generation buses include PCIe (Peripheral Component Interconnect Express), SATA (Serial Advance technology Attachment), USB 3.0 and USB 3.1. These 3rd generation buses follow a serial lane based architecture which replaces parallel bus with serial interconnect bus. These 3rd generation I/O buses possess high performance to interconnect peripheral devices and most likely to find home in portable devices, desktop version PC's, servers and workstations in different computing and communications levels.

Traditional PCI (Peripheral Component Interconnect) is a parallel bus specified under the PCI local bus group of standards. It is typically used by the system architects to interconnect peripherals or add optional add-on cards to systems using PCI plug-in cards with PCI slots provided on the motherboard.

PCIe (Peripheral Component Interconnect Express) is an industry standard serial bus protocol that offers high bandwidth communication links from computing, embedded processors to endpoint peripherals like Ethernet, USB, storage and other type peripherals. It offers fewer upgrades to the specifications that went before it like PCI and PCI-X. By moving to a serial interface, fewer pins are required for a PCIe connection than the previously required, PCI and PCI-X.

1.1 Benefits of Serial Bus

Serial format is chosen to minimize the occurrence of timing skew over parallel format. Restriction forced by the speed of an electrical signal is the direct result of timing skew, at finite speed. Various traces in interface possess distinctive length and transmission of parallel signs from source at the same time, reach base during different intervals. Since bits of single bit word arriving is different at destination, parallel recapture of the word becomes difficult. Maximum bandwidth is achieved when the electrical signal speed merges with variance in length between long and short sign of parallel interconnect. Some examples of serial interconnects are SATA, USB, RapidIO and FireWire. Slow devices are allotted with fewer lanes than the fast device as serial multichannel representation to increasing flexibility.

1.2 What is PHY?

PHY (Physical Layer Interface) is an acronym for physical layer of OSI model required to implement physical layer functions. The interface between the link layer, MAC and any physical medium like fiber optics or copper cable is connected through PHY. It distinctively includes Physical Coding Sub layer (PCS) and Physical Medium Attachment layer (PMA).

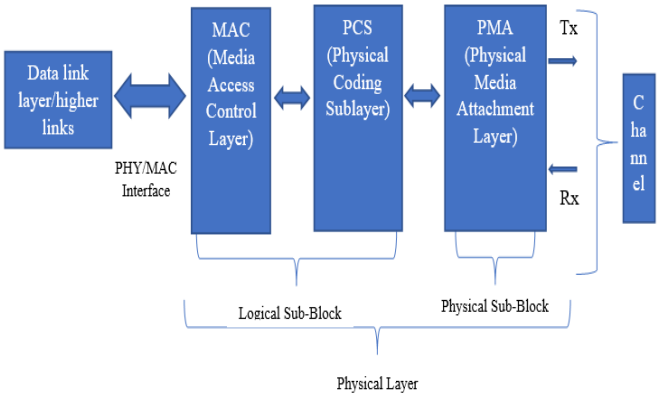

Fig -1: Partitioned physical layer for PCIe

2. PHY LAYER OF PCI EXPRESS

The PHY layer of PCI Express administrates low level PCIe protocol and signaling including features like serialization and deserialization of data, encoding/decoding (128b/130b), 8 GTps, receiver recognition and elastic/analog buffers. The foremost concern of PHY is modifying data clock domain of PCIe rate well matched with general logic of ASIC. The PHY layer has all the necessary circuits for operating the interface, it includes like input buffer, drivers, parallel/ serial to serial/parallel converters, phase lock loops and impedance matching circuits. Through a very specific format data exchange takes place between the physical and data link layer. This layer serializes the received data from data link layer and transmits the same over the PCIe link with compatible width and frequency of device on different side of the link.

3. PROJECT DESIGN AND METHODOLOGY

This thesis mainly involves the designing and verifying/validating of physical layer (PHY) interface for PCIe and USB. The PHY layer we are designing is compatible for PCIe generation 3.0 and USB version 3.1. The document includes the top level of PHY design from verification IP. The diagram below shows the basic architecture block of the design (Physical Layer).

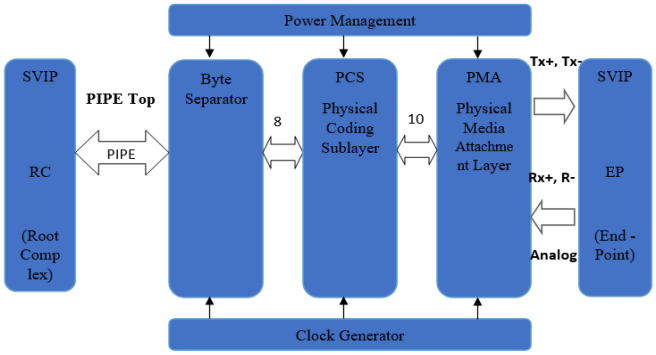

Fig -2: Partitioned physical layer for PCIe

Main modules in the design are SERDES comprising parameterized data (8/16/32) width, clock generation circuitry, encoding/decoding module and byte separator. There's quite a few components or IC's between CPU and PCIe interface collectively referred as root complex (RC). The interface between CPU and PCIe busses may contain several components or chips. Collectively this group is referred to as root complex (RC or root). RC usually inherent at root of the inverted PCIe tree topology. Devices in topology of PCIe that are neither switches nor bridges but perform as initiators and completers of transactions on the respective buses. Endpoints usually inherent at the

3.1 Physical Coding Sublayer

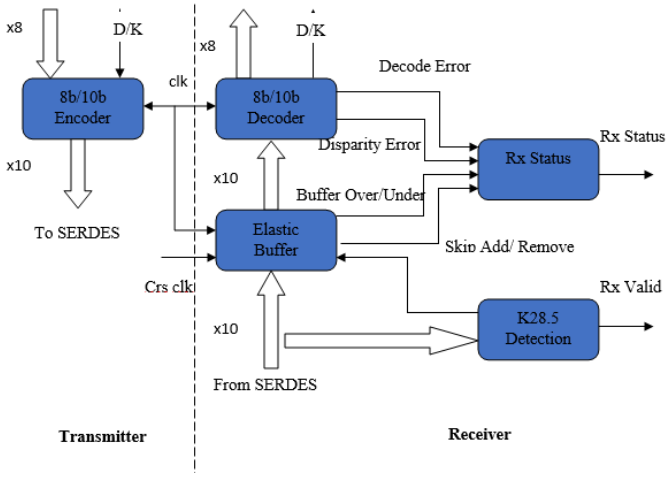

Fig -3: PCS Block Diagram

Lane to lane deskew LTSSM and are the subsections blocks of media access control layer. 8b/10b encoder/decoder, elastic buffer and receiver detection are the subsections blocks of physical coding sublayer. Analog buffers, SEDRES block, 10-bit interface unit are the subsections blocks of physical media attachment layer. The above diagram is subdivided into transmitter and receiver area. Transmitter section includes the 8b/10b encoder. The receiver section involves receiver detection, elastic buffer and 8b/10b

decoder. PCS endorses PHY/MAC Interface as well as interface between PCS and the PMA. Internal bit rate clocks are generated by reference input clock CLK for PCI Express transactions. Data or control character are fed to the 8B/10B encoder, the current RD (running disparity), and the TxDataK signal is needed to encode data character and control character respectively. To process the incoming data the transmitter and the receivers clock frequency should be in synchronization, these shallow variations are indemnified via elastic buffers.

3.2 Physical Media Attachment Layer

The PMA furnishes medium-independent technique for PCS for serialization and deploy physical media. The service interface is responsible for mapping the transmit, receive group between PCS and PMA.

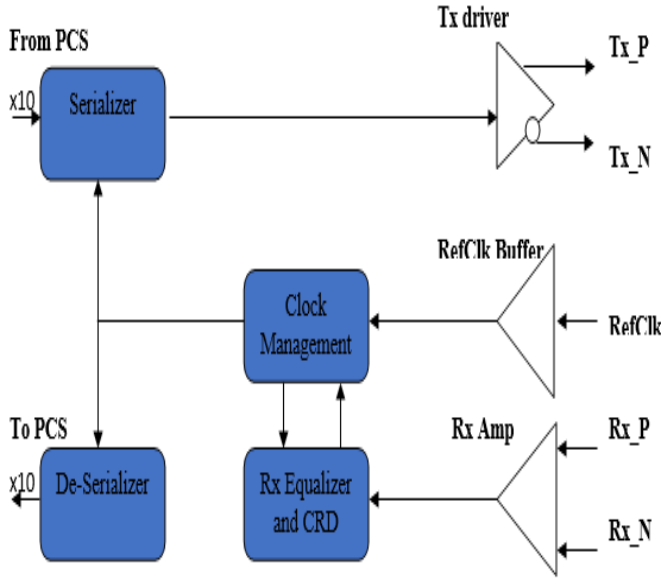

Fig -4: PMA Block Diagram

SERDES functionality and clock recuperation from the code-group provided by the PMD (Physical Media Dependent) layer. The Physical Media Attachment (PMA) Layer includes high-speed analog and digital circuitry for PCI Express signaling, also includes differential drivers and receivers for on lane in a link. Serial transmission takes place over the link and there's a 10-bit parallel implementation-specific interface between PCS and PMA. PMA Consists analog buffers, high speed SERDES (Serialization and De-Serialization) logic creating serial data stream for PCIe, CDR (Clock Data Recovery) wilt PLL and 10-bit interface. Also includes LTSSM (Link Training Static State Machine) required for initializing lanes across links. The above diagram shows the basic PMA block with its internal sub-blocks and architecture.

3.3 PHY Loopback Verification

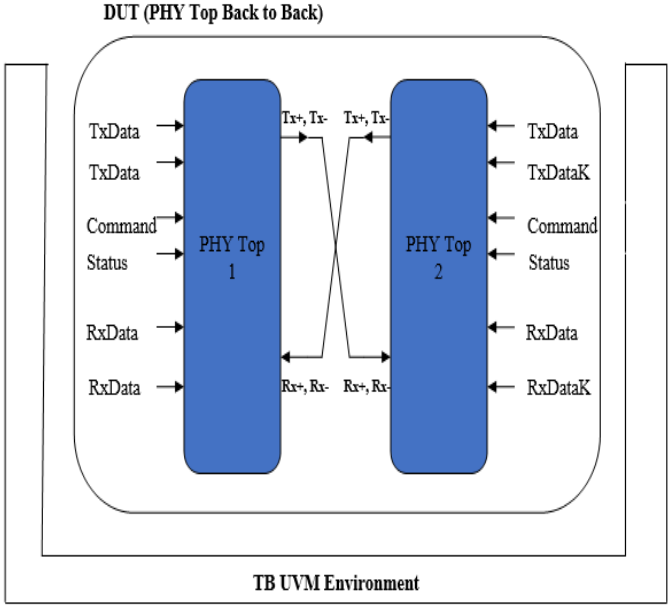

Fig -5: UVM Verification Environment for PHY (Loopback)

For chips to interconnect and communicate with each other many techniques have been established. Some techniques are standardized and some are not. To test, debug, fault isolate and analog or digital validate the loopback (back to back) architecture is used. This loopback is controlled and repeatable at physical layer. loopback is a process where two chips are interconnected and are in a loop and the transmission of signals takes place via in-band interconnects. The input TxData of PHY 1 Top is verified at the output of RxData of PHY 2 Top and the same with TxData of PHY 2 is verified with the RxData of PHY 1. A test bench in UVM environment is built which in turn acts as a MAC (Media Access Control) controlling the PHY (Physical Layer).

3.4 UVM (Universal Verification Methodology)

It is typical derivative of OVM (Open Verification Methodology) and is backward compatible with the OVM. With UVM we can create environments for DUT's in a very systematic manner. Since the methodology is standardized it compiles on all simulators (Questa, IUS and VCS) having system verilog support. This UVM Methodology is an open source, class library and methodology building progressive reusable verification components. The methodology uses language system verilog and enables interoperability and efficiency. Verification environments that are reusable and object oriented can be quickly created using UVM.

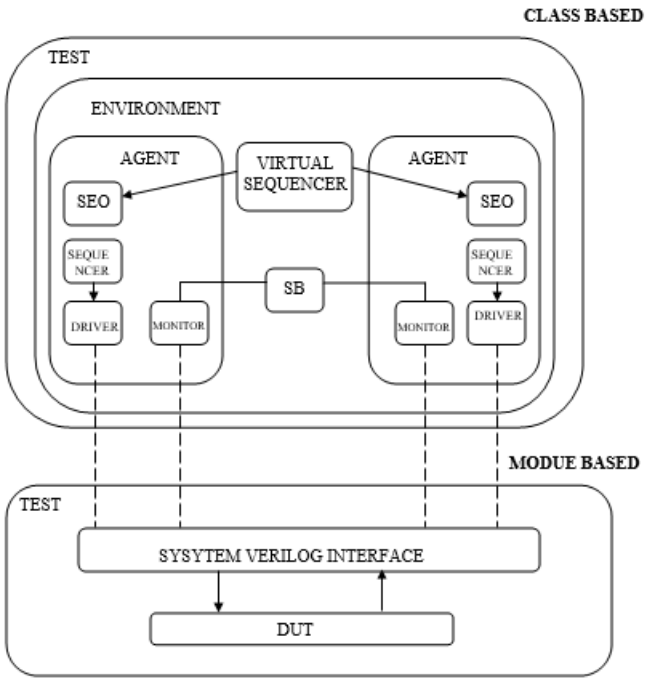

Fig -6: UVM Block Level Architecture and Test-Bench

UVM test-benches are built from classes derived from the UVM component base class. Collection of verification components are reused, when used in the same or different projects they are usually called vertical and horizontal reuse respectively. Frequently reused components are agent and environment.

4. RESULTS

4.1 The 8B/10B Encoder Output

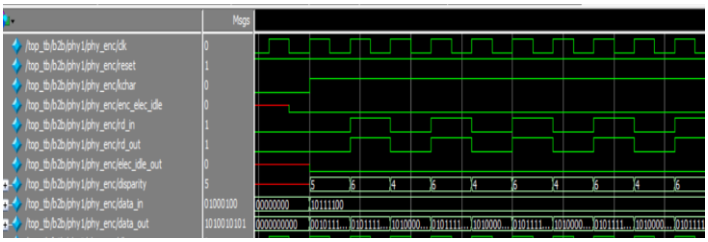

Fig -7: Input/output PHY 1 Encoder

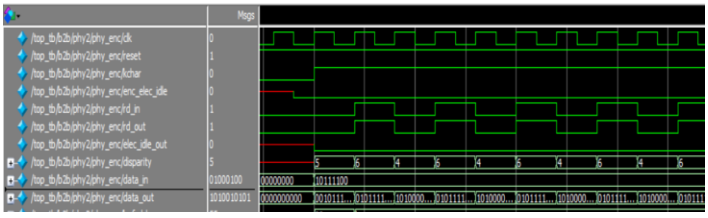

Fig -8: Input/output of PHY 2 Encoder

4.2 The 10B/8B Decoder Output

Fig -9: Input/output of PHY 1 Decoder

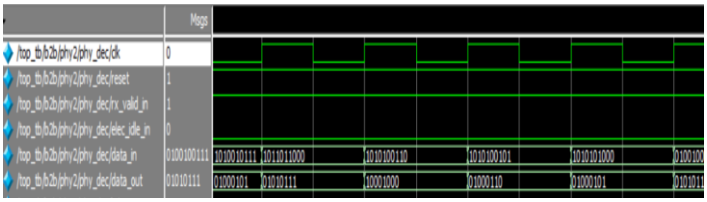

Fig -10: Input/output of PHY 2 Decoder

4.3 SERDES Output

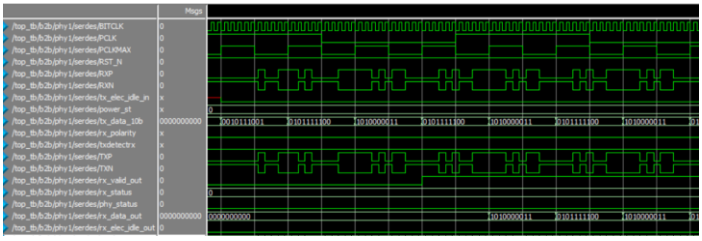

Fig -11: Input/output of PHY 1 SERDES

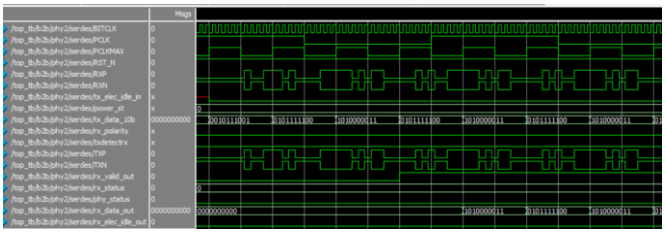

Fig -12: Input/output of PHY 2 SERDES

4.4 PHY Loopback Output

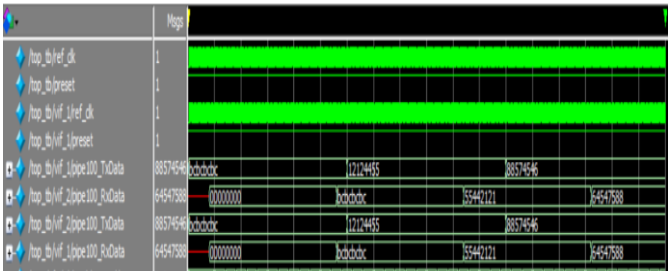

Fig -13: Output of PHY 1 and PHY 2

5. CONCLUSIONS

Designing PCS, PMA and various functional sub-blocks of Physical Layer for PCI Express 3.0 and USB 3.1 has been presented in this paper. The serial data transmission technology makes PCIe further consistent and scalable with very less interference to noise. Improving transfer rate results in improving the overall performance of the system. The 8-bit and data/control character is successfully encoded to 10-bit symbols thru encoder/decoder and inacceptable data is been detected by the encoder.

The underflow and overflow conditions of FIFO are sensed by elastic buffer. SKP symbols are added and removed to the half-filled buffer to maintain the half-filed state. Data loss is evaded by proper synchronization thru Elastic Buffer.

8-bit character, data and control signals are decoded to 10-bit symbols via 8b/10b decoder. Through the received data validity disparity and decoder errors are known. Major future developments are usually carried over in PCS of physical layer. Many such developments were made after the first versions of PCI express. PCIe of 3.0 generation uses 128b/130b instead 8b/10b encoding scheme, practically overcoming maximum overhead in PCI Express 1.0 versions. Point-to-point interconnect has limited electrical load on link permitting frequencies of transmission/reception to scale higher. Systems like “Always-on" are supported by hot Plug/hot Swap.

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BIOGRAPHIES

RICHARD A PRASAD Is pursuing his MTech in VLSI Design and Embedded System in CMR Institute of Technology, Visvesvaraya Technological University, Belgaum. Research interests are Low Power VLSI Design and Physical Design.