International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 01 | Jan -2017 www.irjet.net p-ISSN: 2395-0072

Simulation of H6 full bridge Inverter for grid connected PV system using SPWM technique

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Abstract - *Transformer less inverter is widely used in grid-tied photovoltaic (PV) generation systems, due to the benefits of achieving high efficiency and low cost. Various transformer less inverter topologies have been proposed to meet the safety requirement of reducing leakage currents. In the proposed paper, a family of transformer less H6 inverter topologies with low leakage currents is proposed, and the intrinsic relationship between H5 Inverter topology, highly efficient and reliable inverter concept (HERIC) topology, and the proposed H6 Inverter topology has been discussed well. One of the proposed H6 inverter topologies is taken as an example for detail analysis with operation modes and modulation strategy.*

The proposed H6 Inverter topologies have the following ***advantages*** *and evaluated by simulation results: The conversion efficiency of the novel H6 Inverter topology is better than that of the H5 Inverter topology, and its thermal stress distribution is better than that of the H5 Inverter topology. The leakage current is almost the same as HERIC Inverter topology, and meets the safety standard. The excellent DM performance is achieved like the isolated full-bridge inverter with unipolar SPWM. Therefore, the proposed H6 Inverter topologies are good solutions for the single-phase transformer less PV grid-tied inverters.*

The MATLAB R2010a version is used to simulate the system results and to validate the concept proposed.

1.INTRODUCTION

Technologies available to grid-tie inverters include newer high-frequency transformers, conventional low-frequency transformers, or they may operate without transformers altogether. Instead of converting direct current directly to 120 or 230 volts AC, high-frequency transformers employ a computerized multi-step process that involves converting the power to high-frequency AC and then back to DC and then to the final AC output voltage. Transformerless inverters, lighter and more efficient than their counterparts with transformers, are popular in Europe. However, transformer less inverters have been slow to enter the market over concerns that transformer less electrical systems could feed into the public utility grid without galvanic isolation between the DC and AC circuits that could allow the passage of dangerous DC faults to be transmitted to the AC side. However, since 2005, the NFPA's NEC allows transformer less (or non-galvanically) inverters by removing the requirement that all solar electric systems be negative grounded and specifying new safety requirements. From the safety point of view, most of the PV grid-tied inverters employ line-frequency transformers to provide galvanic isolation in commercial structures in the past. However, line-frequency transformers are large and heavy, making the

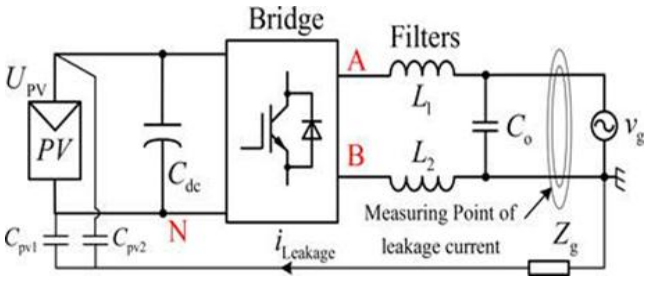

Fig.1.1 Leakage current path for transformerless PV inverters

whole system bulky and hard to install. Compared with line-frequency isolation, inverters with high-frequency isolation transformers have lower cost, smaller size and weight. However, the inverters with high-frequency transformers have several power stages, which increase the system complexity and reduce the system efficiency [3]–[6]. Thus, the transformerless PV grid-tied inverters, as shown in Fig.1.1, are widely installed in the low-power distributed PV generation systems.

Unfortunately, when the transformer is removed, the common-mode (CM) leakage currents ($i_{leakage}$) may appear in the system and flow through the parasitic capacitances between the PV panels and the ground [7], [8]. Moreover, the leakage currents lead to serious safety and radiated interference issues [9]. Therefore, they must be limited within a reasonable range [10]. As shown in Fig.1.1, the leakage current $i_{Leakage}$ is flowing through the loop

consisting of the parasitic capacitances (*C*PV1 and *C*PV2), bridge, filters ($L1$ and $L2$), utility grid, and ground impedance Zg.The leakage current path is equivalent to an LC resonant circuit in series with the CM voltage [11], and the CM voltage V_{CM} is defined as

$$V_{CM} = (V_{AN} + V_{BN})/2 + (V_{AN} - V_{BN}) \frac{L2-L1}{2(L1+L2)} \quad \text{..... Eqn. (1.1)}$$

Where V_{AN} is the voltage difference between points A and N, V_{BN} is the voltage difference between points B and N. $L1$ and $L2$ are the output filter inductors. To eliminate leakage currents, the CM voltage must be kept constant or only varied at low frequency, such as 50 Hz/60 Hz.

In the full-bridge inverters the filter inductors L_1 and L_2 are usually with the same value. Thus, Eqn. (1.1) is simplified as

$$V_{CM} = (V_{AN} + V_{BN})/2 \quad \text{.....Eqn. (1.3)}$$

Many solutions have been proposed to realize CM voltage constant in the full-bridge transformerless inverters A traditional method is to apply the full-bridge inverter with the bipolar sinusoidal pulse width modulation (SPWM). The CM voltage of this inverter is kept constant during all operating modes. Thus, it features excellent leakage currents characteristic. However, the current ripples across the filter inductors and the switching losses are likely to be large.

The full-bridge inverters with unipolar SPWM control are attractive due to the excellent differential-mode (DM) characteristics such as smaller inductor current ripple, and higher conversion efficiency. The CM voltage is kept constant by these full-bridge topologies with unipolar modulation methods. Another solution is to disconnect the dc and ac sides of the full-bridge inverter in the freewheeling modes. Various topologies have been developed and researched based on this method for keeping the CM voltage constant to eliminate leakage currents.

Eliminating the leakage current is one of most important issues for transformer less inverters in grid connected photovoltaic applications. The technical challenge is how to keep the common mode voltage constant to reduce the leakage current. For this purpose, an improved single phase transformer less inverter is proposed. It has two additional switches connected in the dc side. The PWM pulses for those switches are given in such a way that the condition for making the common mode voltage constant is completely met. The common mode voltage can remain a constant during all the modes in the improved inverter. By maintaining common mode voltage as constant in all modes of operation the leakage currents can be effectively reduced.

2.EXISTING INVERTER TOPOLOGIES

H5 and HERIC Inverter topologies are already existing models. H5 Inverter circuit configuration is as shown in fig 2.1. which employs an extra switch on DC side of the Inverter.HERIC Inverter circuit configuration is as shown in fig 2.2. which employs two extra switches at the AC side of the Inverter. Both Inverter topologies have four modes of operation. They are:

1. Active mode in the positive half cycle
2. Freewheeling mode in the positive half cycle
3. Active mode in the negative half cycle
4. Freewheeling mode in the negative half cycle

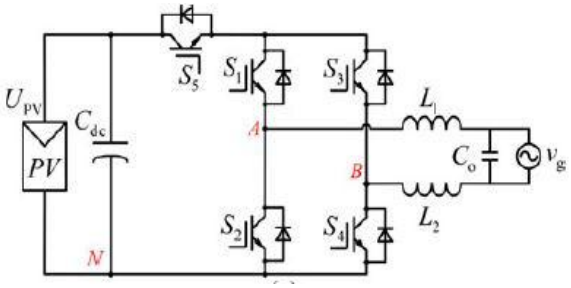

Fig.2.1 Circuit structure of H5 topology

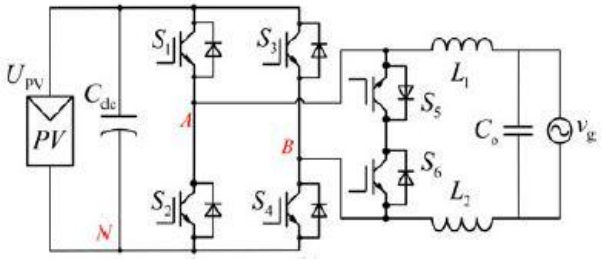

Fig.2.2 Circuit structure of HERIC topology

Each operation mode of operation of the two Inverter topologies has been explained well in reference paper [1]. In this paper a new H6 full bridge Inverter is proposed with unipolar SPWM (sinusoidal pulse width modulation) to reduce common mode leakage current much less compared to H5 and HERIC Inverter topologies.

3.PROPSED H6 INVERTER TOPOLOGY

3.1 Condition of eliminating common mode leakage current

The following assumptions are made for deriving the condition of eliminating the common mode leakage current.

- Filter inductors used L_A and L_B are assumed to be of same value.
- Common mode voltage, μ_{cm} is expressed as
  $\mu_{cm} = (\mu_{AN} + \mu_{BN}) / 2$
- The switches and diodes are ideal and the dead time between the switches are neglected.
- Inductors are ideal without any internal resistance.

3.2. Parasitic capacitance and leakage current

PV panels are manufactured in many layers and the junction of these layers is covered by grounded metallic frame. A parasitic capacitance (stray capacitance) is formed between the earth and the metallic frame. Its value is directly proportional to the surface area of the PV panel. Dangerous leakage currents (common mode currents) can flow through the large stray capacitance between the PV array and the ground if the inverter generates a variable common mode voltage. These leakage currents have to be eliminated or at least limited to a safe value.

3.3 Condition of eliminating the common mode leakage current

The ground leakage current that flows through the parasitic capacitance of the PV array is greatly influence on the common mode voltage generated by a topology. Generally, the utility grid does not influence the common mode behavior of the system. The common-mode voltage can be defined as the average of the sum of voltages between the outputs and the common reference. In this case, the common reference is taken to be the negative terminal of the PV. The differential-mode voltage is defined as the difference between the two voltages.

$$\mu_{cm} = (\mu_{AN} + \mu_{BN}) / 2 \text{...Eqn (3.1)}$$

$$\mu_{dm} = \mu_{AB} = \mu_{AN} - \mu_{BN} \text{.... Eqn (3.2)}$$

From the above two equations

$$\mu_{AN} = \mu_{cm} + \frac{\mu dm}{2} \text{ ....Eqn (3.3)}$$

$$\mu_{BN} = \mu_{cm} - \frac{\mu dm}{2} \text{ ...Eqn (3.4)}$$

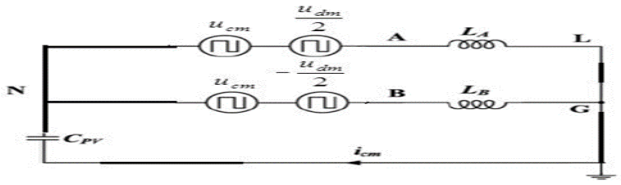

Fig.3.1. Model Showing the Common-Mode and Differential-Mode Voltages

Using Thevenin's theorem in the above circuit the model can be simplified. By applying Kirchhoff's voltage law in the Fig 3.1.

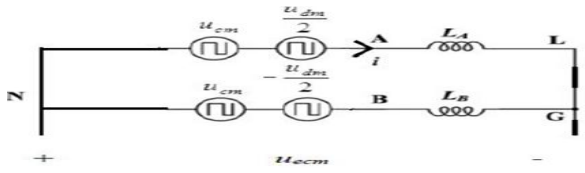

Fig.3.2 Model to find out the Equivalent Common-Mode Voltage

To find out the current,

$$-\mu_{cm} - \frac{\mu dm}{2} - iL_A - iL_B + \mu_{cm} - \frac{\mu dm}{2} = 0 \text{... Eqn (3.5)}$$

$$-\mu_{dm} - iL_A - iL_B = 0 \text{ .....Eqn (3.6)}$$

$$-\mu_{dm} = i (L_A + L_B) \text{ .....Eqn (3.7)}$$

$$i = \frac{-\mu dm}{LA + LB} \text{ .....Eqn (3.8)}$$

To find out the equivalent common mode voltage (μ_{ecm})

$$-\mu_{cm} - \frac{\mu dm}{2} - iL_A + \mu_{ecm} = 0 \text{ .....Eqn (3.9)}$$

$$\mu_{ecm} = \mu_{cm} + \frac{\mu dm}{2} + iL_A \text{ ..... Eqn (3.10)}$$

$$\mu_{ecm} = \mu_{cm} + \frac{\mu dm}{2} + L_A \frac{-\mu dm}{LA + LB} \text{ ...Eqn(3.11)}$$

$$\mu_{ecm} = \mu_{cm} + \frac{\mu dm}{2} \frac{LB - LA}{LA + LB} \text{ .... Eqn (3.12)}$$

The simplified equivalent model of the common-mode resonant circuit has been derived in as shown in Figure 3.3, where *C*PV is the parasitic capacitor, *LA* and *LB* are the filter inductors, *i*cm is the common-mode leakage current. And, an equivalent common-mode voltage μ_{ecm} is defined by,

$$\mu_{ecm} = \mu_{cm} + \frac{\mu dm}{2} \frac{LB - LA}{LA + LB} \text{ .....Eqn (3.13)}$$

3.4 Proposed H6 Inverter circuit topology

From the analysis, an extra switch *S*6 is introduced into the H5 inverter topology between the positive terminal of the PV array and the terminal (B) to form a new current path [1]. Thus, a novel H6 transformer less full-bridge inverter topology is derived, as shown in Fig.3.4. Similarly, the extra switch *S*6 can be introduced into the H5 inverter topology between the positive terminals of the PV array and the terminal (A) to form a new current path as well, as shown in Fig.3.5. Therefore, a new circuit structure of novel H6 inverter is presented. Thus, the conduction loss of the proposed H6 topologies is higher than HERIC topology and less than H5 topology. The two possible configurations of H6 inverter are as shown in figure below.

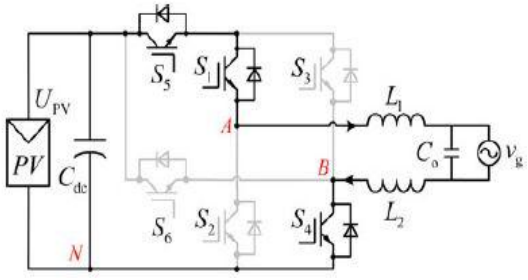

Fig 3.4 Proposed H6-type inverter topology (structure A)

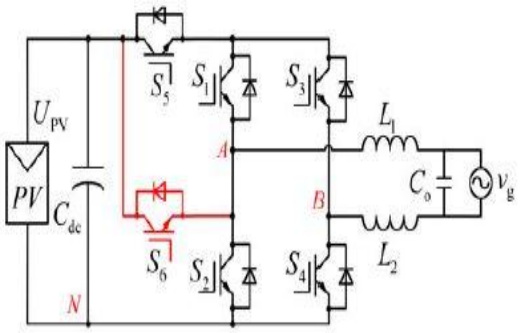

Fig 3.5 Proposed H6-type inverter topology (structure B)

3.5 Operation mode analysis

The circuit structure of proposed novel H6 inverter topologies shown in Fig.3.4 is taken as an example to analysis. PV grid-tied systems usually operate with unity power factor. The waveforms of the gate drive signals for the proposed novel H6 topology are shown in Fig.3.6, where *vg* is the voltage of utility grid. *i*ref is the inductor current reference. *v*gs1 to *v*gs6 represent the gate drive signals of switches *S*1 to *S*6, respectively.

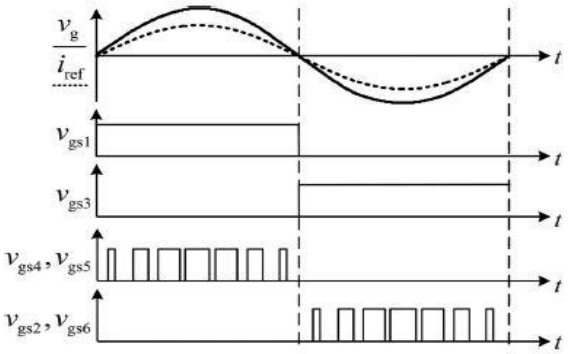

Fig.3.6 Schematic of gate drive signals with unity power factor

There are four operation modes in each period of the utility grid, where V_{AN} represents the voltage between terminal (A) and terminal (N) and V_{BN} represents the voltage between terminal (B) and terminal (N). V_{AB} is the DM voltage of the topology, $V_{AB} = V_{AN} - V_{BN}$. The CM voltage $V_{CM} = 0.5(V_{AN} + V_{BN})$. The four operation modes in each period of utility grid are

1. Active mode in the positive half cycle
2. Freewheeling mode in the positive half cycle
3. Active mode in the negative half cycle
4. Freewheeling mode in the negative half cycle

3.5.1 Active mode in the positive half cycle

Mode I is the active mode in the positive half period of the utility grid voltage, as shown in Fig.3.7. *S*1, *S*4 and *S*5 are turned ON, and the other switches are turned OFF. The inductor current is flowing through *S*1, *S*4 and *S*5.

During this mode of operation

$V_{AN} = U_{PV}$

$V_{BN} = 0$

Thus, $V_{AB} = U_{PV}$

And the CM voltage $V_{CM} = (V_{AN} + V_{AN})/2 = 0.5\ U_{PV}$.

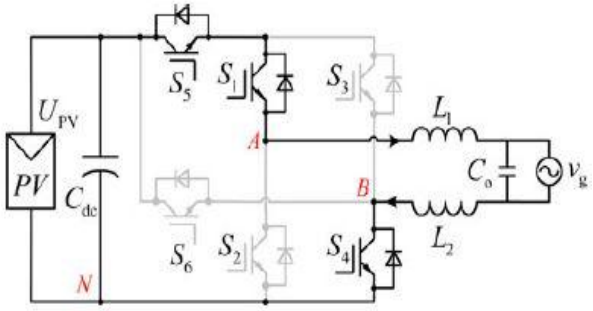

Fig.3.7 Active mode in the positive half cycle

3.5.2 Freewheeling mode in the positive half cycle

Mode II is the freewheeling mode in the positive half period of the utility grid voltage, as shown in Fig.3.8. *S*1 is turned ON; the other switches are turned OFF.As the inductor does not allow sudden changes of current through it so inductor current is freewheeling through *S*1 and the ant paralleled diode of *S*3.

During this mode of operation

$V_{AN} = V_{BN} \approx 0.5\ U_{PV}$

Thus, $V_{AB} = 0$

And the CM voltage $V_{CM} = (V_{AN} + V_{BN})/2 \approx 0.5\ U_{PV}$.

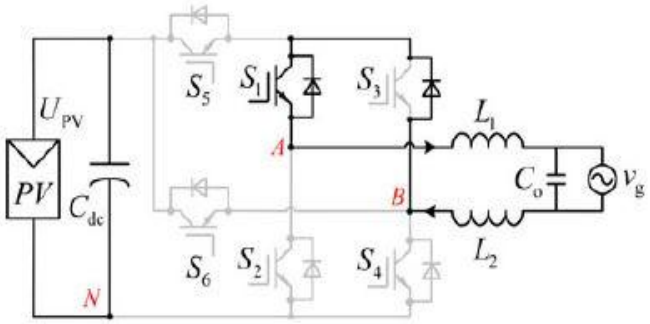

Fig.3.8 Freewheeling mode in the positive half cycle

3.5.3 Active mode in the negative half cycle

Mode III is the active mode in the negative half period of the utility grid voltage, as shown in Fig.3.9. *S*2, *S*3, and *S*6 are turned ON; the other switches are turned OFF.

The inductor current is flowing through *S*2 and *S*6. Although *S*3 is turned ON, there is no current flowing through it, and the switch *S*3 has no conduction loss in this mode. Nevertheless, in the H5 topology, the inductor current flows through *S*2, *S*3, and *S*5. Therefore, the conduction loss of proposed topology is less than that of H5 topology.

During this mode of operation

$V_{AN} = 0$

$V_{BN} = U_{PV}$

Thus, $V_{AB} = -U_{PV}$

And the CM voltage $V_{CM} = (V_{AN} + V_{BN})/2 = 0.5\ U_{PV}$.

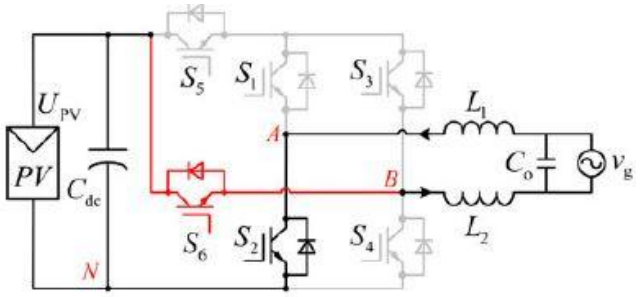

Fig.3.9 Active mode in the negative half cycle

3.5.4 Freewheeling mode in the negative half cycle

Mode IV is the freewheeling mode in the negative half period of the utility grid voltage, as shown in Fig.3.10. *S*3is turned ON, and the other switches are turned OFF.As the inductor does not allow sudden changes of current through it so inductor current is freewheeling through *S*3 and the anti-paralleled diode of *S1*.

During this mode of operation

$V_{AN} = V_{BN} \approx 0.5\ U_{PV}$

Thus, $V_{AB} = 0$

And the CM voltage $V_{CM} = (V_{AN} + V_{BN})/2 \approx 0.5\ U_{PV}$

From all modes of operation, it is concluded that the common mode voltage is constant in each mode of operation. By maintaining so the leakage currents can be reduced. The CM voltage of the proposed topology in each operation mode is equals to 0.5 U_{PV}, and it results in low leakage current characteristic of the proposed H6 topologies.

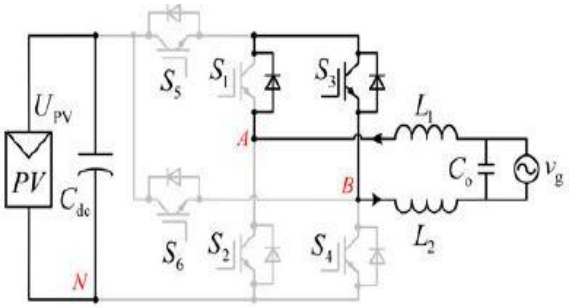

Fig.3.10 Freewheeling mode in the negative half cycle

Based on the fore mentioned analysis, the PV array can be disconnected from the utility grid when the output voltage of the proposed H6 inverter is at zero voltage level and the leakage current path is cut off. The CM voltage of the proposed topology in each operation mode is equals to 0.5 U_{PV}, and it results in low leakage current characteristic of the proposed H6 topologies. The proposed H6 topology with unipolar SPWM method not only can achieve unity power factor, but also can control the phase shifts between voltage and current waveforms. The modulation strategy is shown in Fig.3.11. The drive signal is in phase with the grid-tied current. Therefore, it has the capability of injecting or absorbing reactive power, which meets the demand for VDE-4105 standard.

The schematic of gate drive signals with power factor other than unity are as shown in fig.3.11. From figure, it is observed that the switches S4 & S5 conducts simultaneously while the switches S2 & S6 are in off position and vice versa. The switches S1 & S2 will conduct for more than 50% of the duty cycle.

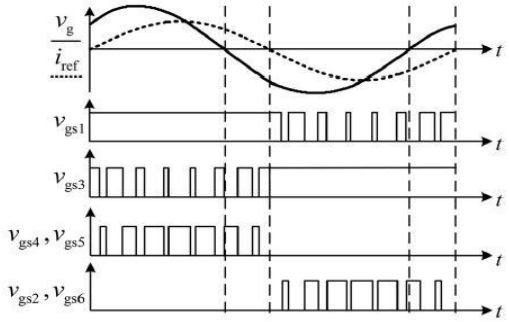

Fig.3.11 Schematic of gate drive signals with power factor other than unity

4. COMPARISON OF THE PROPOSED H6 INVERTER WITH EXISTING TOPOLOGIES

Table 4.1 Comparison of Existing and proposed Inverter topologies

H6 TOPOLOGY	*H5 TOPOLOGY*	*HERIC TOPOLOGY*
Includes two extra switches on the DC side of the Inverter	Includes two extra switches on the DC side of the Inverter	AC side of the Inverter have two extra switches
Total device number is six	Total device number is five	Total device number is six

Device cost is same as that of HERIC	Have lowest device cost	Device cost is same as that of H6
H6 topology has four modes of operation	H5 topology has four modes of operation	HERIC topology has four modes of operation
Conduction losses higher than HERIC	Have highest conduction loss	Conduction loss less than H6
Thermal stress distribution is between H5 and HERIC	Worst thermal stress distribution	Good thermal stress distribution
Leakage current characteristic is like that of HERIC topology	Best leakage current characteristic	Occupies second place in case of leakage current characteristic
Switching losses are same as that of H5 and HERIC	Switching losses are same as that of H6 and HERIC	Switching losses are same as that of H5 and H6
Diode freewheeling loss is same as that of H5 and HERIC	Diode freewheeling loss is same as that of H6 and HERIC	Diode freewheeling loss is same as that of H5 and H6
European efficiency is about 97.09%	European efficiency is about 96.78%	European efficiency is about 97%

5.SIMULATION RESULTS

5.1 simulation model

The simulation model of the H6 full bridge Inverter circuit fed from PV panel feeding the grid through filter inductors is as shown in the figure below. The parasitic capacitances appearing between PV panel and ground are also represented. Unipolar SPWM technique is used as a modulation strategy of switches. By simulating the circuit the common mode voltage is maintained as constant in all modes of operation. And from the results we can prove that H6 full bridge Inverter provides good Differential Mode characteristics with low leakage current characteristic.

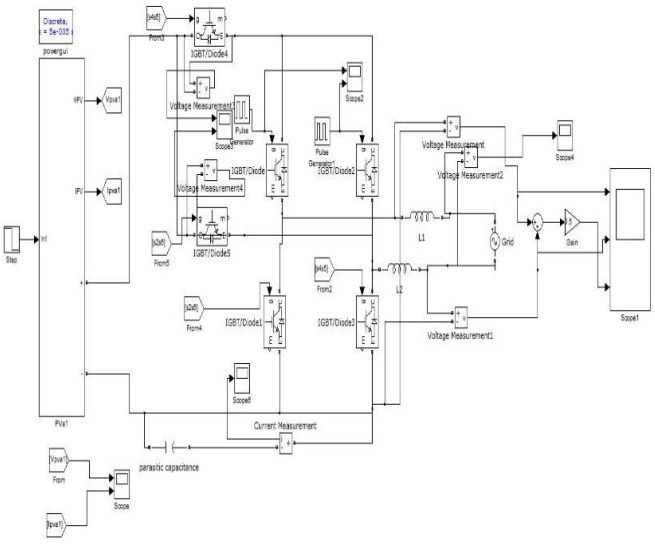

Fig.5.1. Simulation Model of H6 inverter using SPWM technique

5.2 Output Voltage

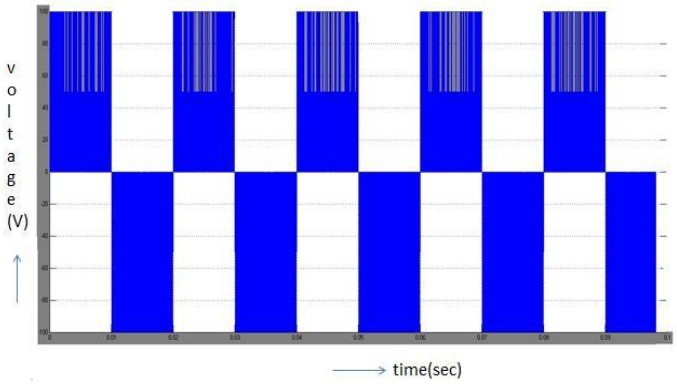

Fig.5.2 Output voltage waveform Differential mode voltage (V_{AB}) = V_{AN}-V_{BN}.

5.3 Common mode voltage

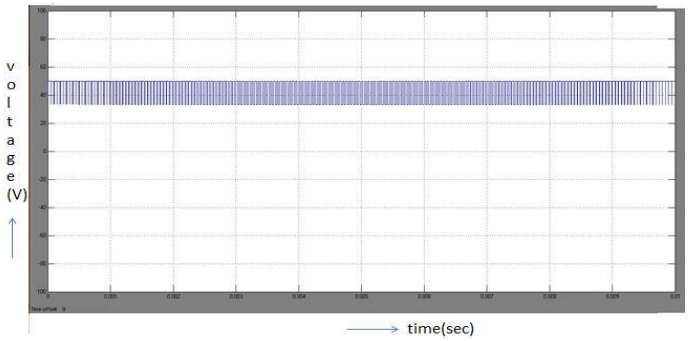

Fig.5.3 common mode voltage waveform

5.4 Leakage current characteristic in H6 topology

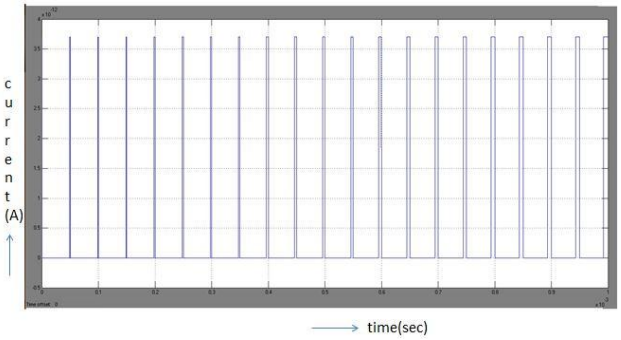

Fig.5.13. Leakage current in H6 topology

6.CONCLUSIONS

Common mode leakage current problem in transformer less inverter is solved using the improved transformer less inverter. The proposed H6 topology is explained in detail with each mode of operation with relevant waveforms showing common mode voltage, output voltage, leakage current, differential mode characteristic and voltage stress across the switches. The improved H6 topology has two additional switches connected in the dc side of the inverter. By employing sinusoidal pulse width modulation technique to the H6 topology the common mode leakage current is kept constant throughout all modes of operation. By maintaining so, the leakage current path is cutoff from the PV panel to the load during freewheeling mode of operation both in positive and negative half cycles. Thereby the common mode leakage current problem in transformer less inverter is solved using the improved transformer less inverter.

ACKNOWLEDGEMENT

I wish to express my gratitude to my beloved guide **Dr. M. VIJAYA KUMAR** M.Tech, Ph.D, Professor, Electrical Engineering Department, J.N.T.U.A. College of Engineering (Autonomous), Anantapur, for his valuable guidance in the successful completion of this dissertation work. I am very much indebted to him for suggesting this topic and helping me at every stage for its successful completion.

I express my profound thanks to **Dr.R. KIRANMAYI** M. Tech, Ph. D, Professor and Head of the Electrical Engineering Department, who has encouraged me to complete the project by providing all necessary facilities to carry out the work in the college.

REFERENCES

[1] Li Zhang, Kai Sun, Yan Xing, Mu Xing "H6 transformerless full bridge PV grid tied Inverters", IEEE Transactions on Power electronics, vol.29, No.3, March 2014.

[2] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2012.

[3] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2012.

[4] B.Yang, W.Li, Y.Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[5] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[6] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[7] W. Cui, B. Yang, Y. Zhao, W. Li, and X. He, "A novel single-phase transformerless grid-connected inverter," in *Proc. IEEE IECON*, 2011, pp.1067–1071.

[8] W. Yu, J. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated ac-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[9] VDE-AR-N 4105: Power Generation Systems Connected to the Low-Voltage Distribution Network—Technical Minimum Requirements For the Connection to and Parallel Operation with Low-Voltage Distribution Networks, DIN_VDE Normo, 2011–08.

[10] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.

[11] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.* vol. 52, no. 4, pp. 902–913, Nov. 2010.

[12] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010

[13] Y. L. Xiong, S. Sun, H. W. Jia, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.

[14] T. Shimizu and S. Iyasu, "A practical iron loss calculation for AC filter inductors used in PWM inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2600–2609, Jul. 2009.

[15] B. Sahan, A. N. Vergara, N. Henze, A. Engler, and P. Zacharias, "A single stage PV module integrated converter based on a low-power current source inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2602–2609, Jul. 2008.

[16] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configuration," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[17] R.Gonzalez, E.Gubia, J.Lopez, and L.Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2694–2702, Jul. 2008.