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Design and Simulation of a 16kb Memory using Memory Banking technique

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Abstract - *Monolithic architecture gives better performance up to in the order of Kb whereas for the bigger memory designs like Mb, the monolithic architecture will not give better performance. As the number of cells increases then the bit line and word line parasitic capacitances increases, hence unwanted delays increases, this in turn reduces the operating frequency. So in the design of bigger memories Memory Banking method is used which gives better performance compared to monolithic architecture.[7] The operating frequency of memory is reduced by a factor two as the number of rows doubles whereas the frequency of operation is reduced by a factor of four as the number of columns doubles. Hence memory banking which is also known as array portioning technique is used in the design of bigger size memories. In industries, the design of bigger memories whose size is around Gb, can be done by using some scripting languages like Perl, SKILL. This paper gives the design of a 16kb memory with the help of memory banking technique.*

***Key Words*: Architecture, capacitances, delays, monolithic, memory banking.**

1.INTRODUCTION

Memory partitioning is the procedure of tiling memory arrays and putting the tiles in memory such that a greatest number of data gets to are fulfilled from local memory. Memory banking is broadly embraced to proficiently increase the memory data transmission by utilizing various memory banks and diminishing data access conflict. Banking distributed arrays to guarantee the locality of reference is broadly perceived as being critical in getting great execution on circulated memory processors. Memory banking has been considered in the distributed registering domain for quite a long time [8, 10, 12], where information components are divided into distinctive processors to diminish communication among the processors. In memory banking method the large array is divided in to number of sub arrays which are identical in size. The sub arrays are commonly referred as macros, which stores the part of the data known as sub word. In order to get complete Word all the sub arrays are accessed simultaneously. To design High performance SRAM the number of macros is limited to around 16 whereas for low power SRAM design the number of macros are limited to only one. [7]

2. DWL TECHNIQUE

In DWL technique the Monolithic array is partitioned into m number of blocks and each block is operated independently hence the word line length is reduced by a factor of m, so the word line RC delay is reduced by a factor of . Hence the frequency of operation is increased by a factor compared to monolithic architecture. The figure 1 shown below depicts the DWL architecture. In that 512 columns are divided into 4 blocks with block size of 128 columns. Now two stages of selection is required to access particular row. First one is a global word line , which is used to select one of the four blocks and second one is local word line which is used to select desired word line. The local word line which are having only 128 columns, hence its RC delay reduces. In spite of the fact that the global word line still is almost the length of the width of the macro it has lower delay compared to full word line because the capacitive load of global word line is smaller. It only consider the input loading of only four global word lines rather than complete loading of 512 cells. And at a time only one block i.e. 128 cells are activated rather than complete memory i.e. 512 cells hence the column current is reduced by a factor of four. The concept of DWL is used recursively in the design of bigger memory leads to hierarchical word line decoding technique.

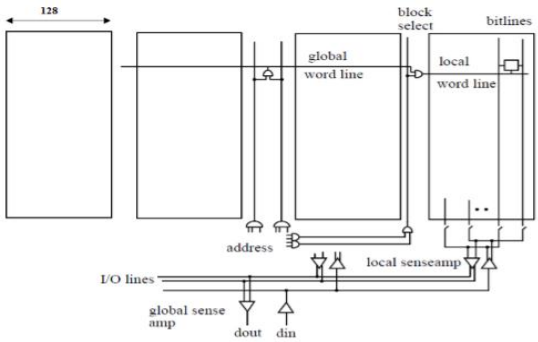

Fig-1 (Divide Word Line architecture)[7]

In this paper 16-Kb SRAM Based memory is designed by using banking method, in which four banks are used with size of each bank is 4Kb. The layout of 16-Kb memory is drawn and post layout simulations also completed for the complete memory. The reason for the Memory Banking architecture presented in this project is to enhance the performance of a system by relegating memory accesses to the disjoint memory banks and giving synchronous clash-free memory accesses. The fig 2 shows the banking

architecture for 16-Kb memory. is selected by using a column 4to1 multiplexer. Hence total eight 4to1 multiplexers are required in the design of 4Kb memory bank.

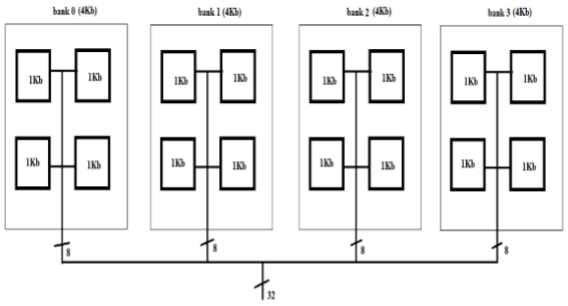

Fig -2: 16Kb memory using banking method

3. DESIGN OF 4KB MEMORY BANK

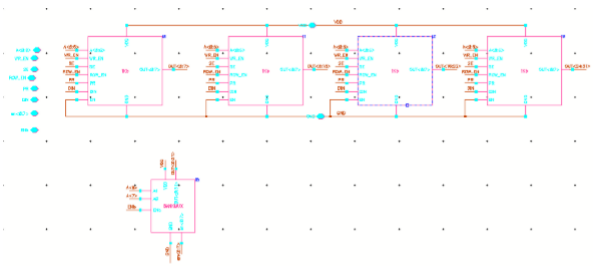

Fig – 3 Schematic of 4Kb Memory Bank

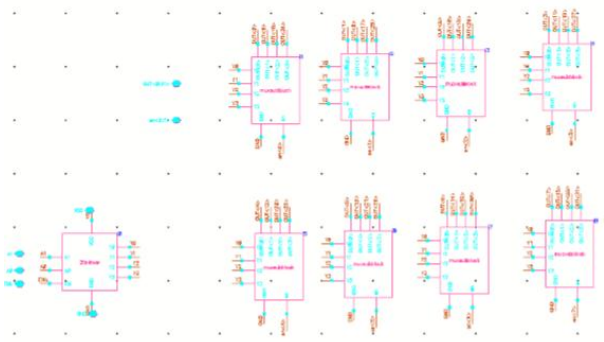

Fig 4 - Schematic of Bank Multiplexer of 4-Kb Memory

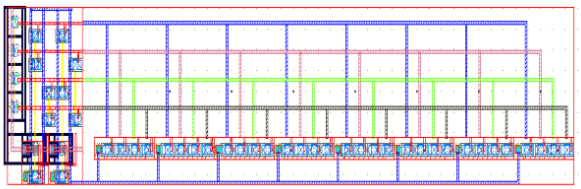

Fig 5: Layout of Bank Multiplexer of 4Kb Memory Bank

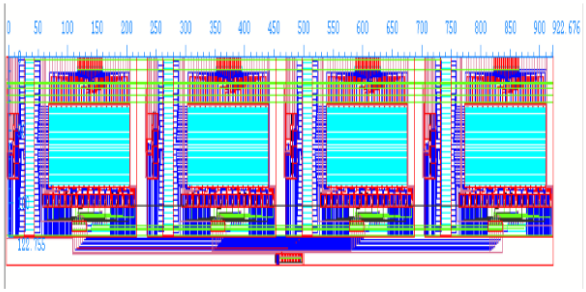

Fig 6: Layout of 4Kb Memory Bank

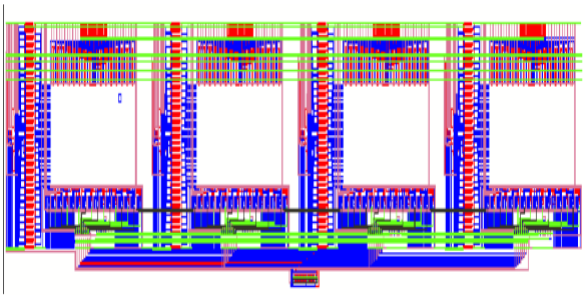

Fig 7: Av-Extracted View of 4Kb Memory Bank

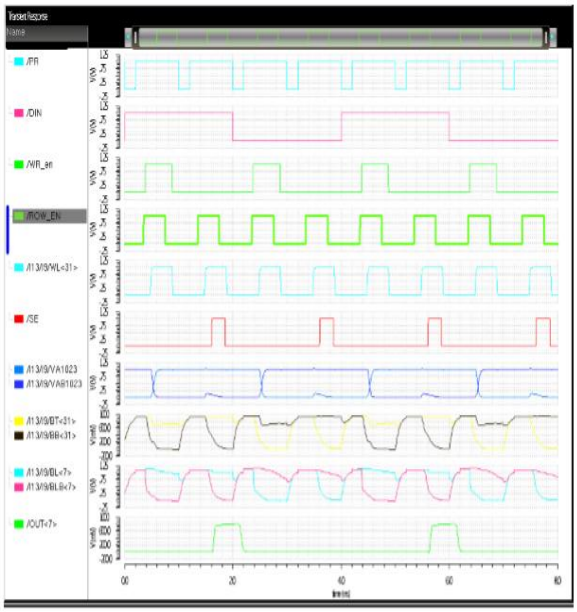

Fig 8: Simulation Results of 4Kb Memory Bank

Table 1: Power Analysis of 4Kb Memory Bank

S.No	Description	Pre-Layout Simulations	Post-Layout Simulations
1	Write 1 power	14.19 p Watt	16.11 p Watt
2	Read 1 power	14.07 p Watt	15.37 p Watt
3	Write 0 power	14.36 p Watt	16.63 p Watt
4	read 0 power	14.33 p Watt	15.67 p Watt
5	Total transient power	57.01 p Watt	80.10 p Watt
6	frequency	1.25 Ghz	1Ghz

4. DESIGN OF 16kb MEMORY BANK

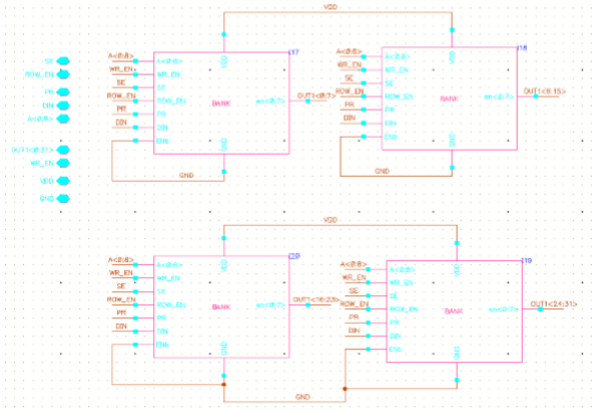

Fig 9: Schematic of 16-Kb Memory

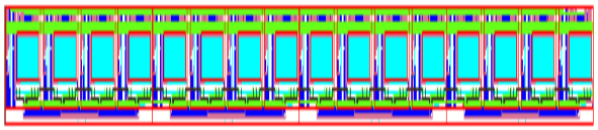

Fig 10: Layout of 16Kb Memory

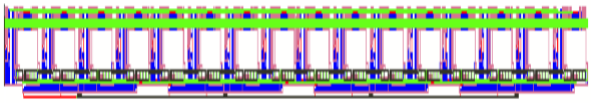

Fig 11: Av-Extracted View of 16-Kb Memory

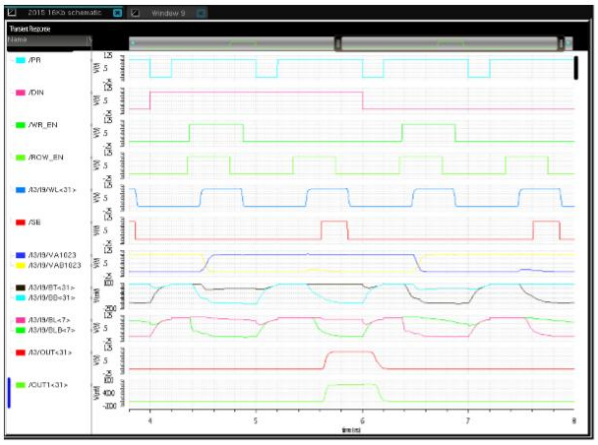

Fig 12: Simulation results of 16kb SRAM Memory

5. CONCLUSIONS

In this paper design and simulation of 4kb Memory and 16 Kb memory has been studied. 16-Kb Memory is designed using banking method with data width of 32 bits and it takes 1ns for one complete operation hence frequency of operation is calculated as 1 GHz.

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