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Design of Parallel Self-Timed Adder

P.S.PAWAR[1], K.N.KASAT[2]

[1]PG, Dept of EEE, PRMCEAM, Badnera, Amravati, MS, India.
[2]Assistant Professor, Dept of EXTC, PRMCEAM, Badnera, Amravati, MS, India.

Abstract - *Adders being core building blocks in different VLSI circuits like microprocessors, ALU's etc. performance of adder circuit highly affects the overall capability of the system. In this paper we present the design and performance of Parallel Self-Timed Adder. It is based on a recursive formulation for performing multibit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fanouts. The proposed work mainly aimed at minimizing the number of transistors and estimation of various parameters viz., area, power, delay for PASTA. We have also designed 4 bit PASTA as an example of proposed approach. Simulations have been performed using MICROWIND 3.1software and DSCH tool in 45nm CMOS technology that verify the practicality and superiority of the proposed approach over existing asynchronous adders.*

***Key Words*: Binary adders,Parallel, Adders, Asynchronous circuits, CMOS design.**

1.INTRODUCTION

Addition is the most common and often used arithmetic operation in microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Thus performance of any circuit is mainly determined by speed of adder circuit. Circuits may be classified as synchronous or asynchronous. Synchronous circuits are based on clock pulse whereas an asynchronous circuit, or self-timed circuit, is not governed by a clock circuit or global clock instead, they often use signals that indicate completion of operations [1] [6]. Such a system tends to have better noise and electromagnetic compatibility properties than synchronous systems due to the absence of a global clock reference [4]. Asynchronous operation by itself does not imply low power, but often suggests low power opportunities based on the observation that asynchronous circuits consume power only when it is active. The synchronous adders perform slowly due to its incremental nature of operation and therefore it is not recommended for fast and parallel adders. The basic building block of combinational digital adders is a single bit adder. The simplest single bit adder is a half adder (HA). The full adders (FA) are single bit adders with the carry input and output. The full adders are basically made of two half adders in terms of area, interconnection and time complexity. This paper proposes the design of parallel self timed adder (PASTA). The design of PASTA is regular and uses half adders along with multiplexers with minimum interconnection requirement. The interconnection and area requirement is linear which makes it feasible to fabricate in a VLSI chip. The design operates in a parallel manner for those bits that do not require any carry propagation. It is self timed, which means that as soon as the addition is done, it will signal the completion of addition thereby overcoming the clocking limitations.

2. RELATED WORK

1] Jens Sparso and S. Furber, 2001 [1] introduced us from background in synchronous digital circuit design to the fundamentals of asynchronous circuit design. Also their work provide the basis to clear need for asynchronous circuits and its performance parameters and their implementation.

2] Ashivani Dubey and Jagdish Nagar, 2013 [2] the comparison between serial adder and parallel adder is proposed in this paper. The author compared the serial adder and parallel adder for speed of operation and power consumption parameters. Serial adder consumes low power but are slow as compare to parallel adder. Whereas parallel adder consume more power as compared to serial adder but as parallel adder add all bit simultaneously they give fast response.

3] N. Weste and D. Harris, 2005 [3] the fundamental theory behind CMOS VLSI Designs is discussed in this book. This include brief description of CMOS logic, CMOS Processing Technology, Circuit Characterization and Performance Estimation , Combinational & Sequential Circuit desig,Circuit Simulation and various tools for testing and verification.

4]David Geer, 2005 [4] presented that Clockless/asynchronous chips offer an advantage over the synchronous counterparts because asynchronous chips have no clock and each circuit powers up only when used, asynchronous processors use less energy than synchronous chips by providing only the voltage necessary for a particular operation. Clockless chips offer power efficiency, robustness, and reliability.

5] Masashi Imai Takashi Nanya, 2008 [5] presented a performance comparison of a self-timed asynchronous circuits with synchronous circuits based on the Technology

Roadmap of Semiconductors. In this paper the author shown that the cycle-time of synchronous circuits becomes large as the process feature size decreases since the maximum delay becomes large due to large variations while the cycle-time of self-timed circuits does not become so large since it depends on the average delay. The self timed asynchronous circuits are effective in the view point of both speed performance and energy dissipation in the future technologies.

6] N. R. Poole, **1994** [6] in this work presented some of the key principles behind self-timed operation. Two main architectural styles have been adopted for the design of self-timed processors: time-stationary and data stationary. Both rely on a pipelined approach. The associated technology has the potential to solve a number of problems which are on the horizon, if not yet critical, for large-scale digital systems.

7] Mark A. Franklin and Tienyo Pan, **1994** [7] presented a performance comparison of asynchronous adders where six adder designs are studied, and their influence on asynchronous system performance are compared in this paper. In asynchronous systems, average function delays principally govern overall throughput.

8] Manisha and Archana, **2014** [8] presented a comparative study of 1-bit CMOS full adder cells using standard static CMOS logic style. The comparison is carried out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP). Different full adders are studied in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor logic (CPL), Double pass transistor logic (DPL), Transmission gate (TGA), Transmission function (TFA), New 14T, Hybrid CMOS, HPSC, Pseudo nMOS, GDI full adders.

9] Akansha Maheshwari and Surbhit Luthra, **2015** [9]proposed a low power full adder circuit implementation using transmission gate. In this paper, the power consumption of a conventional full adder circuit is reduced by using transmission gate at the place of pass transistor logic (NMOS or PMOS). This circuit is designed using 100nm technology parameters.

10] Swaranjeet Singh, **2013** [10] presented a comparative analysis of CMOS transmission gate based adders. Three different types of 4-bit transmission gate based adders namely Ripple Carry Adder, Carry Select Adder and Carry Lookahead Adder are designed in this paper. The different adders are compared on basis of number of transistors, the average power consumption and delay. The simulation results are taken for 180nm technology with the help of Tanner (T-spice) simulation tool.

11] M. Z Rahman, L.Kleeman, and M A.Habib, **2014** [11] proposed a parallel single-rail self-timed adder. It is based on a recursive formulation for performing multibit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. A practical implementation is provided along with a completion detection unit. The author present simulation results using Mentor Graphics Eldo SPICE version 7.4_1.1, running on 64-bit Linux platform.

12] P. Balasubramanian and D.A. Edwards, **2008** [12] presented a new gate level ST full adder, based on synchronous standard cells. Muller C-elements (especially 3 and 4-input elements), which form the backbone of robust self-timed architectures, have also been realized using suitable standard cells of the library.

3. PROPOSED WORK

3.1 DESIGN OF PASTA

The architecture and theory behind PASTA is presented in this section.

A] Architecture of PASTA

The general block diagram of the PArallel Self-Timed Adder (PASTA) is presented in Fig.1. Multi bit adders are often constructed from single bit adders using combinational and sequential circuits for asynchronous or synchronous design.

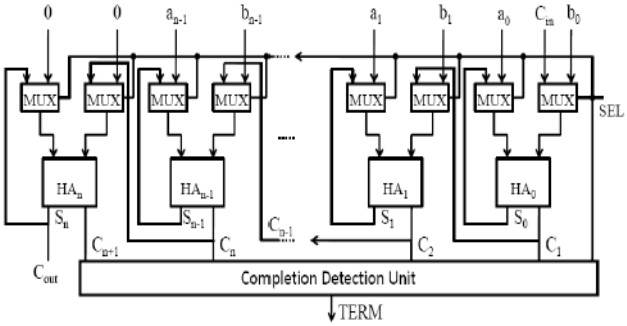

Fig-1: General block diagram of Parallel Self-Timed Adder

The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The adder first accepts two operands to perform half-additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

B] State Diagrams

In Fig.2, two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (*Ci*+1 *Si*) pair where *Ci*+1, *Si* represent carry out and sum values, respectively, from the

*i*th bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state *(11)* cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion.

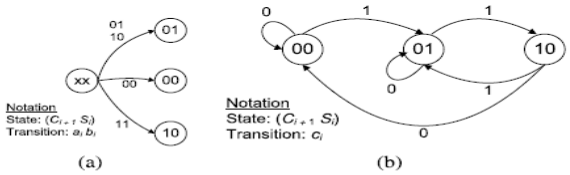

Fig-2: State diagrams for PASTA. (a) Initial phase. (b) Iterative phase.

3.2 IMPLEMENTATION OF PASTA

In this section PASTA is implemented using CMOS technology. The general block diagram of Parallel Self-timed Adder includes following circuits modules:-

- Half-Adder
- Multiplexer
- Completion detection circuit.

The conventional circuit and the proposed circuit for each of the blocks of Parallel Self-timed Adder are as describe and implemented in detail:-

3.2.1 Half Adder

Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit and a carry bit as the output as shown in Fig.2.

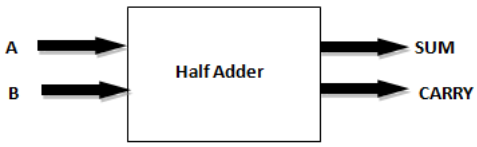

Fig-2:- Block diagram of Half Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table-1:- Truth Table of Half Adder

The operation of half adder is based on the truth table shown above. The different Half Adder circuit are designed as shown below:

A)Half Adder using Logic Gates

For sum side, EX-OR gate using NOT, AND and OR gate requires 22 transistors. For carry side, the carry output is obtained by ANDing the two inputs A and B. This means we require 6T i.e in total we require 28T for implementing half adder using CMOS transistors.

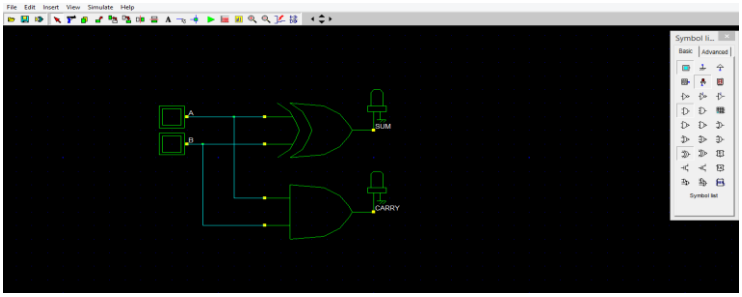

Fig-3 :- Basic Logic diagram of Half Adder

B) Half Adder using NAND Gates

The basic NAND gate requires 4T for its implementation using MOS transistor. i.e., two pMOS transistor in pull-up network and two nMOS transistor in pull-down network. Thus when implementing half adder using NAND gates only, we require 20 T for following circuit.

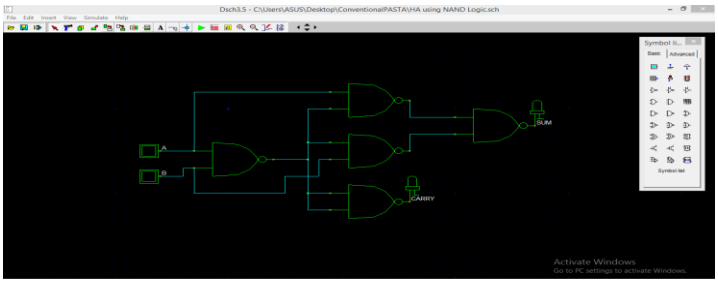

Fig-4:- Half adder using NAND Gates

C) Half Adder as Proposed in paper [11]

Thus the half adder as proposed in paper [11] uses 16T (10T for sum module and 6T for carry module).

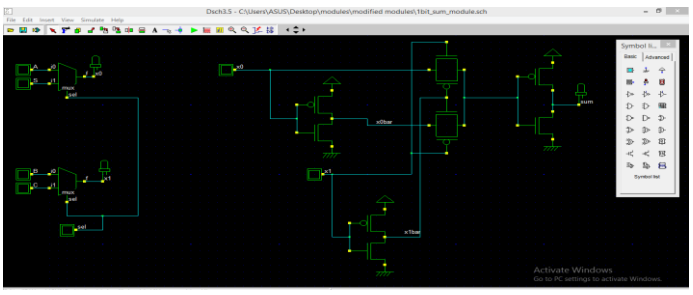

Fig-5 :-1 Bit sum module

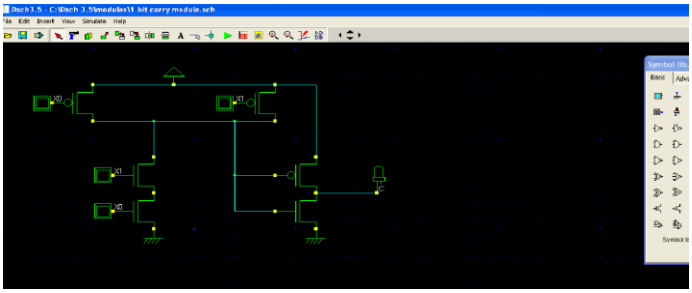

Fig-6 :-1 Bit carry module

D) Proposed Half Adder design

Fig.7 explains proposed schematic of EX-OR with 6 transistors. This schematic uses a new design concept of X-OR gate using transmission gate with two inverter circuits This optimized EX-OR using pMOS and nMOS transistor is used for SUM side in half adder and in carry side again AND gate is replaced by NAND & NOT gate. Thus the proposed circuit requires only 12T for its implementation using CMOS technology.

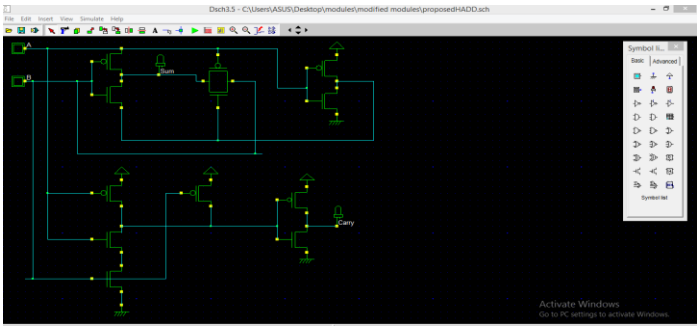

Fig-7: Proposed Half Adder

Table -2: Transistor count for different half adder circuits.

Different Adder circuits	Half adder using logic gates	Half adder using NAND gate	Half Adder as Proposed in [11]	Proposed Half Adder
Number of Transistor count	28T	20T	16T	12T

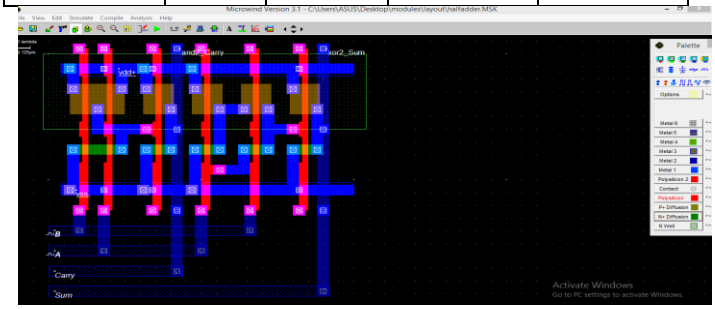

Fig-8 :- Layout of proposed half adder

3.2.2 Multiplexer

The multiplexer or MUX is a digital switch, also called as data selector. It is a combinational circuit with more than one input line, one output line and more than one select line. In PASTA 2:1 MUX is used. Fig.9 shows general diagram of 2:1 MUX.

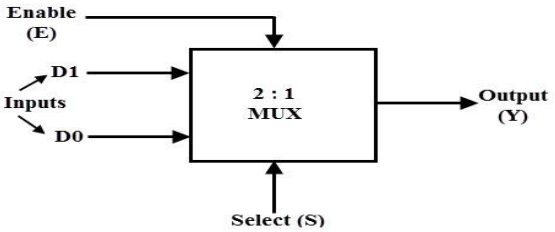

Fig-9:- Block diagram of 2:1 Multiplexer

A)2:1 MUX using basic logic gates.

The below logic circuit of 2:1 MUX requires 2 AND gates, 1 OR gate and a NOT gate. If the circuit in Fig.10 is implemented using pMOS and nMOS then the circuit requires 6T for two AND gates each, 6T for OR gate and 2T for NOT gate. This means, the circuit shown below requires 20T for its implementation.

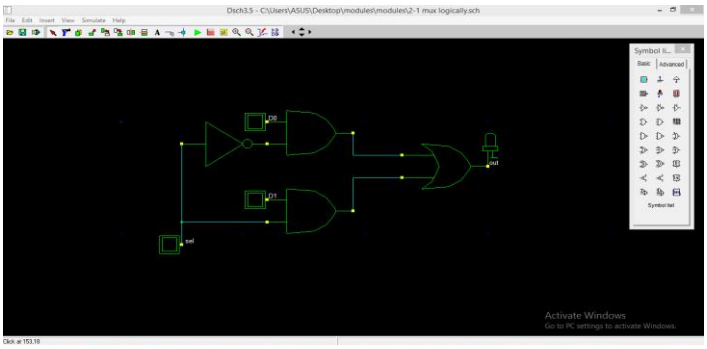

Fig-10 :- 2:1 MUX using basic logic gates

B) 2-1 MUX using NAND Gates

The circuit in Fig.11 requires four NAND gates which means when using pMOS and nMOS the above circuit requires 16T(4T for each NAND gate).

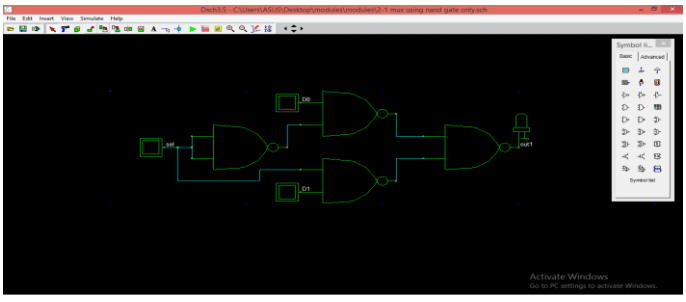

Fig-11 :- 2:1 MUX using NAND gates

C) 2:1 MUX using as proposed in paper [11]

The CMOS implementation as proposed in paper requires 4T in the pull-up network, 4T in pull-down network and 2T for inverter .The circuit in total requires 10T, which are less compared to previous circuits. The circuit is as shown in Fig.12.

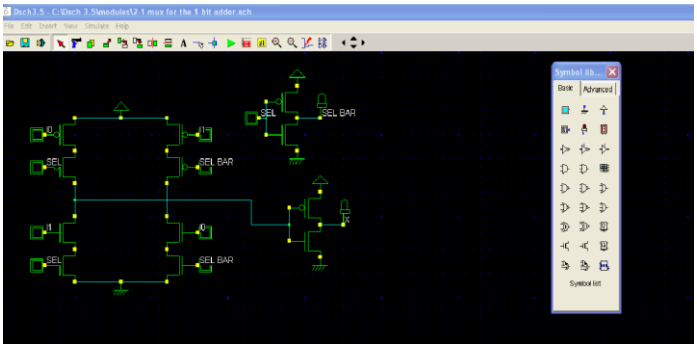

Fig-12:- 2:1 MUX as proposed in paper [11]

D) Proposed 2:1 MUX

The schematic diagram of proposed 2:1 MUX is as shown in Fig.13. This circuit is designed with the help transmission gate and MOS transistors. The MUX will operate based on SEL input. The proposed circuit uses 6T for 2:1 MUX design.

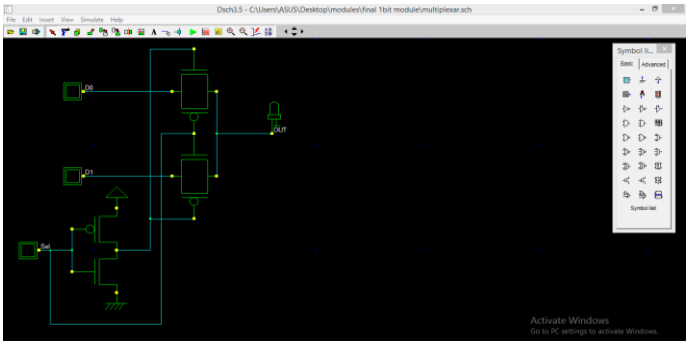

Fig-13:- Proposed 2:1 MUX

Table-3 :- Transistor count for different 2:1 MUX

Different 2:1Mux circuits	2:1Mux using logic gates	2:1Mux using NAND gate	2:1Mux as Proposed in [11]	Proposed 2:1Mux
Number of Transistor count	20T	16T	10T	6T

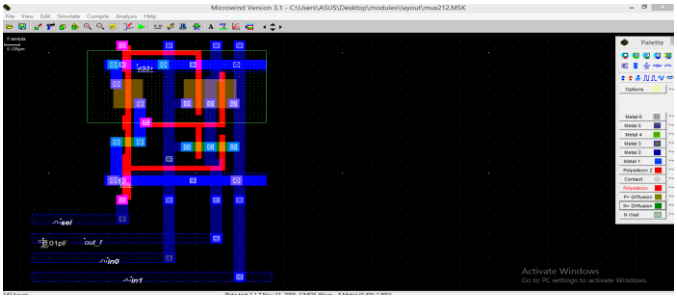

Fig-14 :- Layout of 2:1MUX

3.2.3 Completion Detection Circuit

The completion detection circuit is very critical to the asynchronous adder design. In order to achieve high performance self-timed asynchronous circuits, the key is to design fast completion detection. Its speed will inherently limit the overall performance of the asynchronous adder. The completion detection is negated to obtain an active high completion signal (TERM).

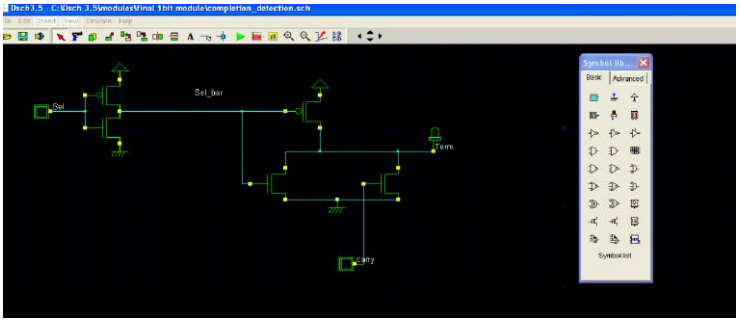

Fig-15 :- Completion detection circuit

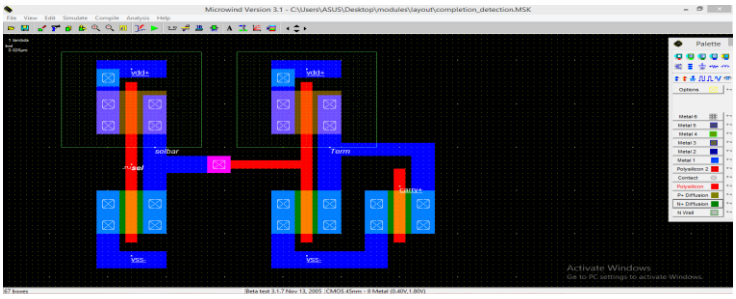

Fig-16 :- Layout of completion detection circuit

3.3 4 bit Parallel Self-Timed Adder

By using the proposed circuits discussed earlier we have designed a 4 bit parallel self-timed adder. The schematic of 4 bit PASTA is as shown in Fig17. The four bit PASTA module is formed by cascading the single bit adder module.

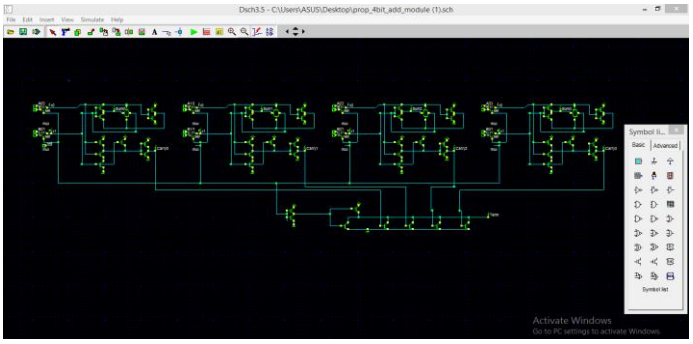

Fig-17 :- Schematic of 4 bit PASTA

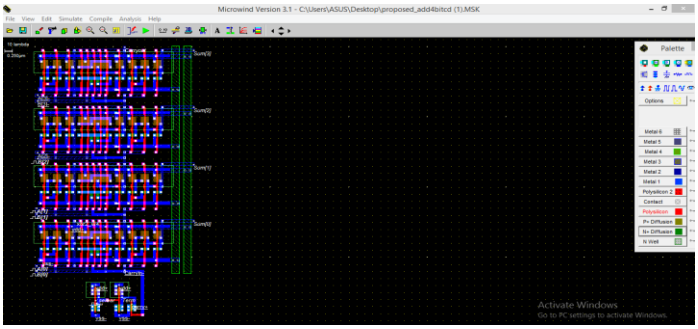

Fig-18 :- Layout of 4 bit PASTA

4. RESULTS & DISCUSSION

4.1 Simulation Results

The simulated results of implemented design for conventional approach and proposed approach of Parallel Self-Timed Adder are shown below. All the circuits are designed, simulated and the performance is evaluated based on power, delay, frequency and area/size etc. Here for the design using VLSI technology Microwind3.1 software is used.

A)Half Adder

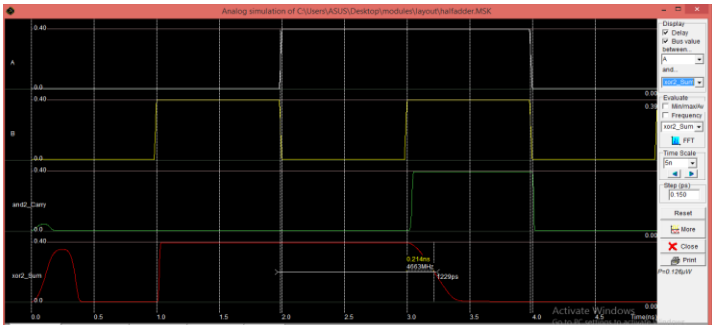

Fig-19:- Input and Output Waveform of Half Adder

B) 2:1 MUX

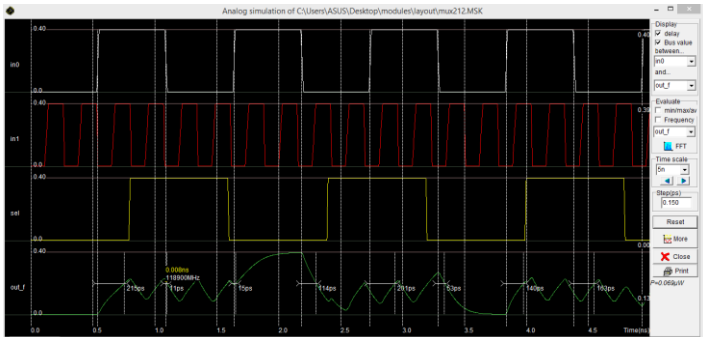

Fig-20 :- Input and Output Waveform of 2:1MUX

C) Completion Detection Circuit

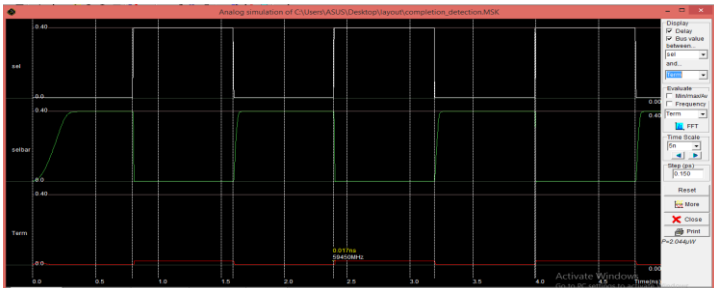

Fig-21 :- Input and Output Waveform of completion detection circuit.

D) 4 bit Parallel Self-Timed Adder

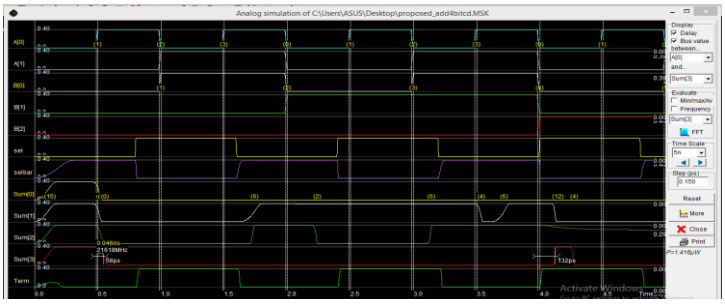

Fig-22 :- Input and Output Waveform of 4 bit PASTA

4.2 Results and Discussion

Table-4 represent the performance parameters analysis of the proposed circuits. We have evaluated the parameters based on number of transistor required, propagation delay, area, power and maximum frequency etc. The superiority of proposed approach can be determined by comparing the previous and proposed circuit in terms of power, delay and area of Self-Timed Adder. The 4 bit self timed adder as proposed in [12] is simulated in 130nm Faraday bulk CMOS process technology using Synopsys and Cadence tools on a Linux platform which has delay of 2.06ns, power as 19.09uW and area estimated as 775um2. Whereas the proposed 4 bit PASTA is simulated in Microwind 3.1tool which has better

performance exhibiting delay of 0.046ns, power as 1.416uW and area calculated as 48.85um2 as shown in below Table-4.

Table-4 :- Parameter analysis of the Proposed Circuits

Circuit Parameters	Proposed Half Adder	Proposed 2-to-1Mux	Completion detection circuit	Proposed 4 bit PASTA
No. of transistor Required	12T	6T	5T	101T
Propagation Delay	0.214ns	0.008ns	0.017ns	0.046ns
Area	6.25um2	5.1875um2	1.74um2	48.85um2
Power	0.126uW	0.069uW	2.044uW	1.416uW
Maximum Frequency	4.67*10[9] Hz	125*10[9] Hz	58.82*10[9] Hz	21.739*10[9] Hz

3. CONCLUSION

In this paper we implemented the Modified PASTA. Initially, the theoretical foundation for a single-rail wave-pipelined adder is established. Subsequently, the architectural design and CMOS implementations for Parallel Self-Timed Adder are presented. The new design using transmission gate and CMOS transistor is proposed and implementation is done using 45nm CMOS technology. With the proposed design, the reduction in number of transistor count is achieved as compared with previous CMOS implementation of PASTA. This achieves a very simple n-bit adder that is area, power consumption wise much more efficient than the previous self timed adder with this, we also designed 4bit parallel self timed adder and analyzed the same for various performance parameters. Moreover, the circuit works in a parallel manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. Simulation results are used to verify the advantages of the modified self timed adder.

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