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A Single Ended SRAM cell with reduced Average Power and Delay

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Abstract- *The increasing demand for high density VLSI circuits and dependency on power and delay is becoming a major challenge. Balancing these requirements is driving the effort to minimize the footprint of SRAM cells. In this work, a single ended bitline approach is used to reduce the power and delay requirements. This cell has been designed and simulated using 90nm technology using cadence on a virtuoso platform.*

Keywords: SRAM, low power, CMOS, Scaling, power dissipation.

I. INTRODUCTION

SRAM cells are used in almost all the digital systems and high performance processors. The usage of sram has continuously increased in system on chip (soc) designs. 70% of SoC area is occupied by SRAM. SRAM is mainly used for cache memory in microprocessor, mainframe computers, engineering workstations memory in handheld devices due to high speed and low power consumption[1].

According to moore's law, the number of transistor on a chip doubles in every eighteen months. With increasingly popularity of a chip memory in VLSI circuits, the range of single chip memory has drastically increased. But with increase in size and density, power consumption and delay increases as well. In digital CMOS circuits, switching power is dissipated when energy is drawn from power supply to charge up the output node capacitance. More than 40% of the active energy is consumed because of leakage currents in modern high performance processors. An array of SRAM cells is a major source of leakage currents in modern high performance processors because a large number of transistors are used in today's on chip cache memory. Thus it is essential to design a low leakage SRAM cell. In order to reduce the power consumption, the methodologies that are generally used to degrade the response time. By reducing the supply voltage Vdd, dynamic power decreases four times and first order leakage power decreases in a linear manner. Thus by operating the cell in subthreshold region, it is possible to achieve low power cell[3]. A conventional 6T SRAM cell poor read stability when operated at low supply voltage. In this paper we propose using of a single ended SRAM cell in the memory array in order to reduce power and delay using cadence tool on virtuoso platform in 90nm technology.

II. SRAM ARCHITECTURE

The memory circuit is said to be static if the stored data can be retained indefinitely i.e. as long as a sufficient power supply voltage is provided, without any need of a periodic refresh operation. A SRAM cache consists of an array of bistable memory bitcells along with peripheral circuits. These peripheral circuits enable reading and writing into the array. SRAM can be organised as bit oriented or word oriented. In bit oriented SRAM, each address accesses a single bit, whereas in a word oriented memory, each address accesses a word of n bits.

An SRAM cell must be designed such that it provides a non destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing. Figure 1 shows a typical SRAM block diagram. SRAM cell transistor ratios that must be observed for successful read and write. Main building blocks are:

1. SRAM Cell
2. Precharge Circuit
3. Write Driver Circuit
4. Sense Amplifier
5. Row Decoder

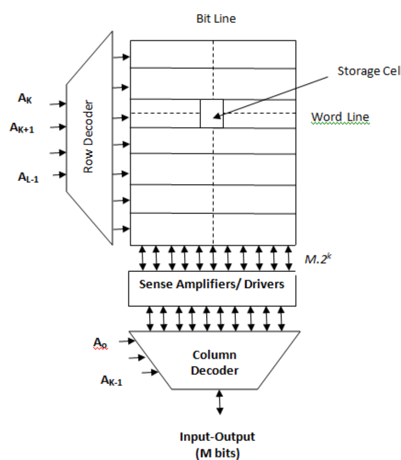

Fig.1 Basic SRAM Architecture

III. SRAM CELL

A conventional 6T SRAM cell consists of two identical CMOS inverters connected in a positive feedback loop as shown in figure 2. It forms a basic unit that is, flip flop or latch to create a bi-stable circuit allowing the storage of one bit of information, either '1' or '0'. The internal nodes (Q and QB) of the bitcell always contain complementary values. The cross coupled inverter pair itself consists of two PMOS pull up devices (M3 & M5) aand two NMOS pull down devices (M2 & M1) which are controlled by wordline (WL), serve as switches between the inverter pair and complementary pair of bitlines (BL and BLB) also called data lines, used to read in or write to the bitcell. The data in SRAM bitcell is stored as long as the power is maintained to the bit cell. The cross coupled inverter pair can be in one of the two stable states of an SRAM bitcell , which corresponds to the data stored '1' and '0' respectively. Basic operation of a bitcell as a storage device are reading or writing new data to the bitcell.

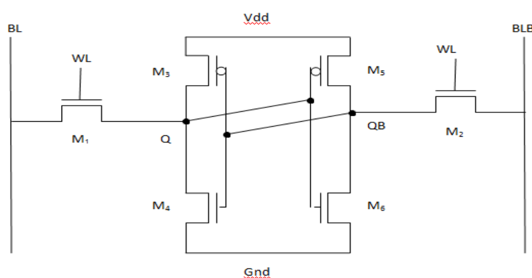

Fig.2 6T SRAM Cell

a. Read operation

i. For the read operation initially it is assumed that storage nodes Q and QB are at '0' and '1' respectively.

ii. BL and BLB are precharged to Vdd or an intermediate level of 0 and Vdd.

iii. WL is risen from '0' to '1' . As a result, one of the bitcell node stores the logic '0'. That side of bitline is discharged through the pass gate and pull down transistors. M1 and M4 discharges the precharged bitlines BL.

iv. If BLB goes low or discharges, then the bitcell holds a logic '1' value. If BL goes low or discharges, then bitcell holds a logic '0' value as shown in the figure 3. Depending upon whether the bitline BL or BLB is discharged, the bitcell is read as logic 1 or 0. A sense amplifier converts the differential signal existing on BL and BLB to a logic level output.

v. The wordline is then de asserted back to 0.

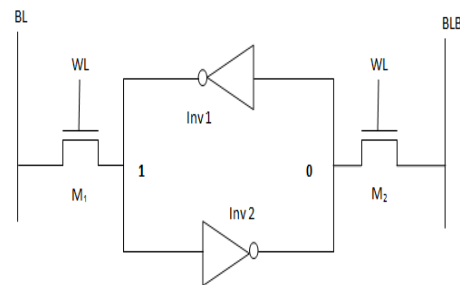

Fig 3. SRAM bitcell 1

b. Write operation

i. For write operation it is initially assumed that internal data storage nodes Q and QB are at '0' and '1' respectively. Initially wordline WL=0.

ii. The bitlines are precharged to supply voltage Vdd and then disconnected.

iii. Wordline (WL) is activated to high and data enters the bitcell.

iv. Data value is placed on the BL and the complementary data value on BLB.

v. The bitline BLB connected to the data storage node QB via M_2 is driven to the ground potential by a write driver through the M_2 pass gate transistor, while BL is remained held at Vdd to pull node Q to high via M_1 pass gate transistor.

vi. Wordline is de-asserted back to 0 as node Q and QB flip their states.

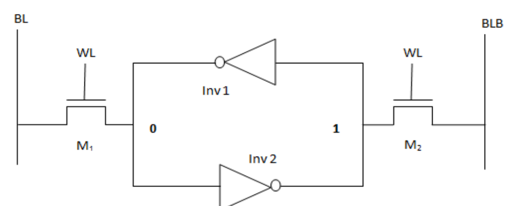

Fig 4. SRAM bitcell 0

IV. SINGLE ENDED SRAM CELL

There are two primary areas having strong potential of active as well as the leakage power reduction: a) lowering the operating voltage which has quadratic dependency with active power.

$$P_{active} = \alpha.C.V^2_{dd}.f$$

and linear relationship with leakage power and b) reduction in charging the capacitance of word and bit lines.

70% of the total active power is dissipated in charging or discharging the capacitance of word and bit lines during read and write operations.

Reduction in charging or discharging capacitance of a word or bit line can be achieved either by having fewer word or bit lines for accessing a bit cell, or by the partial activation of multi divided word or bit lines. It has two advantages, apart from saving of active and leakage power: a) use of fewer word and bit lines reduces the silicon overhead and b) a divided word or bit line configuration will reduce the wire delay.

Such a cell with single bitline is used for reduced power and delay. Figure 5 shows the single ended SRAM bitcell design. This design consists of a cross coupled inverter pair connected in a positive feedback. The inverter pair is connected to a read or write bitline (V_{BL}) by an access transistor M_1 which is controlled by a write word line (WWL). A separate read port used for reading the content of the bitcell comprises of transistor M_{1R} and M_{2R}. The read or write bitline is connected to ground if the node QB and RWL are high, which corresponds to '0' bit is stored in the bitcell. Similarly, if node QB is low and RWL is high, V_{BL} is approximately kept high, which corresponds to '1' bit is stored in the bitcell. Transistor M_2 in read port is controlled by the read wordline (RWL) to read the bitcell content and it is shared per word.

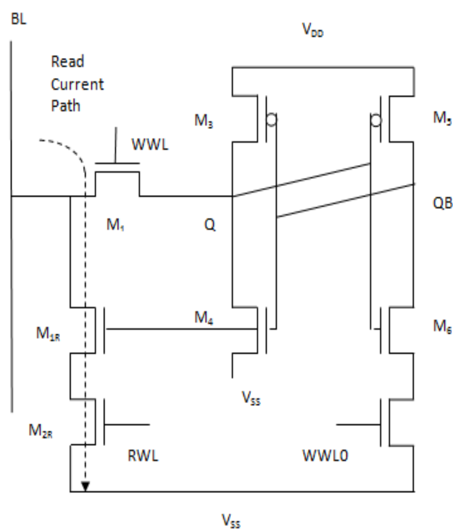

Figure 5. Single Ended SRAM Cell

V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A conventional 6T SRAM cell along with a single ended SRAM cell are designed and simulated using cadence tool on virtuoso platform using 90μm technology.

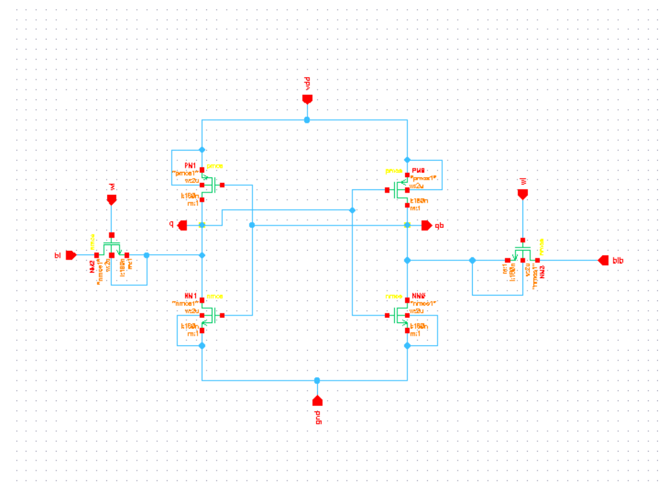

Fig.6 Schematic of 6T SRAM Cell

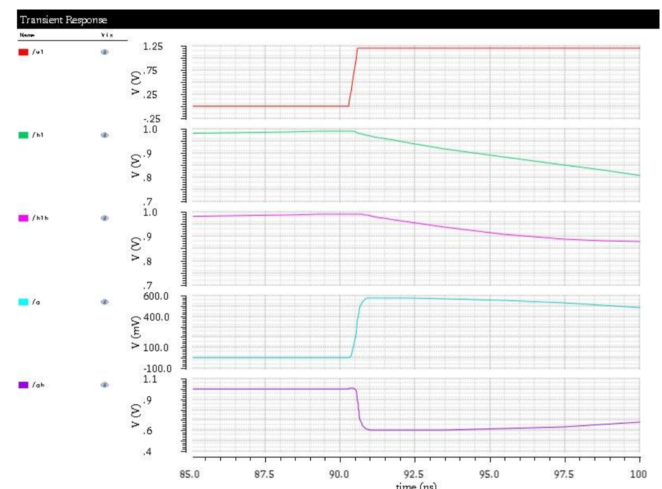

Fig.7 6T Read Operation Waveform

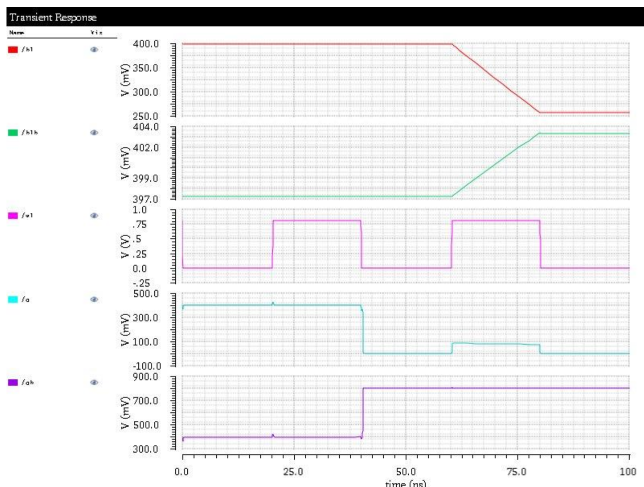

Fig.8 6T Write Operation Waveform

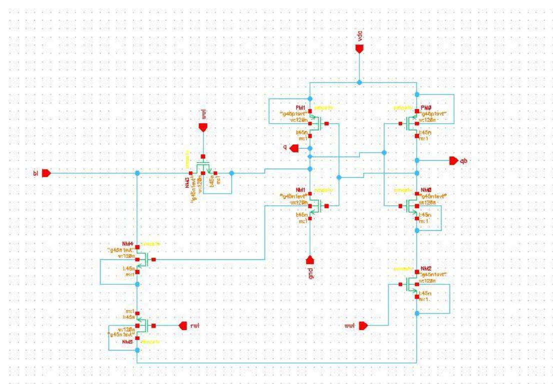

Fig.9 Schematic of Single Ended SRAM Cell

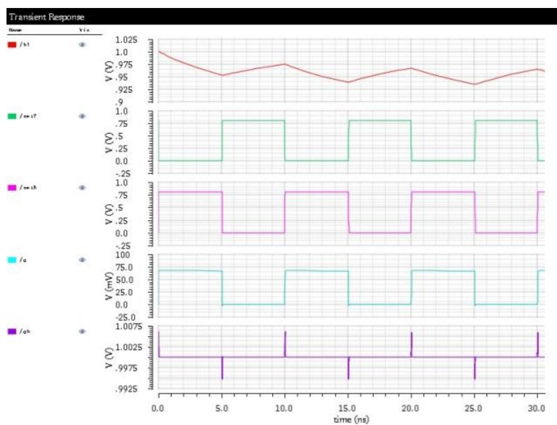

Fig.10 Single Ended Read Operation Waveform

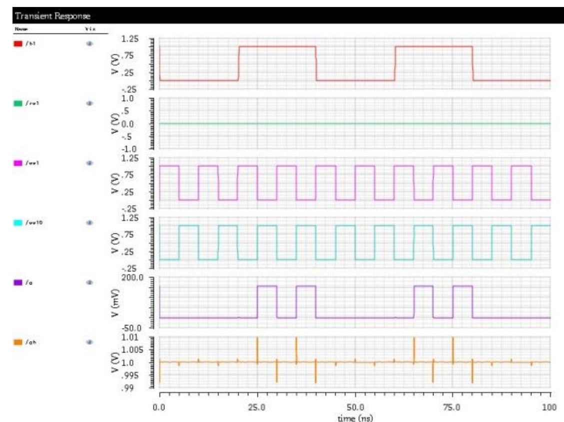

Fig.11 Single Ended Write Operation Waveform

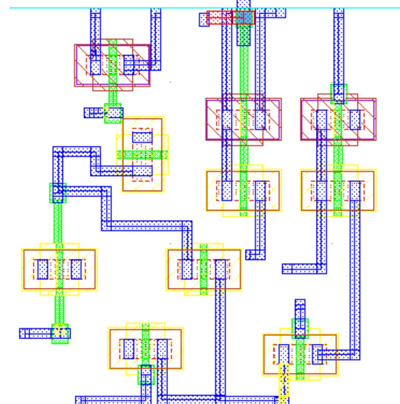

Fig.12 Layout of Single Ended SRAM Cell

VI. CONCLUSION

A 1V, 6T SRAM cell and single ended bitcell were implemented. Using of a single bitline instead of two, saves active as well as leakage power and delay.

Type of SRAM unit	6T SRAM Cell	Single Ended SRAM Cell	Comparison
Delay(ns)	3.001	2.270	24%
Read Power (mW)	6.95	2.068	70%
Write Power (mW)	1.935	1.013	47%

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