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Voltage Controlled Oscillator Design for PLL

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Abstract - ***In spread spectrum, the code or clock synchronization is an important step in the decoding process. A digital phase locked loop can have many uses. If the data bits or clock bits are out of phase then the decoded bits could be decoded incorrectly. Also, if the decoder tries to decode the bits away from the centre of the bits then slight variations could cause the decoder to decode the wrong bit. Voltage controlled oscillator and Frequency division is the concept which is used in many electronics circuits. In the paper we have used the concept for frequency synthesizer used for PLL. The VCO is developed for PLL applicable for FM application with the help of VHDL programming language in Xilinx 14,2 software and the same is synthesized on SPARTAN 3E FPGA.***

Key Words: *Phase Lock Loop (PLL), Field Programmable Gate Array (FPGA), Very High Speed Integrated Circuit Hardware Description Language (VHDL).*

1. INTRODUCTION

Phase locked loops are closed-loop feedback systems consisting of both analog and digital components including a voltage controlled oscillator. They are used for the generation of an output signal the frequency of which (or that of a signal derived from it) is synchronized or locked to that of a reference input. Phase locked loops are used in many applications including signal generation, frequency synthesis, frequency modulation and demodulation, tone recognition, signal detection and filtering. They are available as reasonably priced integrated circuits and are often referred to in the abbreviated form as PLLs. PLL includes a frequency divider.

$$f_d = f_{ref} = \frac{f_{out}}{N} \quad Equtation(1)$$

$$f_{out} = N f_{ref} \quad Equation(2)$$

The signal of frequency fd is generated by dividing the output frequency/out by a factor of Abusing a digital frequency divider circuit. This signal is compared to the reference input, fref by the phase detector. The output voltage of this is a function of the phase difference of the two inputs. The low-pass filtered output of the phase detector is used to control the frequency of the VCO. When the system is 'in lock' condition. Since the divisor N is easy to change in practice, a wide range of frequencies can be generated from a single reference. These frequencies have the accuracy and long-term stability of the original reference.

2. DESIGN OF VCO

The circuit of a frequency phase-locked loop is shown in Fig 1. Ideally, the voltage-controlled oscillator (VCO) is set to produce an output frequency equal to fi when its input voltage is zero. The phase sensitive detector (PSD) is a circuit which produces an output voltage dependent upon the phase difference between its two input signals.

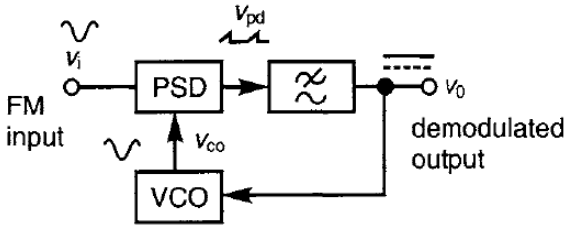

Fig. 1: A PLL used as an FM demodulator circuit as phase-sensitive detector and VCO

There are several types, many of which produce zero output, after filtering, only when their inputs have a 90° phase difference. For simplicity, let's assume that ours produces zero output for zero phase difference. In the working of PLL, First, consider the situation when the FM input signal V_i is unmodulated, so its frequency is fi. Assume the output from the VCO is fi too, so the output from the PSD and filter is zero. With zero input, the VCO produces fi as we assumed. Now consider an input signal Vi with increased, constant frequency. The waveforms of Fig. 2 apply to this case. Notice that the phase of the VCO lags that of Vi. As a result, the output of the low-pass filter

is a positive d.c. level. This is also the output of the PLL. This d.c. level is necessary to cause the VCO frequency to increase, to equal that of Vi. In this way the loop ensures that the frequency of the VCO tracks that of the modulated input signal. So the PPL output, which is also the VCO input, increases positively as input frequency increases, and increases negatively when the input frequency decreases. If the VCO is a type with frequency H nearly-related to its input voltage, then the PLL output, which is also the VCO input, is linearly-related to the modulated input signal's frequency. Thus the phase-locked loop provides an FM demodulator, with linearity equal to that of its VCO.

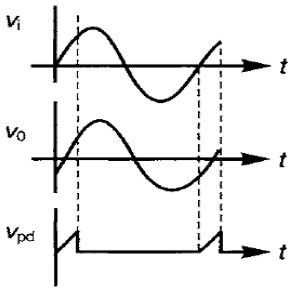

Fig. 2: Wave forms of the VCO

The most linear VCOs are square wave types. These are limited to frequencies of a few megahertz, which rules out their use at higher carrier frequencies. However, such carriers are usually shifted down in frequency, in the receiver, to an intermediate frequency (IF) at which demodulation takes place.

3. RESULTS & DISCUSSION

The Register Transfer Level (RTL) view of the developed chip of FM demolator is shown in Fig.3 and function simulation in Modelsim foftware is shown in Fig. 4. In the simulation results the clk and reset are the default input used for the synchronization and clock signal gives the clock pulse signal. The input signal of VCO is of 12 bit din (11:0) and output is dout(7:0) which can be count the VCO sequence upto 0-255.

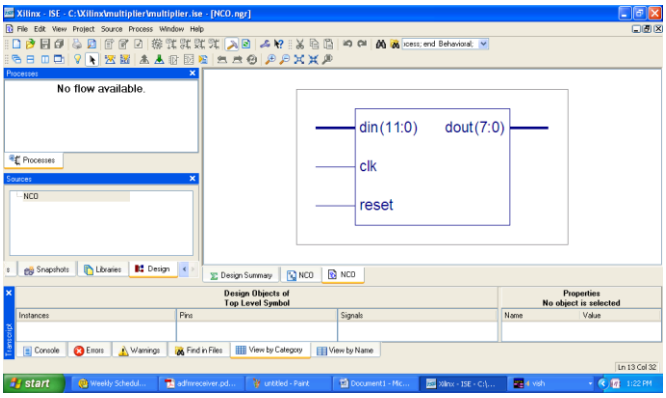

Fig. 3: RTL view of VCO

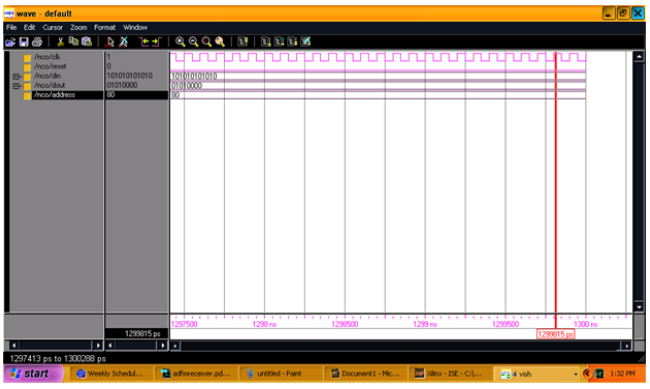

Fig.4: Modelsim result of VCO

HARDWARE SYNTHESIS SUMMARY

Device utilization report gives the percentage utilization of device hardware for the chip development of the chip. Device utilization report provides the information of no. of slices, no. of flip flops, no. of input LUTs, no. of bounded IOBs, and no of gated clocks (GCLKs) used in the implementation of design. Timing details are helpful in analysing the timing performance based on the information of delay, timing parameters such as minimum period, maximum frequency, minimum input arrival time before clock and maximum output required time after clock. Table 1 and Table 2 show the synthesis results as device utilization and timing parameters for voltage controller oscillator for PLL.

Table 1 Device utilization in VCO for PLL

Device	Utilization	
Number of Slices	120 out of 12480,	1%
Number of Slice Flip Flops	249 out of 12480,	2%
Number of 4 input LUTs	40 out of 493,	8%
Number of bonded IOBs	45 out of 172,	26%
Number of GCLKs	1 out of 32,	3%

Table 2 Timing parameters in VCO

Timing parameter	Utilization
Minimum period	0.872 ns
Maximum frequency	275.00MHz
Minimum input arrival time before clock	3.70 ns
Maximum time after the arrival of clock	1.870ns
Total memory usage	9635 kB

CONCLUSIONS

In the paper the design of VCO for PLL and FM application is developed with the e help of VHDL programming language. The functional check for the design is carried with different frequencies and tests. The design supports the frequency upto 275 MHZ. the memory utilization is 9635 kB, Minimum input arrival time before clock is 1.870 ns, and Maximum time after the arrival of clock. The results received by the modelsim simulation for the VCO for PLL are successfully synthesised on SPARTAN 3E FPGA.

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