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MODELING AND ANALYSIS OF SERIES-PARALLEL SWITCHED-CAPACITOR VOLTAGE EQUALIZER FOR BATTERY/SUPERCAPACITOR STRINGS

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ABSTRACT:- *Series-Parallel switched-capacitor power converter is reconfigured as a new voltage equalization circuitry for series-connected batteries or super capacitors. The model of the new voltage equalizer is derived and successfully used to analyze the equalization speed and energy loss. It is a very useful tool to analyze and design switched-capacitor-based equalization systems to meet different balancing speed requirements. Large numbers of battery or super capacitor cells are usually connected in series to meet high operating voltage requirements. All series-connected cells are therefore charged and discharge together. Due to non-uniform properties of individual cell, repeated charging and discharging will cause small imbalance in the form of unequal voltages existed among cells. To overcome this problem, the voltage balancing device, also known as a voltage equalizer, is indispensable equipment in battery management systems. Other type of active cell balancing methods is implemented by employing switched-capacitor (SC) as the energy transfer component. It has the advantages of small size and cost-effective as well as easy control. The analysis and modeling methods can be extended to other switched-capacitor-based voltage balancing systems. A prototype is built and the experimental results are also provided to confirm the theoretical analysis and modeling method.*

Keywords: switched-capacitor (SC), super capacitor cells, series-parallel switched-capacitor, Voltage Equalization

INTRODUCTION

Large numbers of battery or super capacitor cells are usually connected in series to meet high operating voltage requirements. All series-connected cells are therefore charged and discharge together. Due to non-uniform properties of individual cell, repeated charging and discharging will cause small imbalance in the form of unequal voltages existed among cells [1], [2]. To overcome this problem, the voltage balancing device, also known as a voltage equalizer, is indispensable equipment in battery management systems [1]-[4]. The main drawbacks of this method are energy waste and the temperature rise. In order to avoid waste of energy during the voltage balancing and make every cell providing the best performance, various active balancers are designed based on switched-mode power conversion circuits in [7]-[18]. The common design philosophy of these strategies is using power converters to transfer energy from the higher voltage cells to the lower ones. Alternatively with high frequency and charge is transferred from the higher voltage battery cells to the lower ones, automatically, causing their voltages change in opposite manner and toward the average value. In order to facilitate the detailed analysis of the equalization process, the following assumptions have been made: all switched capacitors have the same capacitance C and ESR, R_c and there are the same on-resistance R_s for all switches.

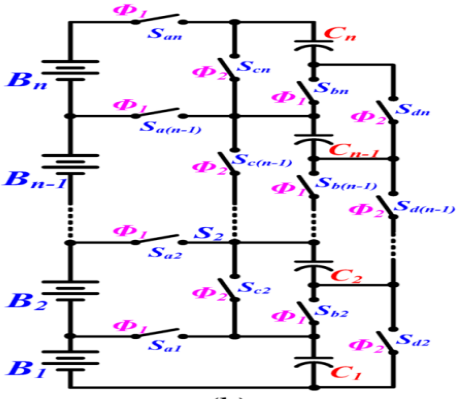

Fig.1. Voltage equalization system implemented by series-parallel switched-capacitor converter

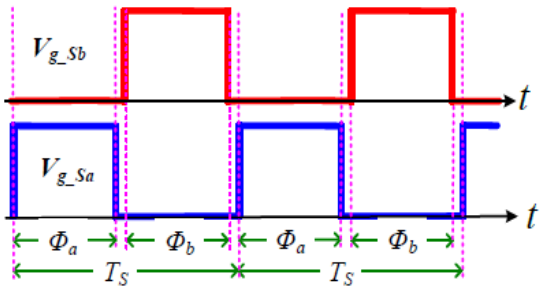

Fig.2. Control signals and time slots of SC equalizers.

B. State Analysis in Clock Phase Φa

In the duration of the phase *Φa*, charge will transfer from the battery cell *Bj* to the capacitor *Cj* when the voltage of *Bj* is higher than the initial voltage of *Cj*, and the capacitor is therefore charged as shown in the lower of Fig.3. The variations of the capacitor voltage and current during the charging process are

Expressed as

$$\emptyset_a: \quad V_{cj}(t) = V_{BJ} - (V_{BJ} - V_{CJ-min})e^{\frac{-t}{rc}} \quad (1)$$

$$\emptyset_a: \quad I_{cj}(t) = \frac{V_{BJ} - V_{CJ-min}e^{\frac{-t}{rc}}}{R} \quad (2)$$

where *VCj_min* is the initial voltage of *Cj* during the phase *Φa*; *VBj* is the voltage of the cell *Bj* and it could be seen as a constant when the capacity of *Bj* is far larger than *C*; *r* is the sum of the ESR of the capacitor and the on-resistance of the switches *Saj1* and *Saj2*, i.e. *r=rc+2rs*.

As shown in the upper of Fig.3, in contrast, the capacitor *Ck* will discharge to the battery cell *Bk* when its initial voltage *VCk_max* is higher than the battery cell's voltage *VBk*. Another type of active cell balancing methods is implemented by employing switched-capacitor (SC) as the energy transfer component [19]-[23]. It has the advantages of small size and cost-effective as well as easy control. According to literatures [24]-[32], the performance of SC power conversion circuits can be seen as a combination of an ideal transformer and an equivalent resistor. It shows the power transfer capacity of SC power conversion circuits mainly depends on the switching frequency and the value of switched capacitors. Specific to SC-based voltage equalization systems, the voltage balancing speed can be directly reflected by the model of the SC balancing circuitry. The model is therefore a useful tool to evaluate the performance of a SC-based cell balancer and to guide the design work in practice. In the relevant literatures, unfortunately, this topic is discussed rarely.

In this paper, the series-parallel SC converter proposed in [28] and further developed in [29]-[31] is reconfigured as a new voltage balancing circuitry. Its circuit configuration and operation principle are introduced in Section II. And the model is derived based on its state analysis in Section III. By using the derived model, the voltage balancing speed and energy conversion loss are discussed in Section IV. In Section V, a four-cell voltage equalizer prototype is built and the experimental verification is given. Finally, the paper is concluded in Section VI.

II.SERIES-PARALLELSCVOLTAGEEQUALIZER

A. Circuitry Description and Operation Principle

As shown in Fig.1, the series-parallel SC voltage equalizer is composed of multiple SC units. Each SC unit is made up of a switched capacitor *Ci* and four transistors *Sai1*, *Sai2*, *Sbi1* and *Sbi2*. The same as the conventional two-phase SC converters [31], the SC voltage balancing circuit is also controlled by a pair of complementary pulse signals with reasonable dead time. There are therefore two clock phases' *Φa* and *Φb* as indicated in Fig.2. During the phase *Φa*, all switches *Sai1* and *Sai2* (*i=1, 2…… n*) are turned ON, simultaneously, while switches *Sbi1* and *Sbi2* being OFF. As a result, the switched capacitor *Ci* is connected in parallel with the battery cell *Bi* and being charged by or discharges

to the battery cell as shown in Fig.3. During the phase *Φb*, switches *Sbi1* and *Sbi2* are turned ON whereas *Sai1* and *Sai2* are OFF. All capacitors are therefore connected in parallel manner and charge flows from the higher voltage capacitors to the lower voltage ones as given in Fig.4. The two states operate variations of the capacitor voltage and current during the discharging process are given as

$$\emptyset_a:\ V_{CK}(t) = V_{BK} + (V_{CK-min} - V_{BK})e^{\frac{-t}{rc}} \quad (3)$$

$$\emptyset_a: \qquad I_{CK}(t) = \frac{(V_{CK-max} - V_{BK})}{R} e^{\frac{-t}{rc}} \quad (4)$$

where VCk_max is the initial voltage of Ck and VBk is the voltage of the cell Bk during the phase Φa.

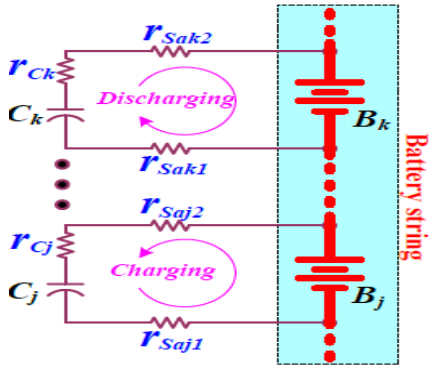

Fig.3. State circuit of new SC equalizer during the phase *Φa*

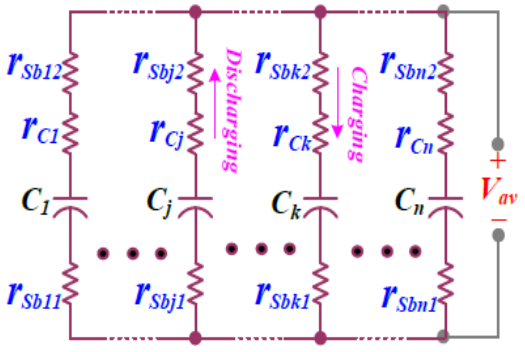

Fig.4. State circuit of new SC equalizer during the phase Φb.

B. State Analysis in Clock Phase Φb

In the duration of the phase *Φb*, all switched capacitors are connected in parallel as shown in Fig.4. *Vav(t)* is the common voltage of all SC paralleled branches, i.e.

$$V_{av}(t) = V_{ci}(t) - rI_{ci}(t) \quad (5)$$

Where *i* is ranged from *1* to *n*; *VCi(t)* is the instantaneous voltage of *Ci*; *ICi(t)* is the instantaneous capacitor current and being positive for charging while negative for discharging. The common voltage *Vav(t)* can be also expressed as

$$V_{av}(t) = \frac{1}{n}\sum_{i=1}^{n}[V_{ci}(t) - rI_{ci}(t)] \quad (6)$$

By using Kirchhoff's current law (KCL) at any one of the two common points of all paralleled branches in Fig.4, the KCL equation could be obtained as given in (7).

$$\sum_{i=1}^{n} I_{ci}(t) = 0 \quad (7)$$

When the KCL equation (7) is substituted into (6), the common voltage *Vav(t)* could be further expressed by (8)

$$V_{av}(t) = \frac{1}{n}\sum_{i=1}^{n}[V_{ci}(t)] = \frac{1}{nc}\sum_{i=1}^{n} q_{ci}(t) = \frac{q_{total}}{nc} \quad (8)$$

Where $q_{ci}(t)$ *the amount of charge stored in the capacitor Ci and qtotal is* is the total amount of charge of all capacitors.

During the phase *Φb*, charge transfers from the higher voltage capacitors to the lower ones. The total amount of chargeq_{total}, however, is constant and the voltage *Vav (t)* is therefore can be seen as a constant voltage source *Vav* during the phase *Φb*.

For the capacitor *Ck* with the initial voltage *VCk_min*, it will be charged by the constant voltage *Vav* during the phase *Φb*. The variation of the capacitor voltage and current during the charging process can be expressed as

$$\emptyset_b: V_{ck}(t) = V_{av} - (V_{av} - V_{ck-min})e^{\frac{t}{rc}} \quad (9)$$

$$\emptyset_b: I_{ck}(t) = \frac{(V_{av}-V_{ck-min})}{R} e^{\frac{t}{rc}} \quad (10)$$

Similarly, the capacitor *Cj* with the higher initial voltage *VCj_max* will discharge to the constant voltage source *Vav* and the capacitor voltage and current are given by

$$\emptyset_b: V_{cj}(t) = V_{av} + (V_{cj-max} - V_{av})e^{\frac{-t}{rc}} \quad (11)$$

$$\emptyset_b: I_{cj}(t) = \frac{(V_{cj-max}-V_{av})}{R} e^{\frac{-t}{rc}} \quad (12)$$

III. MODELING FOR SC VOLTAGE EQUALIZER

Assuming each switching cycle is divided by the two clock phases *Φa* and *Φb* evenly, the maximum and minimum values of capacitor voltage *VCj* obtained at the end of the phases *Φa* and *Φb* are given as $V_{cj-max}=V_{bj} - (V_{bj} - V_{cj-min})e^{\frac{-1}{2rcf}}$ (13) $V_{cj-min}=V_{av} + (V_{cj-max} - V_{av})e^{\frac{-1}{2rcf}}$

Where *f=1/TS* is the switching frequency.
Different relationships of the voltages *VBj* and *Vav* can be therefore derived from (13) as given

$$V_{bj} + V_{av} = V_{cj-max} + V_{cj-min} \quad (14)$$

$$V_{bj} + V_{av} = (V_{cj-max} + V_{cj-min})\frac{1+e^{\frac{-1}{2rcf}}}{1-e^{\frac{-1}{2rcf}}} \quad (15)$$

Similarly, the minimum and maximum values of capacitor voltage *VCk* are obtained at the end of the phases *Φa* and *Φb* are expressed as

$$V_{ck-min} = V_{bk} + (V_{ck-max} - V_{bk})e^{\frac{-1}{2rcf}} \quad V_{ck-max} = V_{av} - (V_{av} - V_{ck-min})e^{\frac{-1}{2rcf}} \quad (16)$$

And the different relationships of the voltages *VBk* and *Vav* can be also derived from (16) as given in $V_{bk} + V_{av} = V_{ck-max} + V_{ck-min}$ (17)

$$V_{av} - V_{bk} = (V_{ck-max} + V_{ck-min})\frac{1+e^{\frac{-1}{2rcf}}}{1-e^{\frac{-1}{2rcf}}}) \quad (18)$$

Expanding the equations (14) to all SC units corresponding higher voltage battery cells and (17) to all SC units corresponding lower voltage cells, respectively, a new equation could be derived and given as

$$\sum_{i=1}^{n} V_{bi} + nV_{av} = \sum_{i=1}^{n} V_{ci-max} + \sum_{i=1}^{n} V_{ci-min} \quad (19)$$

Applying the equation (8) at both of the start and the end moments of the phase *Φb*, another new equation could be derived and given as

$$\sum_{i=1}^{n} V_{ci-max} + \sum_{i=1}^{n} V_{ci-min} = 2\frac{q_{total}}{nc} = 2V_{av} \quad (20)$$

The common voltage *Vav* can be therefore derived by substituting (20) into (19) and expressed as

$$V_{av} = \frac{1}{n}\sum_{i=1}^{n} V_{bi} \quad (21)$$

During one switching cycle, the average current *IBi* flowing into or out of the battery cell *Bi* could be obtained by dividing the switching cycle *TS* into the total charge *C(VCi_max-VCi_min)*. The equations (15) and (18) can be therefore further developed as

$$V_{av} = V_{bi} - I_{bi}R_{sc} \quad (22)$$

$$V_{av} = V_{bk} + I_{bk}R_{sc} \quad (23)$$

where *RSC* is the equivalent resistance of the switched capacitor power conversion circuit between *VBi* and *Vav* as given below

$$R_{sc} = \frac{1+e^{\frac{-1}{2rcf}}}{cf(1-e^{\frac{-1}{2rcf}})} \quad (24)$$

Though this expression of equivalent resistance is similar to that obtained in [24]-[27], the result will be further used to evaluate the balancing speed and regarded as a design consideration in the next section.

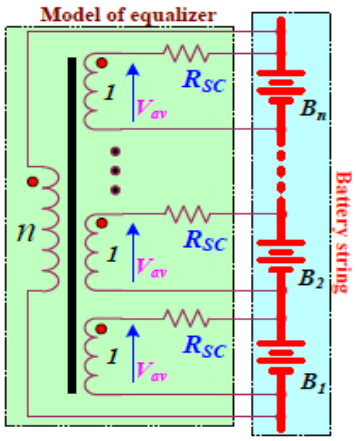

Fig.5. Model of series-parallel SC equalizer

According to above analysis, *Bj* represents any one battery cell with higher voltage and *Bk* represents any one with lower voltage. According to the equations (21), (22) and (23), the model of the series-parallel SC voltage equalizer with battery string can be depicted in Fig.5, where the turns ratio of the ideal multi-winding DC transformer is *n:1:...:1*. It shows the energy can be transferred from the higher voltage cells to the lower ones directly, rather than just be transferred between adjacent cells like the equalization circuit introduced in [19], [21].

IV. MODEL-BASED ANALYSIS OF BALANCING SPEED, ENERGY LOSS AND DESIGN METHOD

A. Balancing Duration

The assumptions that all battery cells have the same capacity *CB* which is measured in Farads, and there is a linear relationship between the cell voltage and the amount of charge storied in the cell, are made to facilitate the analysis. Using symbols *VB1*(0), *VB2*(0), ..., *VBn*(0) as the battery cells' initial voltages. The amount of charge storied in all battery cells could is therefore given as

$$Q(0) = C_b \sum_{i=1}^{n} V_{bi}(0) \qquad (25)$$

With the operation of the series-parallel SC voltage equalizer, charge transfers from the higher voltage cells to the corresponding switched capacitors during the phase *Φa* firstly. And then, these charge flows to other switched capacitors during the phase *Φb*. For the next phase *Φa*, the same amount of charge is released to the lower battery cells. In the power transfer process, there is no charge lost or produced and the total amount of charge is therefore always constant. The average of the battery cells is therefore derived and expressed as below

$$V_{av} = \frac{1}{n}\sum_{i=1}^{n} V_{bi}(t) = \frac{Q(0)}{nc_b} = \frac{1}{n}\sum_{i=1}^{n} V_{bi}(0) \rightarrow (26)$$

It depicts the common voltage *Vav* in the model of Fig.5 is constant for the whole equalization process even though all cell voltages are varied.

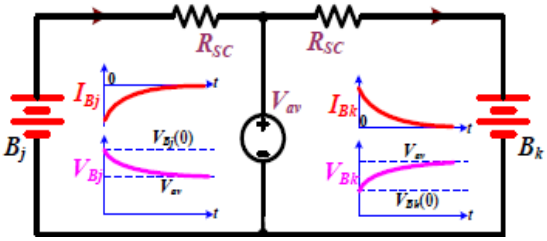

Fig.6. Equivalent circuit of the voltage balancing process.

Hence, the voltage equalization process could be regarded as each separated battery cell discharges to or be charged by the constant voltage source *Vav* as depicted in Fig.6. The balancing process can be therefore expressed as

$$V_{bi}(t) = V_{av} - [V_{av} - V_{bi}(0)]e^{\frac{-t}{R_{SC}C_b}} \qquad (27)$$

$$I_{bi}(t) = \frac{V_{av} - V_{bi}(0)}{R_{sc}} e^{\frac{-t}{R_{SC}C_b}} \qquad (28)$$

For the equation (28), the positive current *IBi*(t) means the battery cell *Bi* is charged by the constant voltage source *Vav* while the negative current means *Bi* is discharged to *Vav*. As time goes on, the cell voltage *VBi* is infinitely close to *Vav* but they are never exactly equal. Hence, using another value *VBi(end)* represents the expected value of the battery cell voltage, the duration of the balancing process can be derived from (27) and given as

$$t = R_{sc}C_b \ln \frac{V_{av}-V_{bi}(0)}{V_{av}-V_{bi}(end)} \qquad (29)$$

After a period of *3RCSCB* to *6RCSCB*, usually, the cell voltage *VBi* is very close to *Vav* and the equalization process can be regarded as finished. It means the balancing time is mainly decided by the capacity of battery cell and the equivalent resistance of the SC equalizer.

B. Energy Conversion Loss Analysis

Energy storied in the battery string, before equalization, is expressed as

$$E(0) = \frac{1}{2}C_B \sum_{I=1}^{n} V_{Bi}^2(0) \qquad (30)$$

At the end, all cell voltages are balanced to the average voltage *Vav* and the total amount of charge is distributed evenly to all battery cells. The energy storied in the battery string is

$$E(\infty) = \frac{1}{2}nC_B V_{av}^2 \qquad (31)$$

Substituting the average voltage expression (21) into (31), the final energy storied in the battery string is further derived as

$$E(0) = \frac{1}{2n}C_B \sum_{I=1}^{n} V_{Bi}^2(0) \qquad (32)$$

The energy conversion loss is therefore derived from (30) and (32) as given by

$$E_{loss} = E(0) - E(\infty) = \frac{C_B}{2}\left\{\sum_{I=1}^{n} V_{Bi}^2(0)\right\} - \frac{1}{n}\left[\sum_{i=1}^{n} V_{Bi}(0)\right] \qquad (33)$$

It can be seen that the energy conversion loss is determined by the initial cell voltage distribution and the ended state instead of the balancing speed. For instance, a supercapacitor string has four series connected cells with initial voltages 2.5V, 2.6V, 2.7V and 2.8V and the rated capacity of each cell is 1F, the total initial energy storied in the four cells is 14.07J. Finally, all cell voltages are fully balanced to 2.65V and the final energy is 14.045J. The energy conversion loss during the balancing process is therefore 0.025J which is the same as that calculated by the equation (33).

C. Design Steps

To meet different requirements of the balancing speed, circuit parameters including the value of capacitors and switching frequency can be determined according the model of SC balancing circuits. The detailed design steps are presented as follows:

1) Estimating the equivalent resistance *RSC* of switched capacitors making reference to (29), i.e.

$$R_{SC} = \frac{t_{req}}{(mC_B)} \qquad (34)$$

Where *m* is constant and can be ranged from 3 to 6; *CB* is the capacity of each battery cell and been measured in Farads; *treq* is the required balancing duration.

2) Selecting the appropriate switching frequency *f* according to the type of switching capacitors.

3) According to the equation (24) and the equivalent resistance *RSC* calculated in the first step to calculate the value of switched capacitors *C.*

V SIMULATION RESULTS

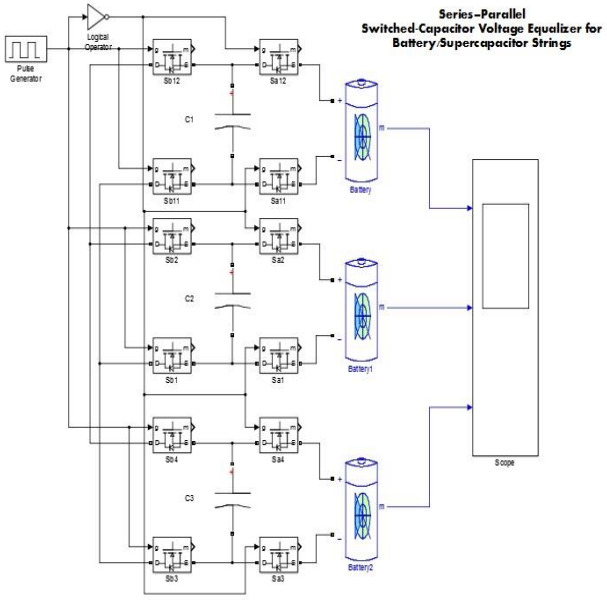

Fig.7 : Simulation diagram

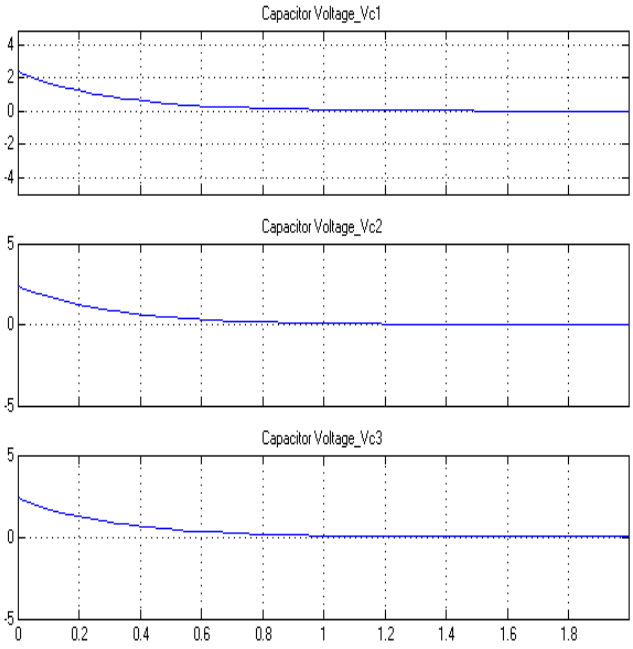

Fig.8. Voltage across capacitors with decreasing waveform.

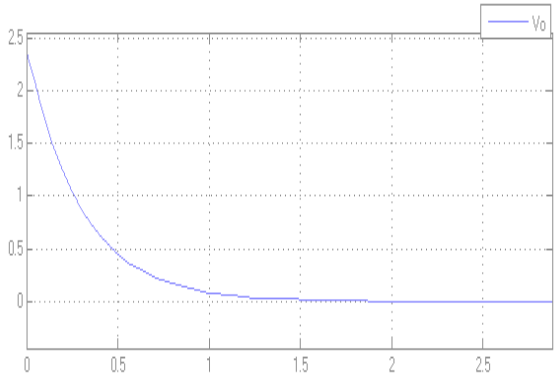

Fig:9. Capacitor Voltage

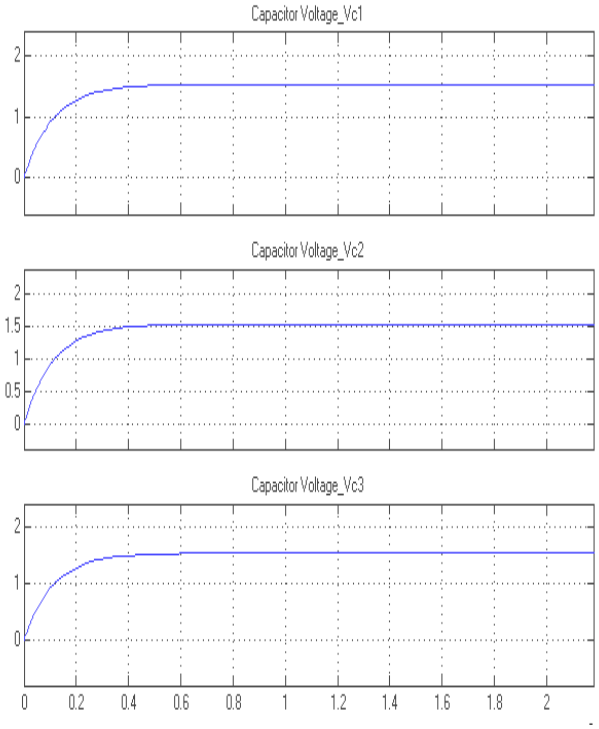

Fig.10:Voltage across Capacitors with increasing waveform.

VI CONCLUSION

The circuit configuration and operation principle of the series-parallel SC voltage equalizer are analyzed in this

paper. Based on the detail state analysis, its model depicted as an ideal DC multi-winding transformer with multiple equivalent resistors is derived. The key of the model is the value of the equivalent resistor that related to the switching frequency and capacitance. Based on the model, the voltage equalization speed can be determined. It is very useful in practice to decide the switching frequency and select appropriate switched capacitors to meet the different balancing speed requirements. The energy conversion loss is also discussed based on the derived model. Furthermore, four-cell equalizer prototype is built in laboratory to verify the theoretical analysis. For the further works, the model-based analysis and design method will be developed and applied to other switched-capacitor-based voltage equalization systems.

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