

Design of Cascode LNA in 65nm CMOS

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Abstract - Demand for fully-integrated RF circuits offering low power consumption continues to grow, along with a strong desire for high performance. A design that enhances the performance of the cascode LNA is detailed in this paper. A new low power, low noise LNA dedicated to implantable biomedical applications is introduced in this work. The Designed circuit has been optimized for high gain, high linearity and low power consumption. RF frequency used for the proposed design is 915MHz i.e. ISM band. The circuit is designed to have a gain of 15dB and the total power consumption of 49 μ W. This design is validated in 65nm CMOS process with the power supply of 0.6V.

Key Words: LNA, CMOS, Inductive source degenerated cascode, Impedance matching, Noise figure.

1. INTRODUCTION

In recent years there has been significant growth in low power wireless technologies. Linearity plays a vital role in the RF systems. Nonlinearity in RF system causes many problems like gain compression, harmonic generation, cross modulation, blocking, desensitization and intermodulation, etc. Nonlinearity in receiver systems such as Low Noise Amplifier (LNA) and Mixers is directly related to the immunity to the various interferences. The performance measure for the nonlinearity is expressed by third order input intercept point (IIP3).

In a receiver front-end, a low noise amplifier needs to attain a large gain and low noise with minimum possible power consumption and area. To realize high gain (>15dB), good linearity and high stability, a Cascode LNA has been proposed. As far as the receiver front-end concern, the need for a low noise amplifier (LNA) is mandatory. Regardless of the type of receiver, the LNA has to provide low noise figure (NF), input matching, high gain. Low current consumption and low silicon area are also required.

This paper presents a Cascode Stage LNA, which is well suited for biomedical applications as it operates at the frequency of 915MHz i.e. ISM band and also suited for low power applications. This amplifier is responsible for amplifying the bio signals, and has to offer low input referred noise and low power consumption.

This paper is organized as follows. Section II reviews the operation of proposed LNA, Section III explains circuit design approach and Section IV proposes the simulated results of the proposed work, while conclusions are wrapped up in Section V.

2. Theory of operation

A schematic of the proposed Cascode LNA is shown in Figure. 3. The Cascode LNA has better reverse isolation and robustness than a CS-LNA. Thus, the use of a Cascode stage improves the stability and bandwidth. The bandwidth of the design increases because of reduction of miller effect in the circuit. Since the gate of M2 can be treated as virtual ground, M2's source voltage and M1's drain voltage are held nearly constant. That means the upper M2 offers a low input resistance to lower M1. This reduces the gain of M1 and as a result the miller effect also get reduced which in turn results in increased bandwidth. The overall gain of the design is not affected by the decrease in gain of M1 because M2 compensates it. M2 is not affected by miller effect because charging and discharging of drain to source stray capacitance is carried out through the drain resistance and the load and the frequency response is affected only for high frequency.

The output of the design is well isolated from its input in cascode configuration. M1 has nearly constant voltage at its drain and source terminals, whereas M2 has almost constant voltage at its source and gate terminals. Basically, there is nothing to feedback from the output to input. The only points with importance in-terms of voltage are the input and output terminals and are well isolated by a central connection of constant voltage.

3. CIRCUIT DESIGN

The main design target of an LNA is to provide 50 Ω input matching on the 915MHz frequency, thus minimizing signal reflections back to the receiver antenna. Of course, high gain and low NF are also essential to reduce the noise contribution to subsequent stages and improve the receiver sensitivity.

To design any analogue circuit, it is necessary to calculate the aspect ratios of all the MOSFETs. In order to calculate the aspect ratios of MOSFETs, magnitude of the

current should be determined and is calculated from below equation,

$$I = C_L \frac{dV}{dt} \quad \text{----- (1)}$$

Where C_L is load capacitance and dV/dt is slew rate.

Slew rate is defined as rate of change of output voltage and is calculated by using output signal frequency and amplitude. Load capacitance is chosen according to the design. By using these two parameters the magnitude of the current I is calculated using equation (1). And then it is important to make all the transistors to operate in saturation region i.e. $V_{ds} > V_{gs} - V_{th}$.

Once the voltages at all nodes are found out then calculate aspect ratio using the saturation current equation given below,

$$I = (\mu C_{ox}/2) (W/L) (V_{gs} - V_{th})^2 \quad \text{----- (2)}$$

And finally load resistors are replaced with active device i.e. PMOS which can be operated as load, and resistance is controlled by over drive voltage.

$$R = 1 / (\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})) \quad \text{----- (3)}$$

Where, μ is carrier mobility, C_{ox} is capacitance per unit area of gate oxide and W and L are the channel width and length respectively. V_t is threshold voltage [7].

To design a Cascode LNA for particular gain, use the following equation (3).

$$A_v \approx -g_{m1} g_{m2} r_{o1} (r_{o2} || r_{o3}) \quad \text{----- (4)}$$

Where, g_{m1} and g_{m2} are transconductance of transistors 1 and transistor 2 respectively.

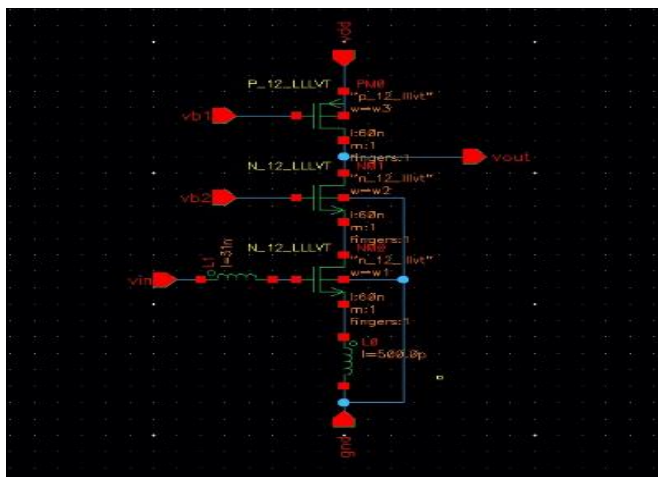


Figure-1: Designed Cascode LNA

4. SIMULATION RESULTS

The proposed circuit of Cascode LNA was designed in Cadence Virtuoso 6.1.6 platform and simulated using the Spectre simulator in Analog Design Environment. This work has been implemented in CMOS 65nm technology. The circuit is simulated with the 0.6V power supply and a RF frequency of 915MHz. The gain obtained from the designed cascode LNA is 14.8dB. The input intercept point is -20dBm. The noise spectrum at 915MHz is $6.9e-16 \text{ V}^2/\text{Hz}$. And the results are shown for post layout simulation. Table1 shows the optimised results of designed mixer. Figure4 shows the output of Cascode LNA for input RF frequency 915MHz. From figure 2 to figure 6 shows the various simulation results of designed Cascode LNA.

TABLE-2 OPTIMISED PARAMETER FOR DESIGNED LNA.

Parameters	Values
CMOS Tech.(nm)	65
Supply Voltage (V)	0.6
RF frequency (MHz)	915
Gain (dB)	15
Power Consumption (μW)	49
IIP3 (dBm)	-20
1dB Compression (dBm)	-29.1
Noise spectrum (V^2/Hz)	$6.9e-16$

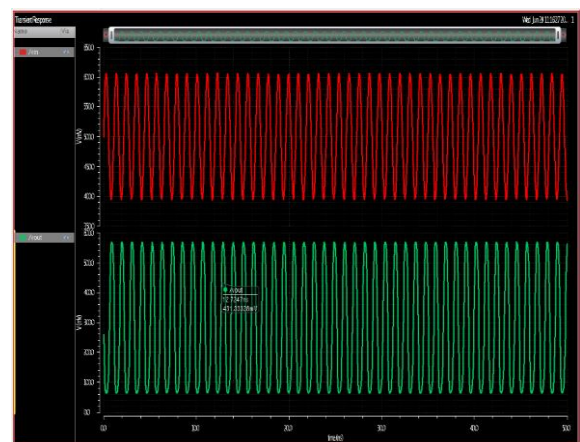


Figure 2: Input and output waveforms

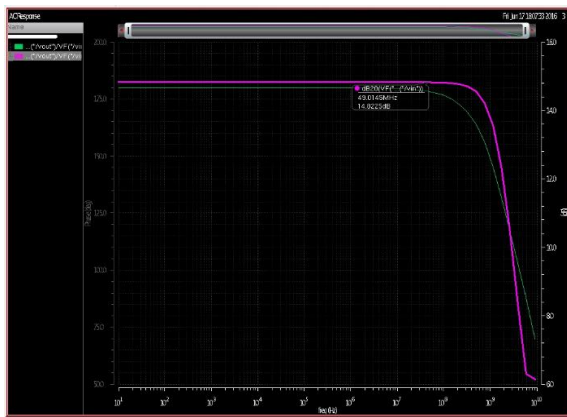


Figure 3: LNA Gain

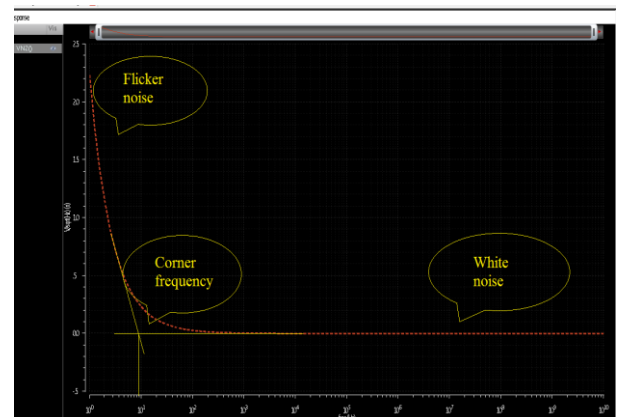


Figure 6: LNA Noise

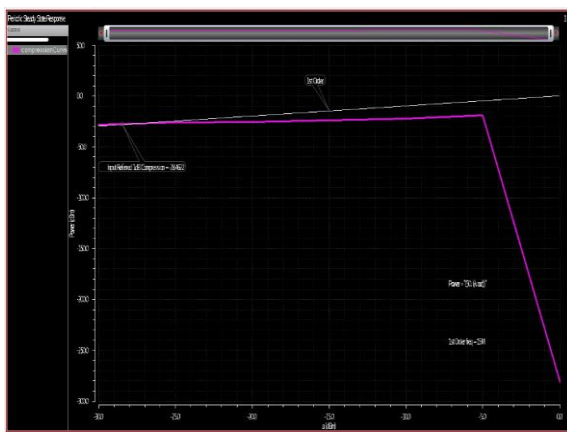


Figure-4: 1-dB compression point

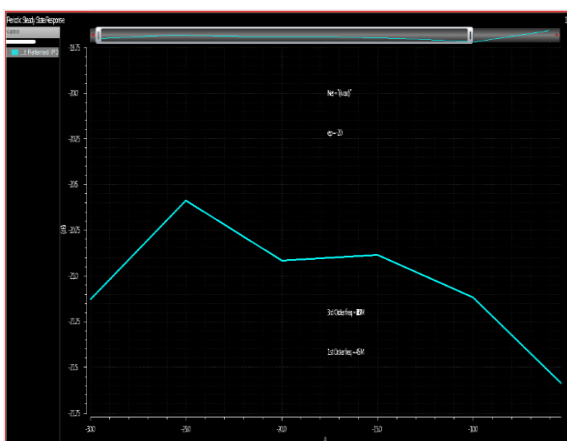


Figure 5: Input intercept point

5. CONCLUSION

In this paper, we proposed a low power low noise amplifier (LNA) dedicated to biomedical applications. Designed Cascode LNA is implemented in cadence virtuoso platform using 65nm technology with gain of 15dB. 1dB compression point (1-dB) of -28.47dBm, with a low power consumption of 49μW. It can be used for receiver with operating frequency of 915MHz for biomedical applications.

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BIOGRAPHY



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