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High Speed ALU Processor by Using Efficient Multiplication Technique

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Abstract - As the scale of integration keeps growing, more and more sophisticated and fast processing systems are being implemented on a VLSI chip. These fast processing system applications not only demand great computation capacity but also consume considerable amount of power. And the ALU are main functional unit in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. So the performance such VLSI circuit is dependent on the performance of the ALU. The performance of ALU is mainly depends on the performance of multiplier because the multiplier is generally the slowest and area consuming element in the system. Hence, optimizing the speed and area of the multiplier is a major design issue. Here, a High-speed multiplier is designed and analyzed which is based on the algorithm named as "Urdhva Tiryakbhyam" sutra (UT Technique). Traditionally, this well known Technique has been used for fast multiplication. The proposed algorithm is developed using VHDL. Implementation has been done using Xilinx14.2, Spartan 6.

***Key Words*: ALU, Multiplier, Adder, Logical Unit, Multiplexer, Vedic mathematics.**

1. INTRODUCTION

An arithmetic logic unit (ALU) is a Computation unit that performs various arithmetic (addition, subtraction, multiplication) and logical operations (AND, OR, INVERTER). And that's why the ALU is called heart of microprocessor, microcontroller and digital signal processor. The performance of Fast processing system is dependent on the speed of the ALU. The speed of ALU depends greatly on the multiplier. In algorithmic and structural levels, numerous multiplication techniques have been developed to enhance the efficiency of the multiplier which concentrates in reducing the partial products and the methods of their addition but the principle behind multiplication remains the same in all cases. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. Employing these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power etc. Though there are many sutras employed to handle different sets of numeric, exploring each one gives new results. Our work has proved the efficiency of Urdhva Tiryakbhyam– Vedic method for multiplication.

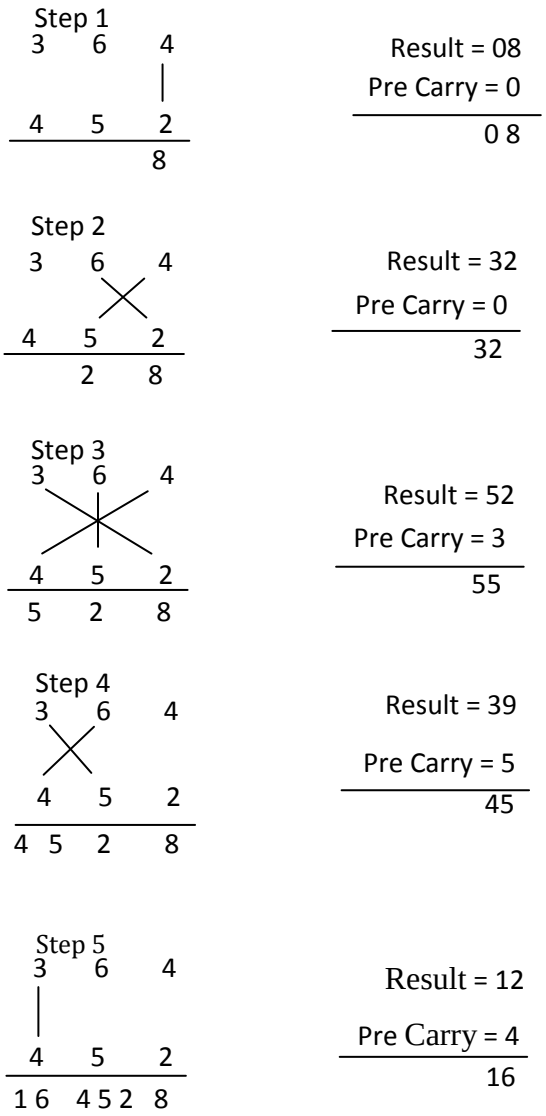
The organization of paper starts with a brief introduction that describes in the section I. Thereafter, Section II describes the Multiplication technique. Section III describes the Architecture of proposed multiplier. Section IV describes the design and implementation of ALU based on UT Technique module in XilinxISE14.2. Section V comprises of Result and Discussion in which computational path delay obtained. Finally Section VI comprises of Conclusion.

2. MULTIPLICATION TECHNIQUE

Urdhva Tiryakbhyam (UT) technique is sutra of Vedic mathematics used for multiply two given numbers in Decimal number system. However, we put forward the multiplication of two binary numbers using this technique. The literal meaning of UT is "Vertically and crosswise" and the multiplication happens in this fashion. UT is a novel concept through which introduces a parallel execution of partial products and sums which is explained in fig- 1. The word Vedic is derived from the word 'Veda' which means the store-house of all knowledge. Hundred years ago(in between 1911 and1918) Sanskrit scholars Jagadguru Swami Sri Bharati Krishna Tirthaji translated the Vedic documents and got surprised about the depth of knowledge enriched in that and became very popular to achieve high speed processing of the data. Vedic mathematics mainly based on 16 Sutras dealing with various branches of mathematics like arithmetic's, algebra, geometry etc. these sutras with their brief meaning are given bellow.

1) (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikina Purvena- By one more than the previous One.
4) Ekanyunena Purvena -By one less than the previous one.
5) Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
6) Gunitasamuchyah-The product of sum is equal to sum of the product.
7) Nikhilam Navatashcaramam Dashatah -All from 9 and last from 10.

8) Paraavartya Yojayet-Transpose and adjust.
9) Puranapuranabyham -By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam -By addition and by subtraction.
11) Shesanyankena Charamena- The remainders by the last digit.
12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yaavadunam- Whatever the extent of its deficiency



364 × 452 = 164528

Fig -1: Multiplication of two decimal numbers: 364 × 452

3. Proposed Multiplier Architecture

UT Technique based Multiplier is efficient hardware architecture for multiplying two integers, compared to a normal multiplier; it is mostly used for high speed multiplication. The block diagram of 4×4 bit Multiplier is shown in Fig -2. The 4×4 bit Vedic Multiplication unit is further realized by incorporating four similar modules of 2×2 multipliers. The processing in the form of block diagram is depicted in Figure 2. Demonstrating with an example of two digits consisting of 4 bit each named as A=A3A2A1A0 and B=B3B2B1B0 the output is obtained in 8 bits length say P7-P0 and last two output bit P_8, P_9 are Garbage Bits. Furthermore, the numbers A and B is divided in to two equal parts of two bits A[3:2], A[1:0] and B[3:2], B[1:0]. Now the 8 bit end product term is understood as:

$$P[1:0] = A[1:0] \times B[1:0]$$

$$P[9:2] = A \times B$$

$$P[9:2] = \{(A[1:0] \times B[1:0]) + (A[3:2] \times B[1:0])\} + \{(A[1:0] \times B[3:2]) + (A[3:2] \times B[3:2])\}$$

Multiplication of higher bits can be done in the similar manner. This multiplication technique is faster than any of the conventional multipliers. This technique uses less number of computational steps to get the result.

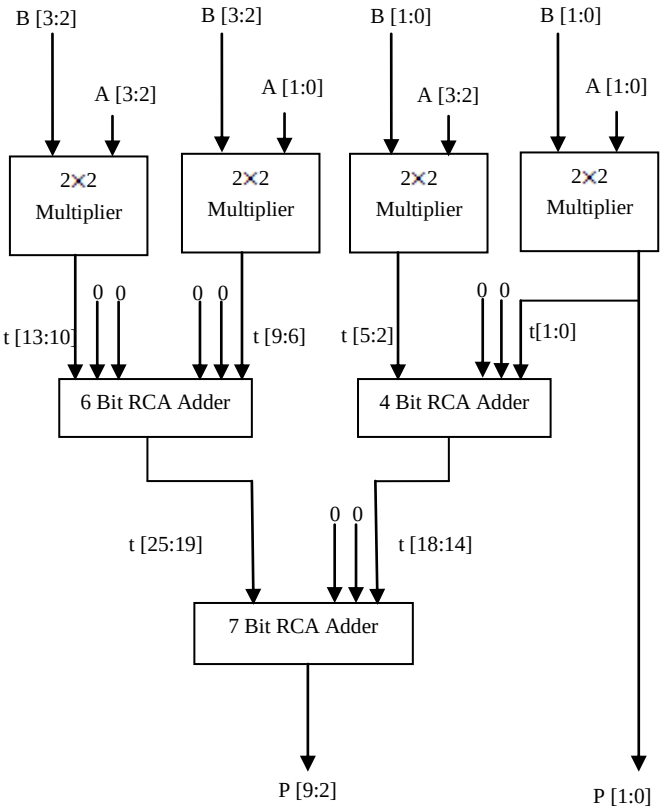


Fig -2: Block Diagram of Proposed 4×4 Multiplier

3. Proposed ALU Architecture

The ALU is a Computation unit that performs various arithmetic and logical operations. And that's why the ALU is called heart of microprocessor, microcontroller and digital signal processor. The performance of Fast processing system is dependent on the speed of the ALU. Every technology uses those operations either fully or partially which are performed by ALU. No technology can exist, without those operations which are performed by ALU. In this section, we will discuss about our proposed ALU architecture as shown in Fig -3. Two inputs are provided based on the selection line s0, s1, s2, s3 to perform arithmetic and logical operation as shown in Table1. Here 16:1 multiplexer are used for receiving the output of all the arithmetic operation and logical operation through this multiplexer the required output can be generated using selection line. Employing UT techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area etc.

TABLE 1.CONTROL WORD FOR ALU OPERATIONS

S. No.	Multiplexer Selection Lines and Operation					
	S0	S1	S2	S3	Y	Operation Selected
1.	0	0	0	0	t0	Addition
2.	0	0	0	1	t1	
3.	0	0	1	0	t2	
4.	0	0	1	1	t3	
5.	0	1	0	0	t4	
6.	0	1	0	1	t5	Multiplication
7.	0	1	1	0	t6	
8.	0	1	1	1	t7	
9.	1	0	0	0	t8	
10.	1	0	0	1	t9	
11.	1	0	1	0	t10	
12.	1	0	1	1	t11	
13.	1	1	0	0	t12	
14.	1	1	0	1	t13	AND
15.	1	1	1	0	t14	OR
16.	1	1	1	1	t15	NOT

4. Results and discussions

This paper describes the design and implementation of Multiplier and ALU based on UT Technique module in XilinxISE14.2 Spartan 6 series. This section also deals with quantitative and comparative result analysis of different approach of multiplier design and implementation is depicted in fig -4.

Proposed Vedic multiplier is compared with Array and Vedic Multiplier in terms of area and delay. Results obtained from these implementations are shown in Table 2. Area is nothing but the Number of Used slices in the design and delay is maximum combinational path delay obtained from the final report. Proposed Vedic multiplier shows better performance results than Array and Vedic Multiplier in terms of area as well as delay as shown in fig. 4. Proposed Vedic multiplier is faster compared to Array and Vedic Multiplier. By using of proposed Vedic multiplier construct an ALU Architecture that shows the computational benefits given by UT Technique. The Table.3 shows the device utilization summary and computational path delay of proposed ALU Architecture. Fig-5 shows RTL Schematic of Proposed ALU Architecture.

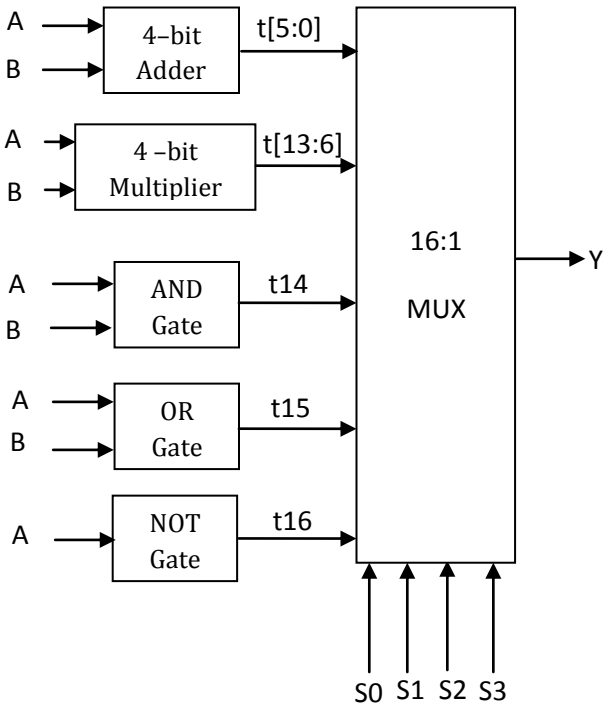


Fig -3: Proposed ALU Architecture

TABLE 2.DEVICE UTILIZATION SUMMARY OF 4-BIT MULTIPLIER.

4-bit Multiplier	Number of Used slices	Number of Bonded IOBs	Delay (ns)
Array Multiplier	40	20	20.117
Vedic Multiplier	18	16	17.473
Proposed Vedic Multiplier	20	18	9.332

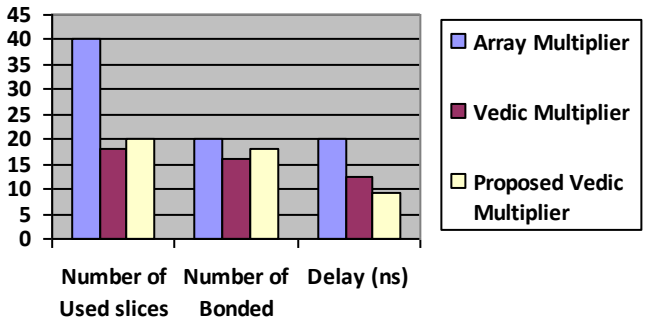


Fig -4: Delay and area Comparison graph of different multiplier.

TABLE 3.DEVICE UTILIZATION SUMMARY OF PROPOSED ALU

ALU	Number of Used slices	Number of Bonded IOBs	Delay (ns)
Array ALU	49	23	20.227
Vedic ALU	29	19	17.583
Proposed Vedic ALU	43	30	11.586

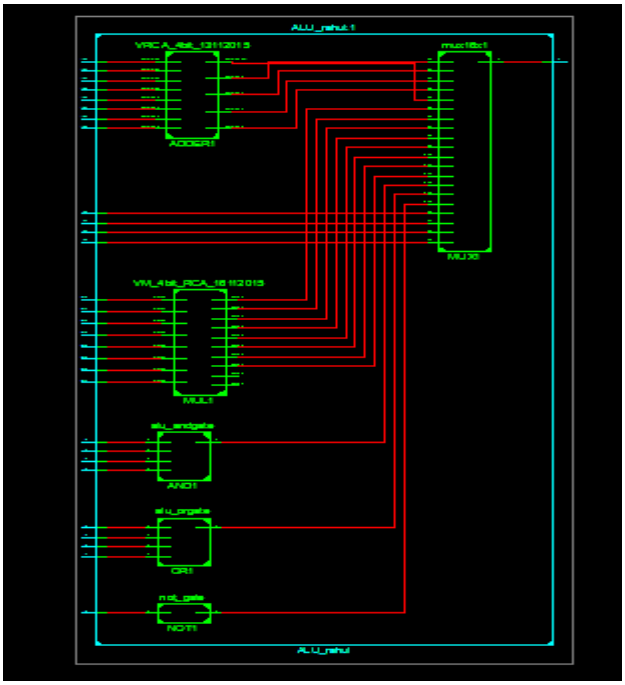


Fig -4: RTL Schematic of Proposed ALU Architecture.

5. CONCLUSIONS

In this paper we have proposed an extremely effective method of multiplication based on Urdhva- Tiryakbhyam algorithm. With this method we can construct multiplier and practically saw that Proposed Vedic Multiplier is much more efficient than Array and Vedic multiplier as shown in the Table2. By using of proposed multiplier construct an ALU Architecture that shows the computational benefits given by UT Technique. Since our objective was to reduce the computational path delay for proposed ALU is found to be 11.586ns, hence we achieved our objective.

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