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Implementation and Comparison of Power Gated CMOS Circuits

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Abstract - *As CMOS technology scales down, supply voltage is reduced to avoid device failure. This decreases the switching speed of transistors. To prevent this speed problem, threshold voltages of the transistors are reduced, due to which sub threshold leakage current increases exponentially. Power gating structure is one of the solutions to reduce leakage power. Design of a suitable power gating structure is an important and challenging task in sub-90nm VLSI circuits where leakage currents are significant. In designs where sleep mode to wake up mode and wakeup mode to sleep mode transitions are frequent, a significant amount of energy is consumed to turn on or off the power gating structure. It is thus desirable to develop a power gating solution that minimizes the energy consumed during mode transitions. This paper presents different power gating structures and their mode transition energies in 90nm technology. Various power gating techniques like STMTCMOS, NPMTCMOS, CRMTCMO, NPSCCMOS and CRCCMOS are implemented using Spice on 4 bit parallel carry look ahead adder CLA(74182) and 27-INPUT CHANNEL INTERRUPT CONTROLLER(C432). Mode transition energy, wake up time and ground bounce noise are calculated.*

Key Words: MTCMOS – Multi Threshold Complementary MOS, STMTCMOS – Standard MTCMOS, NPMTCMOS- Nmos and Pmos sleep MTCMOS, CRMTCMOS – Charge recycling MTCMOS, NPSCCMOS –Nmos and Pmos sleep transistors Super cutoff CMOS, CR SCCMOS –Charge Recyling SCCMOS.

1.INTRODUCTION

As CMOS technology scales down, supply voltage is reduced to avoid device failure due to high electric fields in the gate oxide and the conducting channel under the gate. This supply voltage scaling reduces the dynamic component of circuit power dissipation, but unfortunately also decreases the switching speed of transistors. To compensate for this performance loss, the transistor threshold voltages are decreased, which in turn causes an exponential increase in the sub-threshold leakage current. Furthermore, to maintain the gate voltage control over the active region of the transistor, thickness of the dielectric between the gate and the channel region is reduced, which in turn results in an exponential increase in the gate leakage current. Please refer to [1] for a more detailed discussion. Power gating, also known as Multi-threshold CMOS [2] or MTCMOS for short, is used to cut off the power to some functional blocks in a design. MTCMOS provides low leakage and high performance operation by utilizing high speed, low Vt (LVT) transistors for logic cell implementation and low leakage, high Vt (HVT) transistors for power gating switch implementation. The power gating switch itself is typically realized as a single (footer) NMOS or (header) PMOS transistor, which disconnects logic cells from ground or VDD rails to reduce the leakage when the circuit is in the sleep mode.

Some of the design challenges that must be considered when using the power gating technique are: (i) Placement and sizing of the sleep transistors; (ii) Automatic generation of sleep signal; (iii) Sleep signal scheduling for wakeup noise reduction; (iv) Mode transition energy minimization; (v) State retention; (vi) Support for multiple levels of sleep. In this paper, we focus on the mode-transition energy, Wake up time, power and ground bounce noise. The remainder of this paper is organized as follows. In Section II, we review prior work in the area of power gating. Section III compares the techniques and Sections IV and V present our simulation results and conclusions, respectively.

2. PRIOR WORK

MTCMOS is a leakage power saving solution that provides high active mode performance and low standby leakage power [3][4]. Sleep transistors slow down logic cells during the active mode operation of the circuit. This is due to the voltage drop across the functionally-redundant sleep transistors and the increase in the threshold voltage of logic cell transistors as a result of the body effect. The performance penalty of using a sleep transistor depends on its size and the amount of the current that flows through this transistor due to logic transitions in the active mode. A number of researchers have proposed methods for optimal sizing of sleep transistors in a given circuit to meet a performance constraint [5]-[9]. A large amount of current can flow during the sleep to active mode transition in an MTCMOS circuit. High peak rush current in the circuit can cause Electro-Migration (EM) problems in the power/ground rails. This rush current can also result in supply/ground bounces due to the *Ldi/dt* effect. In [10] the authors propose a wakeup strategy and a partitioning technique to limit the rush-through current. The authors of [11] tackle the problem of minimizing the wakeup time while limiting the current that flows to ground during the sleep to active mode transition. Their approach consists of

first obtaining the discharge patterns of all logic cells and then
Grouping the circuit into a minimum number of clusters in such a way that the total discharge current of each cluster is below a given threshold. In [12] the authors introduce two power mode transition strategies to reduce the ground bounce while turning on the circuit. The first strategy uses single sleep transistor and gradually turns it on, while the second technique employs parallel-connected sleep transistors with increasing widths and turns them on one after the other starting from the transistor with the smallest width. Due to the large amount of mode-transition energy overhead and large wakeup latency for the circuits, sometimes, for short standby periods, it is better to put the circuit in a drowsy mode instead of the sleep mode. The reason is that the wakeup latency of the drowsy circuit is much less than that of the circuit in sleep mode. The work in [13] presents multiple power modes for the circuit, but it needs multiple supply voltages (stable reference voltages to drive the gate terminal of the sleep transistor which will be operating in different points of the sub threshold conduction region during the sleep mode). In [14], the a authors propose a power gating structure to support an intermediate (drowsy) power-saving mode and the traditional power cut-off mode. The idea is to add a PMOS transistor in parallel with each NMOS sleep transistor. By applying zero voltage to the gate of the PMOS transistor, the circuit can be put in an intermediate power saving mode whereby leakage reduction and data retention are both realized. Furthermore, by transitioning through this intermediate mode while changing between sleep and active modes, the magnitude of the voltage fluctuation of the power supply or ground during power-mode transitions is reduced. In the cut-off mode, the gate of the PMOS transistor is connected to VDD. A charge-recycling technique is present in [15] to minimize the power consumption during the mode transition in a power gating structure while maintaining the wake up time.

3. POWER GATING TECHNIQUES

Circuit blocks that are not in use are temporarily turned off by transistor switch in Power Gating. Low leakage (10x to 50x), high performance and huge power benefit can be achieved using power gating. But it affects design architecture, Increase time delays as power gated modes have to be safely entered and excited. Some of the power gating techniques are ST-MTCMOS, NP-MTCMOS, CR-MTCMOS, NP SCCMOS and CR-SCCMOS.

3.1 STMTCMOS :

Utilizes low Vt High speed transistor for logic cell implementation and low leakage, high Vt transistor (footer) for power gating switch implementation as shown in Fig1. It gives Low leakage and high performance operation. Time required for recovering from the idle mode (wake up time) is long relative to circuit clock rates. Hard to turn on completely at very low supply voltages.

3.2 NPMTCMOS:

Utilizes one NMOS and one PMOS sleep transistors. Circuit is partitioned into two blocks, where one uses an NMOS sleep transistor, while other uses a PMOS one as shown in Fig3. In the active mode, sleep transistors SN and SP are in the linear region and the voltage values of the virtual ground and virtual VDD are equal to 0 and VDD, respectively. In the sleep mode, sleep transistors SN and SP are turned off; since they are high threshold voltage devices, very little sub threshold leakage current flows through them. Circuit takes long time to settle down to power rails. Hence, for short sleep mode operations this technique will not reach to 0 and Vdd power rails. More mode transition energy required.

3.3 CRMTCMOS:

To reduce the energy as circuit switch between active and sleep modes of the circuit charge recycling technique is used[15]. To reduce the switching power consumption during the active-to-sleep and sleep-to-active transitions by adding a *charge sharing switch* between the VGND and VVDD nodes as shown in Fig. 5. The proposed charge-recycling strategy works as follows. We turn on the charge sharing switch (i) immediately before turning on the sleep transistors while going from the sleep to the active mode, and (ii) just after turning off the sleep transistors while going from the active to the sleep mode. By turning on the switch at the end of the sleep mode as the circuit is about to go from sleep to active mode, we allow charge sharing between the completely charged up capacitance CG and the completely discharged capacitance CP. After the charge recycling is completed, the common voltage of the virtual ground and virtual supply is αVDD, where α is a positive real number less than 1. The value of α depends on the relative sizes of CG and CP. As a result of this, the mode transition energy is reduced.

3.4 NP-SCCMOS:

Turning on HVT devices is difficult in sub 1-V CMOS technologies [16].Super Cut-off CMOS (SCCMOS) circuits solve this problem by using a low threshold voltage (LVT) device for cutting off ground or VDD [16]. Instead of using HVT devices for leakage reduction, SCCMOS circuits overdrive the LVT PMOS sleep transistors by applying a positive overdrive voltage of ΔVDD in excess of VDD to their gate terminals. Similarly, they under drive the LVT NMOS sleep transistors by applying a negative voltage of –ΔVDD to their gate terminals. It has been shown the SCCMOS circuits achieve the same leakage reduction as the corresponding MTCMOS circuits with shorter wakeup times due to the use of LVT transistors. This Circuit suffers from wasteful mode transition energy consumption.

3.5 CR-SCCMOS:

Charge recycling may be applied to SCCMOS circuits to save the mode transition energy in the same fashion as it is applied to MTCMOS circuits.

4. SIMULATION RESULTS

All the circuits are simulated using Spice with 90nm technology. Fig 1 shows Carry Look Ahead adder with sleep transistor as footer transistor. The CLA has A,B,C as inputs and cnx,cny,cnz, pbo(propagate output) and gbo (generate output) outputs.

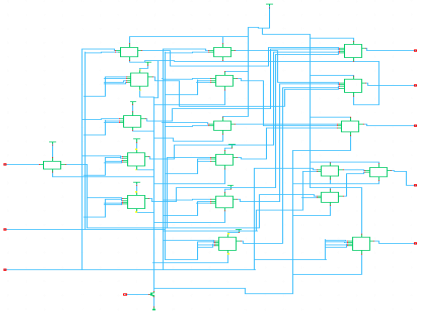

Fig1: ST MTCMOS (footer sleep transistor)

Fig2 gives the simulated outputs of Fig1. From the waveforms it is observed that the pbo(yellow) and gbo (blue) outputs are suffering from mode transition

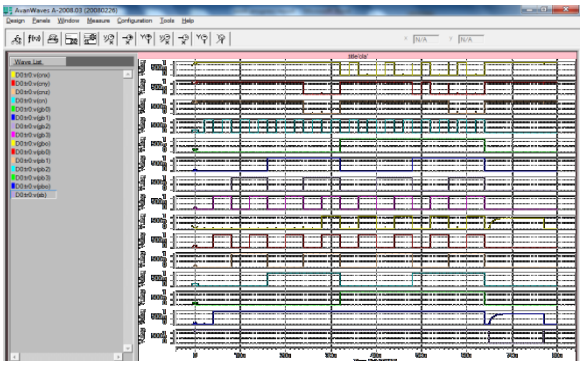

Fig 2: ST MTCMOS simulation waveforms

Fig 3 shows the NMOS and PMOS switches to CLA. From Fig4 simulated results cnx(first yellow) and gbo (last pink) are suffering from mode transition and delay.

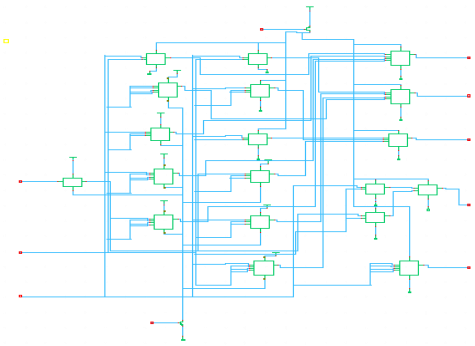

Fig 3: NP-MTCMOS

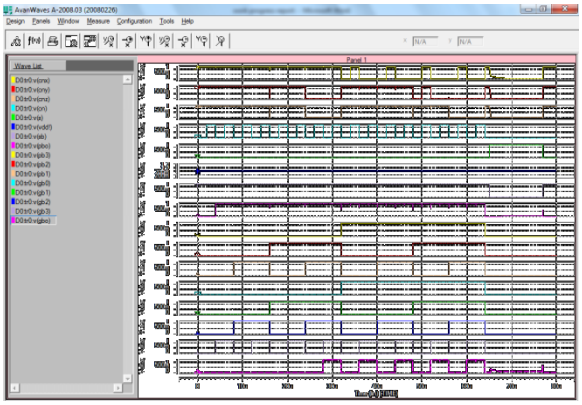

Fig4: NP-MTCMOS simulation waveforms

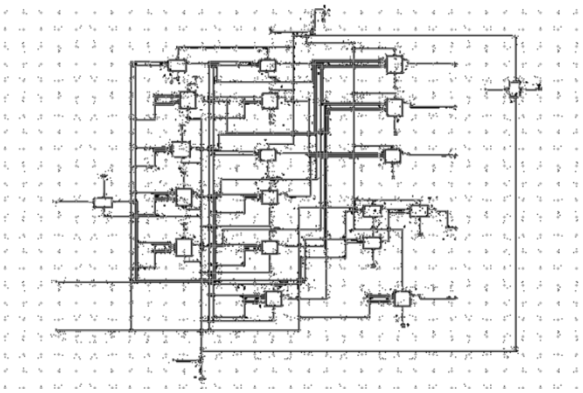

Fig 5: CR-MTCMOS with transmission gate as switch

Fig 5 shows a Transmission gate as charge recycling switch between two blocks and the simulated results of fig6 shows that the delay is reduced.

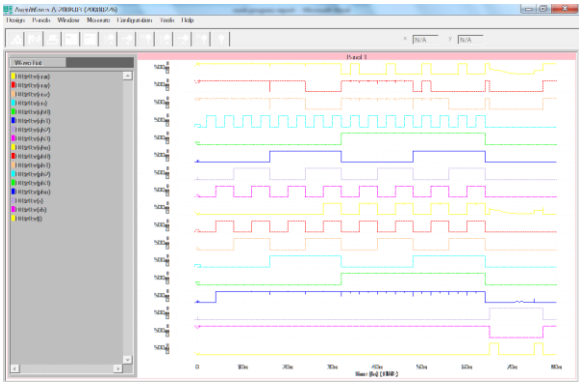

Fig 6: CRMTCMOS simulated waveforms

With the use of SCCMOS circuits delays are reduced and switching speed increases. From Fig7 and Fig8 it is concluded that output switches immediately once there is a mode transition occur.

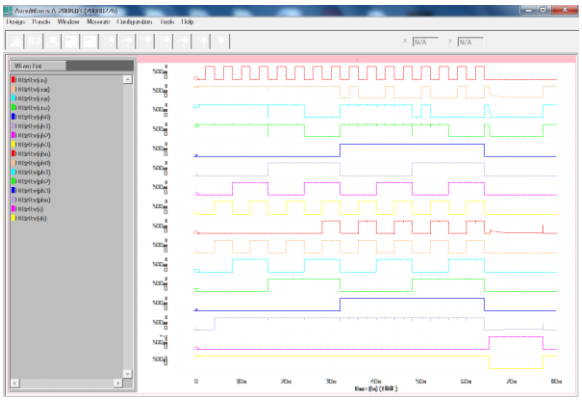

Fig 7: NP-SCCMOS simulated waveforms

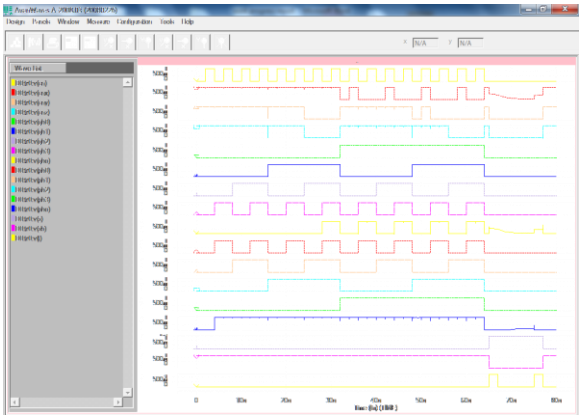

Fig 8: CR-SCCMOS simulated waveforms

From the table 1 it is concluded that mode transition energy is less for charge recycling circuits. From Table 2, it is shown that wakeup time for charge recycled circuits is less when compared to the St and NP circuits. From table 3 it is concluded that we can reduce the peak voltage and the settling time of the ground bounce occurred while waking up the circuit.

Table1: Mode transition energy comparison in Femto Jouls

circuit	ST Mtcmos	NP Mtcmos	CR Mtcmos	NP Sccmos	CR Sccmos
CLA (74182)	23.218/ 15.54	27.8/ 19.524	14.5/ 11.98	27.81/ 19.362	14.61/ 12.1
(C432)	111.50	129.34	65.078	129.11	65.886

Table2: Wake up time comparison for CLA

NPSCCMOS	NPMTCMOS
wakeup_time_cnx= -5.2695E-09 wakeup_time_cny= -4.1659E-09 wakeup_time_cnz= -3.2855E-09	wakeup_time_cnx= 5.9901E-09 wakeup_time_cny= 6.0245E-09 wakeup_time_cnz= 6.0878E-09
CRSCCMOS	CRMTCMOS
wakeup_time_cnx= -7.9411E-09 wakeup_time_cny= -5.9773E-09 wakeup_time_cnz= -4.5635E-09	wakeup_time_cnx= 4.9382E-08 wakeup_time_cny= 4.9464E-08 wakeup_time_cnz= 4.9554E-08

Table3: Ground bounces noise comparison

Circuit	POSITIVE PEAK			NEGATIVE PEAK		
	NP-Mtcmos	CR Mtcmos	%reduction in CR	NP Mtcmos	CR Mtcmos	%reduction in CR
CLA	86.8uv	5.3uv	93.8	-51.5uv	-6.3uv	87.76
C432	54uv	19uv	64.8	-1062uv	-47uv	95.5

5. CONCLUSIONS

In this paper we calculated the mode transition energy, wake up time and ground bounce noise for 4 bit carry look ahead adder and 27 channels interrupt controller. We concluded from the results that by applying charge recycling to MTCMOS or SCCMOS circuits, we can save the energy wasted during mode transition while maintaining the wake up time of the original MTCMOS or SCCMOS circuit. We also showed that by using the charge recycling, we can reduce the peak voltage and the settling time of the ground bounce occurred while waking up the circuit.

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