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DESIGN AND IMPLEMENTATION OF MEMORY CONTROLLER FOR REAL TIME VIDEO DISPLAY USING DDR3 SDRAM

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Abstract - *The rapid development in designing of memory controller in the field of VLSI motivated the design engineer to integrate the complex systems of several million transistors in a single chip. The designing of DDR3 SDRAM by using FPGA technology plays the most important role on the integrated circuit area in order to minimize the time to market and cost. The enhancement/improvement in the designing of memory controller has lead to achieve good support for memory, device and I/O. This project includes reading the data stored on the FPGA in organized manner and then sending it to the VGA/TFT driver and then to the VGA screen for the display of the video data. The results can be are verified by real time display of the stored data and by using simulation tool and chip-scope. This project explains the designing of the memory controllers for the DDR3 SDRAM devices using with IP and reconfigured memory controller. The DDR3 SDRAM is a twofold information rate. The main advantage of DDR3 is the capacity of I/O information exchange increases by eight times of the information rate of the memory cells. This DDR3 gives higher rates than earlier memory transfer rates. This project givers a genuine explanation for the designing of DDR3 SDRAM controller using Xilinx Design Suit 14.7 and Implemented on FPGA using Virtex-6 board.*

Key Words: Virtex-6 FPGA board, DDR3 SDRAM, Web Camera module, Monitor display.

1.INTRODUCTION

In recent years, there has been enormous progress in the area of integrated circuit design. The progress in the processing technology required memory devices operating at a high speed. The evolving memory devices developed with improvement in the latency, speed etc. The radical memory device developed was SDRAM referred as synchronous DRAM, it is synchronized with respect to the positive edge of the clock. The further advance involves precision in designing a system. This involves designing a memory controller. The controller mainly aims the interaction of memory and processor with a goal of well refined memory designs.

Types of memory

DDR1 SDRAM:Double data rate originally referred to as simple DDR and it was designed to replace SDRAM. The data transition occurs at the both falling edges and rising edges of digital Pulse. DDR transfers the data twice to the SDRAM.

DDR2 SDRAM: After DDR1, DDR2 is next generation of memory device. The DDR2 SDRAM operates twice to that of the DDR SDRAM.

DDR3 SDRAM: DDR3 is next generation of memory introduced after DDR2. DDR3 operates twice in speed to DDR2 SDRAM with a Pre-fetch buffer having size of 8-bits, also with increased frequency of operation which results in higher data transfer rate than DDR2. DDR3 has memory reset option which other types of memory do not reset allows memory to be cleared by software reset action which results in a more stable memory system. FPGA design is widely used and this technology plays very important role in order to minimize the time to market and cost. Design of the memory controller is advantageous for efficient use of the memory. The graphic display for video used is VGA. It is a video display standard that gives straight forward technique to interface any framework with a screen for display of data or pictures. VGA is widely utilized as standard display unit. Video graphic display is more advantageous while presentation than the verbal voice.

II. IMPLIMANTATION

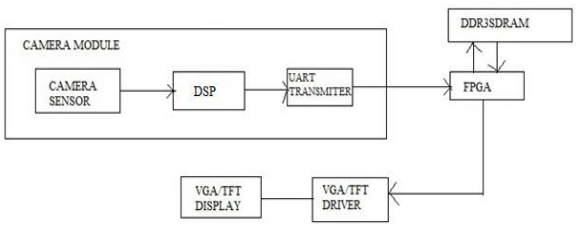

Figure 1: Main Block diagram

Camera module captures images and the images are then sent to the DSP in the camera vc0706. The image is then transmitted over UART communication protocol to the FPGA and then it is written (stored) on chip memory of FPGA. The block shown in fig 1 involves reading the data stored on the FPGA in organized manner and then sent to the VGA/TFT driver and then to the VGA screen for the display of the video data.

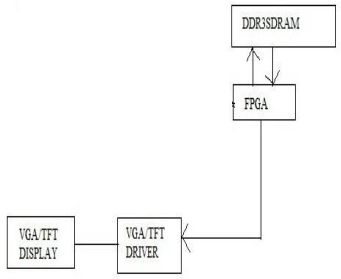

Figure 2: Real time video display using ddr3 sdram memory controller

The block shown in fig 2 involves reading the data stored on the FPGA in organized manner and then sending it to the VGA/TFT driver and then to the VGA screen for the display of the video data.

FPGA

Generally in the FPGA design the most part is determined utilizing a hardware description language (HDL), like that utilized for an ASIC. FPGA advanced ICs contain logic blocks with configurable squares. It contains programmable segments known as logic elements.

FPGA presents reconfigurable nature, which is advantageous in reducing the inventory cost of the design. This is the reason that FPGA are extensively used as the prototype development standard.

VGA CONTOLLER

VGA is a video display, technique that interface framework with screen to indicate data and pictures. VGA analog interface is used as high definition video with higher resolution .It is referred as an array rather than adapter because it can be easily available as single chip VGA. It can be directly implemented on PC mother boards with less complexity as it requires timing crystals, external RAM DAC and video memory.

VGA Principle

- It is a video interface standard and contains 640 Horizontal by 480 vertical of picture components namely pixel.
- The pixels are continuously tuned on and off to represent image.
- After the values are updated in horizontal row the pointer increments to the new column and repeat the same procedure.
- Screen must be refreshed for every 60seconds.

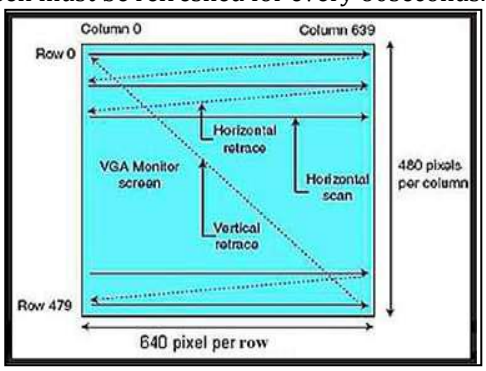

Figure 3: Scanning pattern of VGA Controller

General Architecture of Virtex-6 FPGA

The given figure 4 shows memory interface using Vertex-6 FPGA MIS center. The architecture contains core modules and interface with IP.

User Design

The client outline block shown in Figure 4 is FPGA plan associated with DDR3 SDRAM. Client outline interfaces with memory controller through the client interface. A case client outline is provided with the core.

- User Interface/ Interface block

The UI block exhibits UI to the client plan block. It gives a basic contrasting option to local interface by displaying level location space with buffering read operation and write operation.

- Native Interface and Memory Controller (MC)

Front end of MC shows the local interface to UI square. The local interface allows client outline to provide write information and read information as well as allows some components to move data from outside memory to client outline or vice-versa. The back end is associated physical interface. MC throughput as well as latency can be improved by reordering.

IP design of DDR3 memory controller

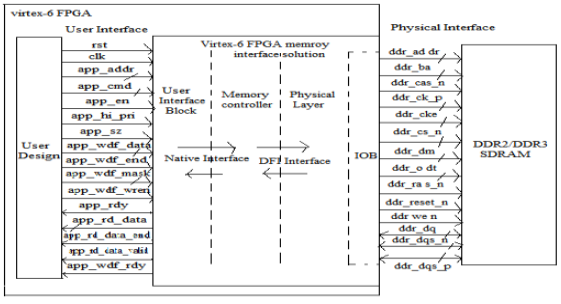

Figure 4: The complete memory interface from the user design to the DDR3 SDRAM

In the design of the DDR3 SDRAM controller readily available IP the signals are initialized and applied according to the MIG design and perform the operation at the user design end, for either it is read or write. For write operation the addrs/cmd performs the address translation and Wr_Data/DM is the given to write data buffer and then these signals are applied to reordering controller following the physical layer. The detail flow of signal after the user interface block represented by given to the native interface and the data is flowed finally to the physical interface and then to the external DDR3 SDRAM from the FPGA. Every stage involves representation of the signals. Reconfigured memory controllers: The memory controller is designed by using the corresponding signals given below in the diagram and every signal has an event associated with it.

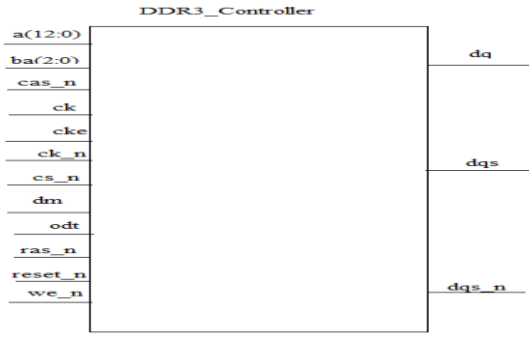

Figure 5: Internal block diagram of the Memory controller design.

The signal ddr_ad_dr is of width 13 bits with width [12:0]. The other signal detail is given in the table every position indicates some feature as described by MR0 of the DDR3 SDRAM. The signal dq provides the data either read or written depending on operation. The dqs indicated the data strobe is bi-directional pin when the system is performing the write operation the controller issues the dqs command and vice versa in read command.

FSM for DDR3 SDRAM controller

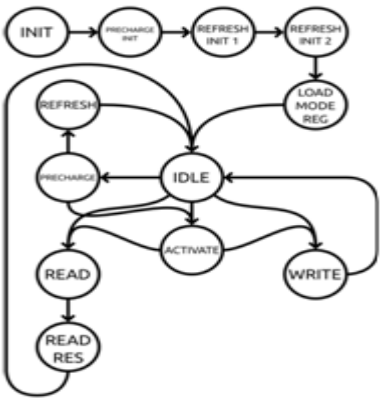

Figure 6: FSM for DDR3 SDRAM memory

IV. RESULTS

RESULTS AND OBSERVATIONS

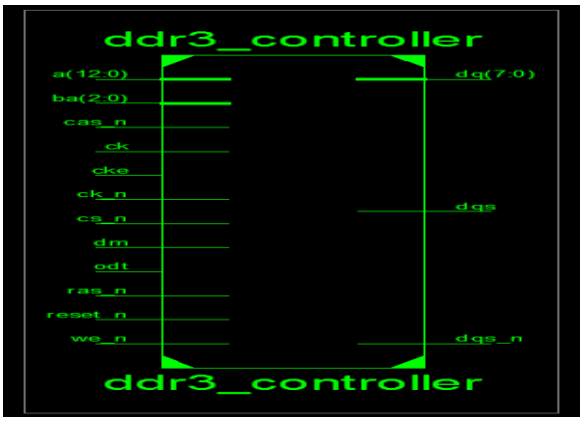

Figure 7: RTL schematic of reconfigurable device

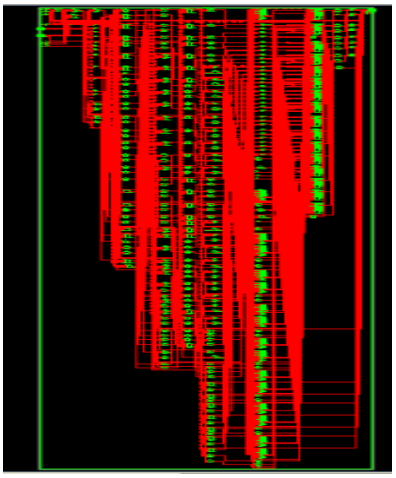

Figure 8: Tec schematic of reconfigurable device

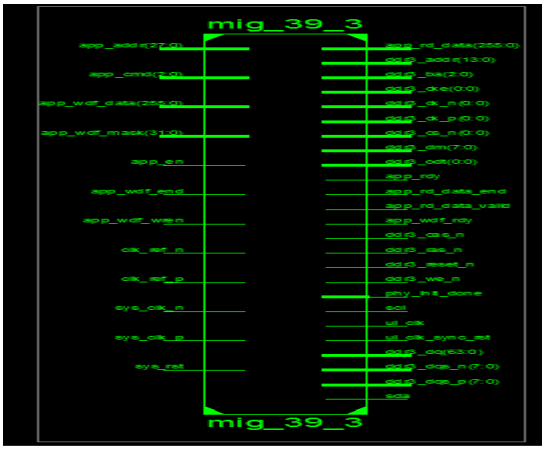

Figure 8: detail RTL schematic with IP

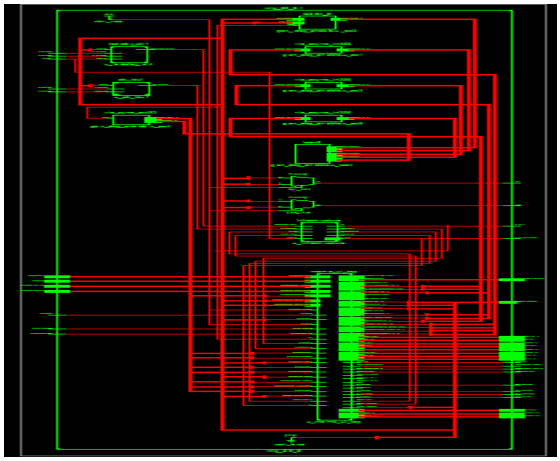

Figure 9: TEC schematic of with IP

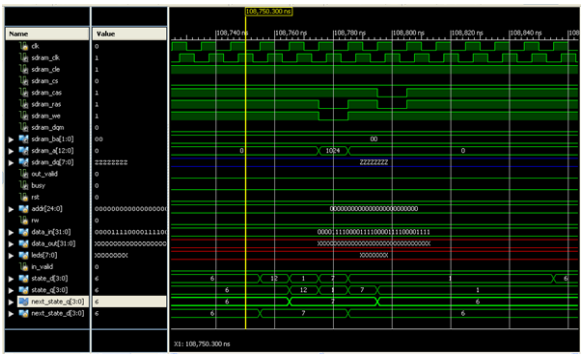

Figure 10: Simulation result of read signal

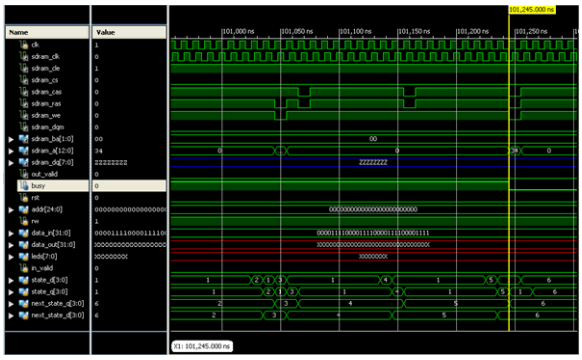

Figure 11: Simulation result of Write signal

V. CONCLUSION

The design developed for the real time video display and memory controller designed serves to provide efficient use of the memory. The project is employed using Xilinx 14.6. The controller is designed for the available IP and reconfigured controller. The controller displays the data and it is an attractive approach for various applications involving a display. The display used is VGA. The project is implemented on ML605 evaluation board with on chip DDR3 SDRAM of 1GB.The designed system involves a display of data at same time at different locations. The designed system can explore the in-built various features such as error detection and correction and AXI interface etc. The design can be implemented on advanced virtex series to increase the speed of operation. It can be used in various applications.

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