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# Design of Dynamically Tunable Band-Pass Filter for Software Defined Radio (SDR) and Cognitive Radio (CR) Applications

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**Abstract -** *For the radio communication, filter is one of the important module. In the defence the SDR radios used where in which the data rate and the bandwidth are manually selected. In this project an alternative technique is defined to identify the data rate of the received signal dynamically. The proposed method is implemented on the Vertex6 xc6vlx130t device. The digital filters are having wide applications in communication section. Software filters are designed and implemented.*

***Key Words***: Dynamically tunable band-pass filter, digital filters.

## 1. INTRODUCTION

A tunable filter is one in which the filter will automatically tune to the incoming signals and provides the required information which is useful for the further process in the communication system. Filter is one of the main module in both SDR and CR as it is required to get the original transmitted signal. Filters can be both hardware and software. But the designing of hardware filters using RLC components for all the data rates will be cumbersome, space consuming and costlier effort, because we have to design hardware PCBs for this. Hence we are using software filters in this project.

Tunable filters are used in the radio communication, which are having its wide applications in military defense. SDR is a radio where the components that are realized in hardware in earlier radios are now designed using the software. In SDR some of the physical layer operations are done by software means. The other definition is that the CR is an intelligent radio that accesses the available spectrum in its surrounding area and selects the most excellent spectrum for its transceiver [7].

In the SDR and CR, the receiver part of the system must be flexible enough to detect the incoming signal bandwidth so that the filter in the receiver part will tune itself to the required filter type. As the transmitter of the SDR will send the data at different data rates and in large RF band so the receiver must have the capability to detect in which bandwidth or frequency band the signal is coming for the filter in the receiver side and the filter should be dynamically tunable one. Digital filters have the advantage of re-programmability hence provides more stability [1]. Digital filters have their applications in acoustic processing, signal frequency analysis etc.

## 2. PROPOSED WORK

The design of dynamically tunable filter for software defined radio and the cognitive radio is done in 2 ways. At present separate filters are designed and implemented for different signals coming in different data rates and here the filters are selected manually using the front panel of the radio. Also in the earlier system the information regarding the data rates used to transmit the information is shared between the transmitter and the receiver. Here we propose 2 different advance methods to filter the signals by finding the data rates in which the signal is coming prior to filtering the signal.

1. By using the predefined training sequence
2. Using LPA (Local Polynomial Approximation)-ICI (Intersection of Confidence Intervals) algorithm.

In the first method some predefined training sequence is used to determine the data rates. Here a different 8bit sequence is defined for different data rates. At the transmitter side before sending the data the transmitter sends this training sequence to indicate the receiver that at which data rate the information it is sending. At the receiver after verifying this training sequence the receiver decides the data rate at which the information is received after that it is passed through the respective filter to filter the signal in order to obtain required information. The flow chart that defines the method 1 design is shown in Figure 1.

Store the received training sequence in the buffer. Here we consider that the training sequence should send three times by the transmitter and each of the received sequence is compared with the any of the predefined sequence at the receiver. If the training sequence matches with the first sequence, then depending on that sequence respective filter is selected. In the flow chart shown in Figure

3.1 we define two variables i and n and initialized these variables to 1 and 0 respectively. For the count of i less than or equal to 3 the received sequence is compared with the stored predefined sequence at the receiver for 3 times within the loop. For every match in the sequence the n value is incremented once. After that when i value exceed 3 the instruction will come out of the loop and checks for the condition of n value. If n value is equal to 2 or 3 then corresponding filter is selected to filter the signal else again the process is repeated to compare the received training sequence with another sequence.

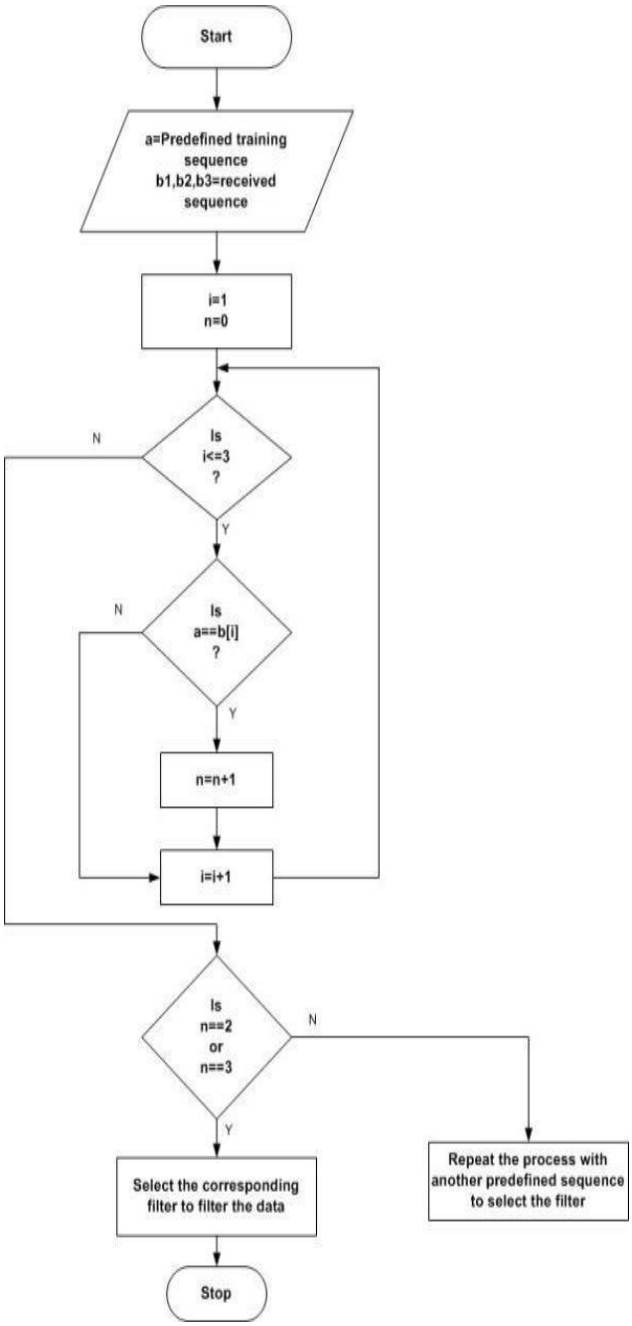


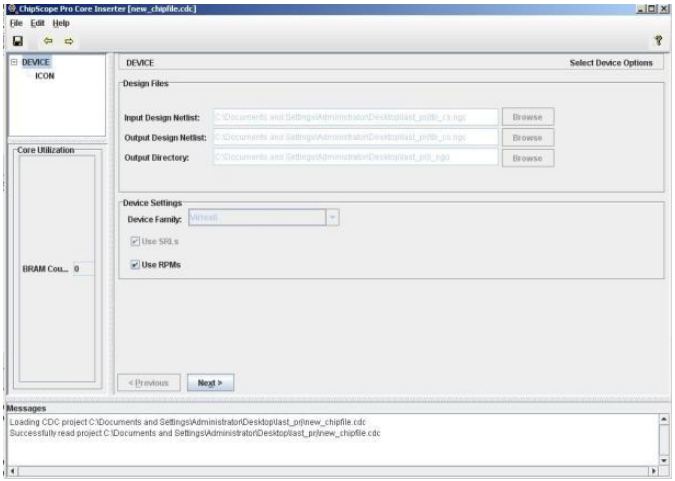

Figure 1: Flow chart

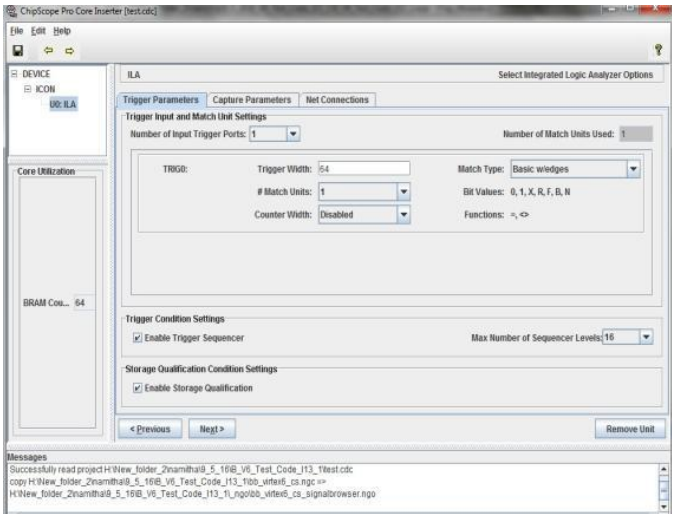
## 3. HARDWARE IMPLEMENTATION

The logic designed is implemented on the Vertex 6 XC6VLX130T device. Its performance is checked using the chip scope. The hardware implementation procedure is explained step by step as follows:

Step 1: The black card is connected to the PC using JTAG. The black card is one which used in the radio it consist of modulation/demodulation, ADC, DAC, RF up converters. This part of functions is done in the black card.

Step 2: After the code is ready the ucf file and cdc file is attached to the project. The ucf file consists of the pin matching description of the board and the cdc file is used for the chip scope settings. The Figure 2 shows the opened dialog box of the chip scope pro analyzer which shows the device name used in the project. Also the figure 2 shows the trigger and capture parameter settings along with the net connection settings.



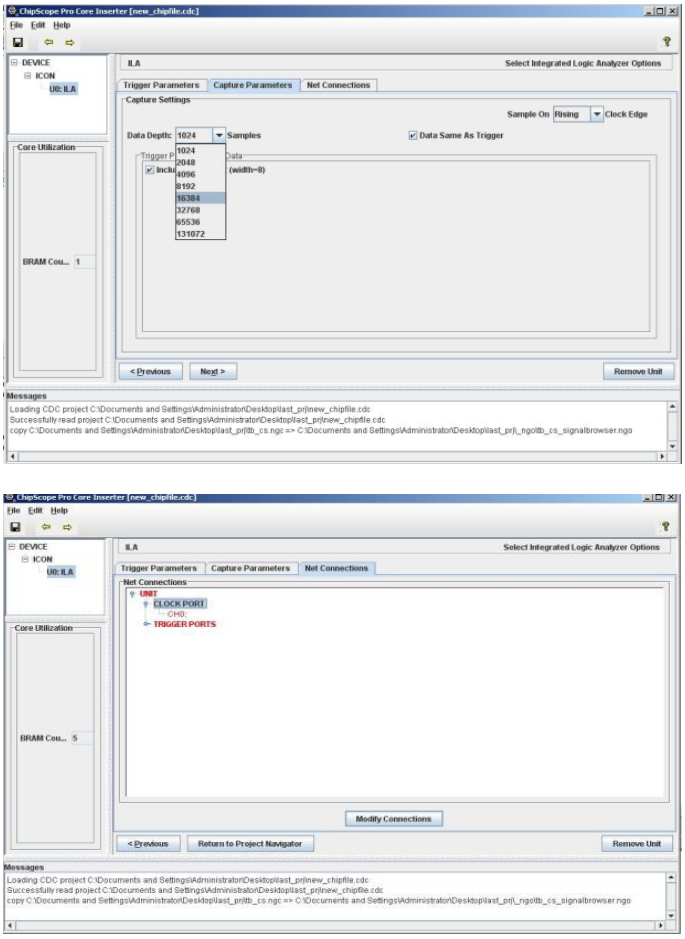



Figure 2: Chip scope parameter settings

Step 3: After the chip scope settings are done the bit file is generated. The program is dumped into the device Vertex 6 using IMPACT tool of the Xilinx software.

Step 4: Analyze the design using the chip scope. The cdc file is imported and the outputs are observed.

The Figure 3 shows the black card used.

Figure 3: Black card image

## 4. SIMULATION AND IMPLEMENTATION RESULTS

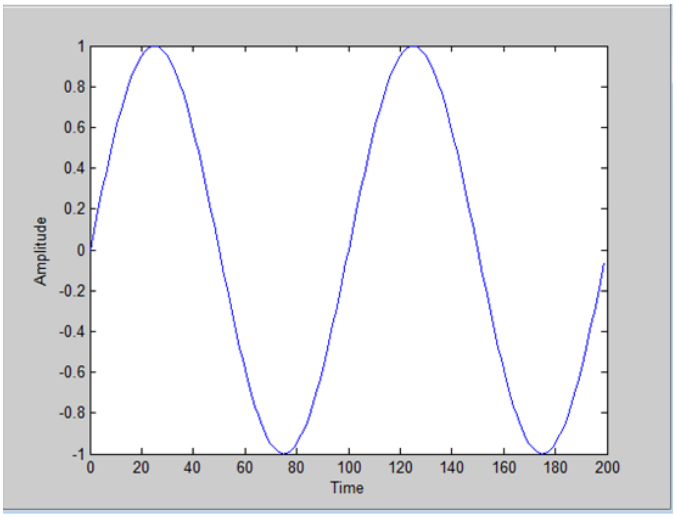



Figure 4: Generated 10MHz signal.

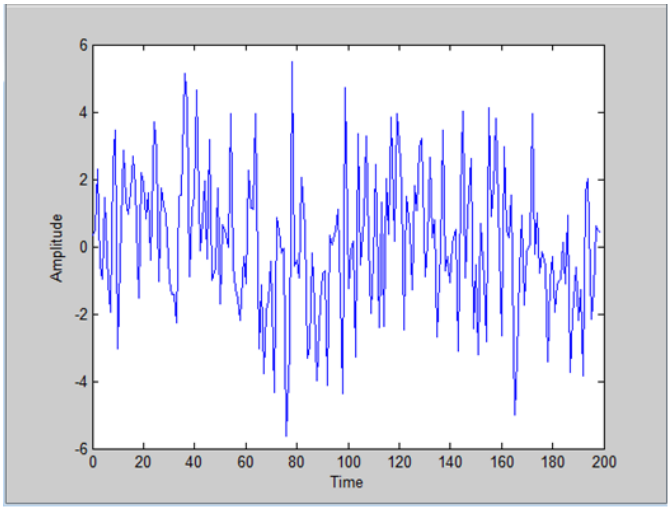



Figure 5: Signal with noise time domain.

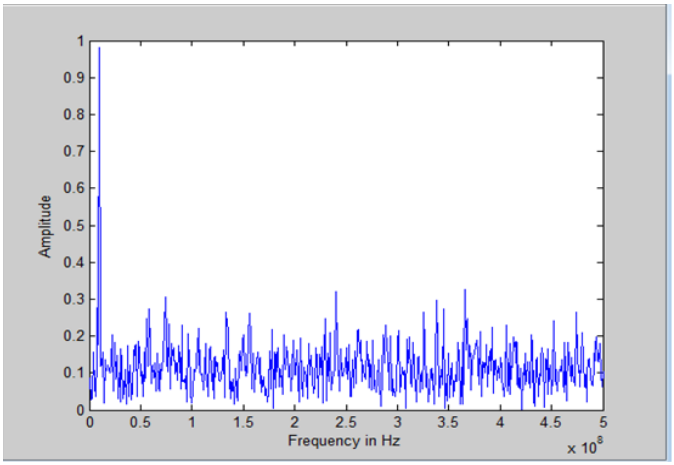



Figure 6: Signal with noise frequency domain plot.

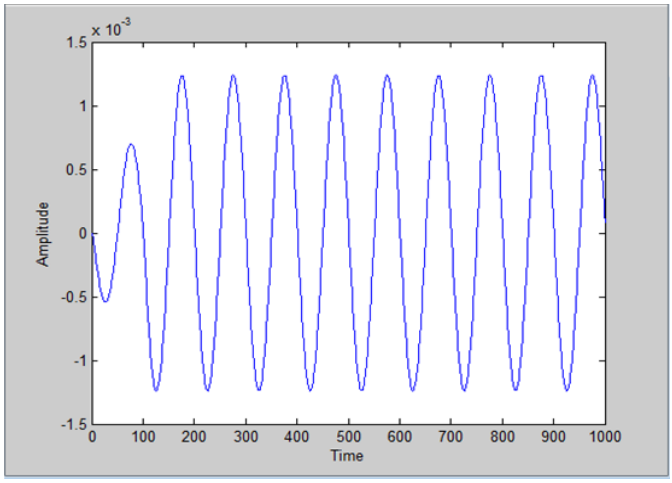



Figure 7: Time domain plot of filter output.

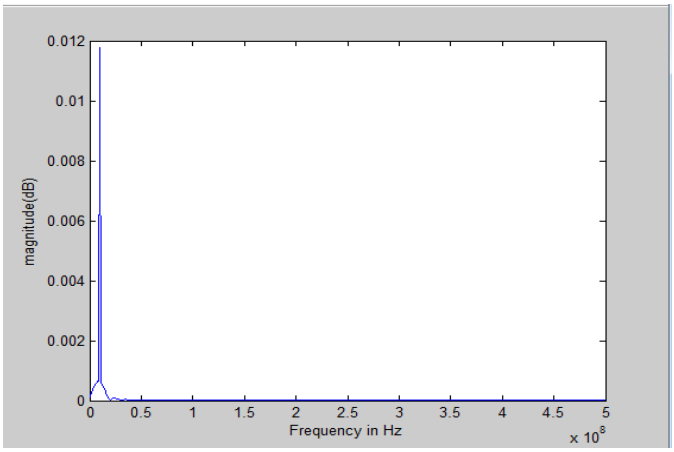



Figure 8: Frequency domain filter output plot.

The figures from 4 to 8 show the time domain as well as frequency domain plots. The signal of 10MHz is generated as it was passed through the channel where noise is added. At the receiver after computing the logic of method 1 the respective filter is selected and the filter output after scaling the received signal in both time and frequency domain is plotted.

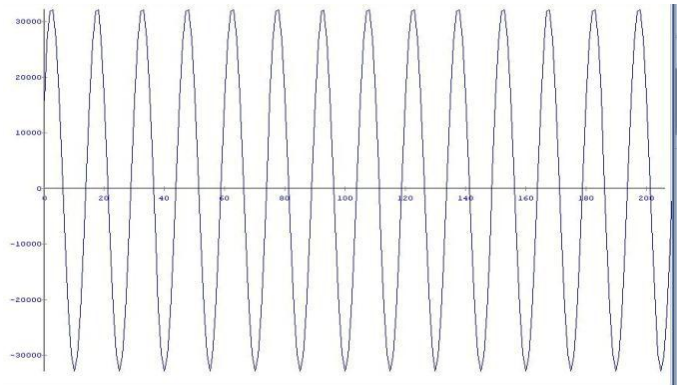


Figure 9: Data vs time generated signal bus plot.

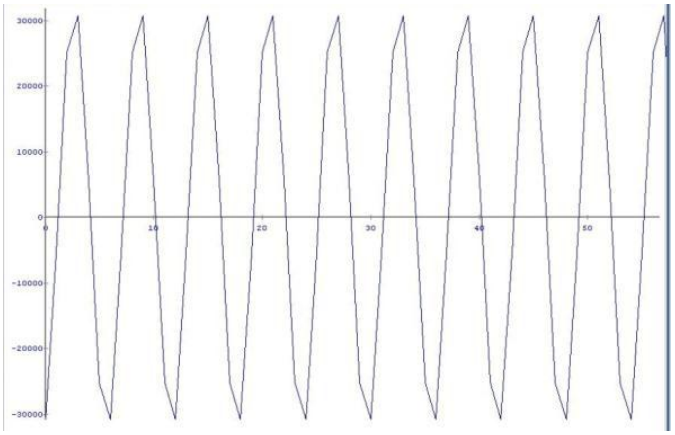


Figure 10: Data vs time ADC output bus plot.

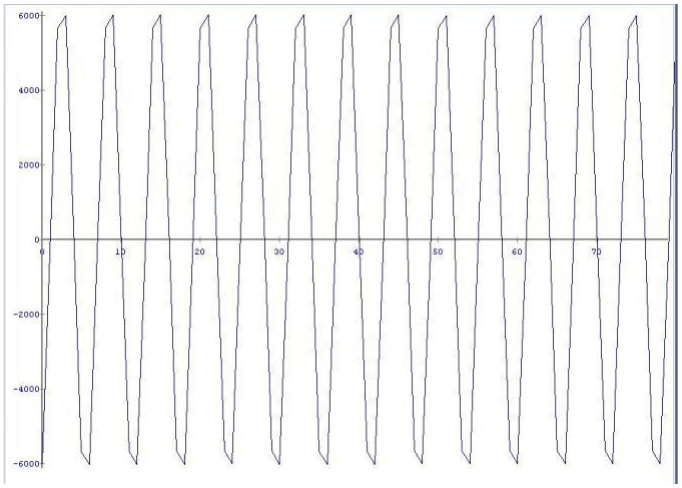


Figure 11: Data vs time filter output bus plot.

Figure 9 to 10 shows the chip scope results of generated data, the ADC output, and the filtered output respectively.

## 5. CONCLUSION

A filter as mentioned is one of the important module in the communication system. In order to enhance the receiver performance and its flexibility for the reception is improved using the proposed work. Using the proposed method the filter at the receiver to filter the received signal is dynamically selected by identifying the data rate of the received signed with the help of predefined training sequence.

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