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# Monitoring The Performance Of USB 3.0 Protocol Using System Verilog

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**Abstract -** *USB 3.0 is the protocol used for connecting computers to electronic devices and USB 3.0 architecture has these elements: Host, hub and device. The response time of the device and latency in data path between host and device and vice versa play a vital role to determine speed of USB3.0 IP. This paper explains about the latency in USB 3.0 IP in different data path.*

## 1. INTRODUCTION

USB 3.0 is the third major version of universal Serial Bus (USB). It is also called superspeed which can transfer up to 5Gbps (Giga bits per second).USB 3.0 is 10 times faster than USB 2.0 and have backward compatible with USB 2.0. USB 3.0 connector can be distinguishable from USB 2.0 by blue color coding of the receptacles, plugs and the initials SS.

USB 3.0 is similar to USB 2.0 but with many improvements and alternative implements. For example endpoint and transfer types are preserved but protocol and electrical interface have been changed.

In USB it is important to identify the latency of the transfer at each level and from device to host response of DP (Data packet) and TP (Transaction packet).There are different types of latency in USB 3.0 from which it is useful to find the delay at each point. And actions can be taken to increase the speed of the USB 3.0.

## 2. USB 3.0 ARCHITECTURE

Super speed bus is a layered communication that support following elements

**Interconnect**: super speed interconnects is one in which devices are connected to communicate with the USB 3.0 host through super speed bus.

**Device:** They implement required device end, to exchange information between the driver on the host and logic function on the device. It is passive part all transactions are initiated by Host only.

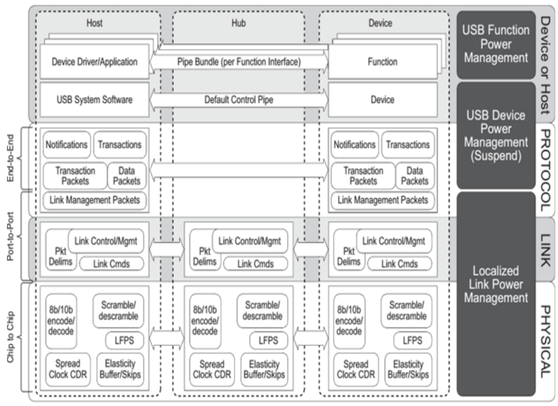


**Fig-1:** Architecture

**Host:** They implement required host end to exchange information between the bus. Its activity is to schedule and management of bus and all devices connected to it.

### 1.1 Physical layer

Physical layer defines the PHY portion of the port and connection between the downstream facing port on Host and upstream port facing port on a device. Physical layer consists of two differential data pair , one transmitter and one receiver path which supports 5Gbps data rate and link layer side it has PIPE interface.

The electrical aspects of the path are as transmitter, receiver and channel which collectively called as unidirectional differential link. At electrical level each differential link is initialized by enabling the receiver termination. The transmitter is responsible for the detection of far-end receiver termination and informs the link layer for further process.

PHY has its own clock domain with speed spectrum clocking modulation (SSC). The USB 3.0 doesn't support any reference clock on its own.

### 1.2 Link layer

Link layer defines the logical portion and connection between the link partners.

Logical portion of the port has:

A. State machine: Is used to manage the ends of the physical connection i.e., the initialization and event management which includes connect removal and power management.

B. State machine and buffering: Is used to manage the information exchange between the link partners. That is flow control, reliable delivery of header packets and link power management.

C. Buffering: Is used for data and protocol layer information exchange.

### 1.3 Protocol layer

Defines the end to end communication between the host and the device. USB 3.0 supports host directed protocol in which host directs data transfer to the device. The protocol layer communication is through exchange of packets. Packets are sequence of bits and defined by protocol to decode as either control information or data information. Host transmits protocol packets are routed through hubs and is received by the devices. Same in case of device, if device transmits protocol packets it routes through the hubs and reaches the host.

### 1.4 Devices

USB 3.0 devices share their base architecture with the USB 2.0 and are required to carry information for self-identification and generic configuration and functions it supports as mass storage is one of them.

All devices are assigned to the USB address. Each device has one or more pipes through which it communicate to the host. All device should support endpoint zero in the designated pipe to which the device control pipe is attached.

## 3. TRANSACTIONS

### 3.1 Bulk Transaction

Bulk transaction types are characterized by the ability to guarantee error-free delivery of data between the host and a device by means of error detection and retry. Bulk transactions use a two phase transaction consisting of TPs and DPs.

### 3.1.1 Bulk In Transaction

When the host is ready to receive bulk data, it sends an ACK TP to a device indicating the sequence number and number of packets it expects from the device.

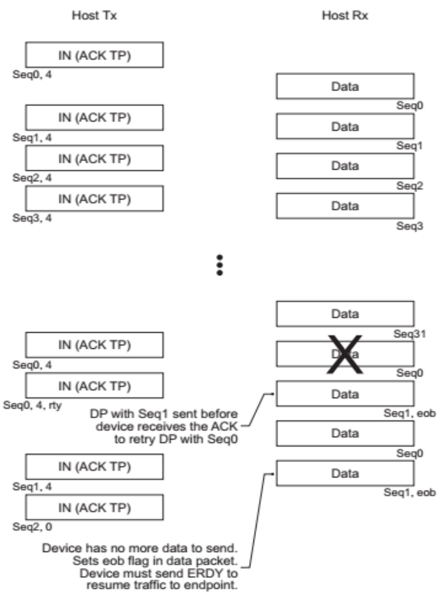


**Fig-2:** BULK IN Transaction

### 3.1.2 Bulk Out Transaction

When the host is ready to transmit bulk data, it sends one or more DPs to a device. If a DPH with valid values is received by a device it sends an ACK TP.

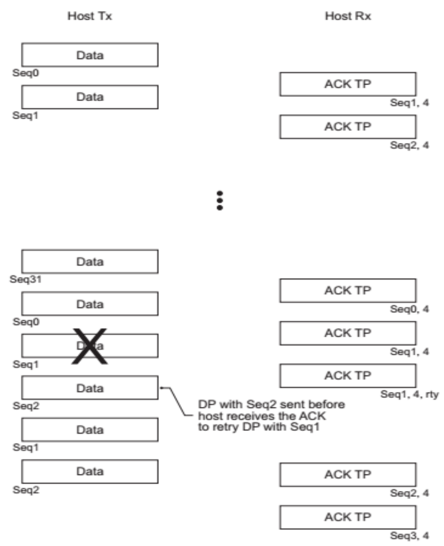


**Fig-3:** BULK OUT Transaction

## 4. LATENCY

Definition: In a computer network, it is an expression of how much time it takes for a packet of data to get from one designated point to another or source to destination. There are two types of latency they are end point latency and response latency.

To calculate the latency first need to find the start point and end point i.e., from which point to which point the latency is calculated. The monitor is placed in between the physical and link layer. Whatever signal we get from the physical layer will be scrambled to maintain the signal information. So at link layer descrambling is done and the calculation of latency is made after that point. To coupe up with the delay of descrambling and scrambling need to add time taken for descramble or scramble the data. The latency monitor is fixed in pipe interface. Monitor is a passive component, which monitors the latency of the USB. Latency signals are taken from RTL.

Between each layer interface is created from where signals are taken to calculate the latency. Then in response latency scrambler and descrambler is not used. Monitor signals are used to find latency which is placed near pipe interface. All Signals which is used for this is indentified using the type field and sub type field in the packets. Figure 4 shows how the monitor is placed.

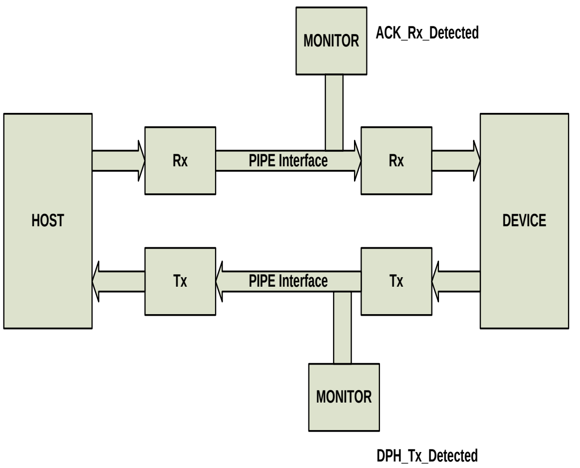


**Fig- 4:** Block diagram of Implementation

### 4.1 Types of Latency

### 4.1.1 End point latency

Definition: End point Latency is defined as the time between the input and output from each layer.

End point latency is checked for both IN FLOW and OUT FLOW at each layer. DPH for OUT FLOW is check from link layer to protocol layer and in protocol layer. In protocol layer DPH is checked and removed from the data packet. DPP for OUT FLOW latency is calculated from link layer, link to FIFO and FIFO to firmware. DPP takers more time because DPP will be saved in FIFO when DPH is been checked by the protocol layer. After protocol layer is checked then DPP will be read by the firmware.

IN FLOW DPH is calculated from protocol layer and protocol to link layer.DPP is done from Firmware to FIFO , FIFO and FIFO to link layer.DPP here also takes more time because after firmware writes the data to FIFO, header will be created by the by the protocol layer then the packet will be processed.

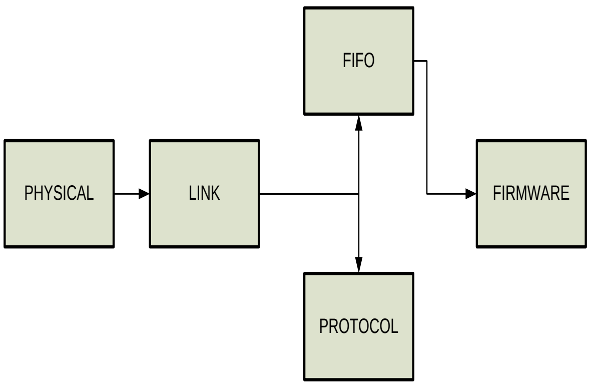


**Fig-5:** Layers to calculate latency

### 4.1.2 Response latency

Definition: Response latency is defined as the time required for the host or device to respond to the data received.

**IN FLOW:** Response Latency is defined as device response to host request.

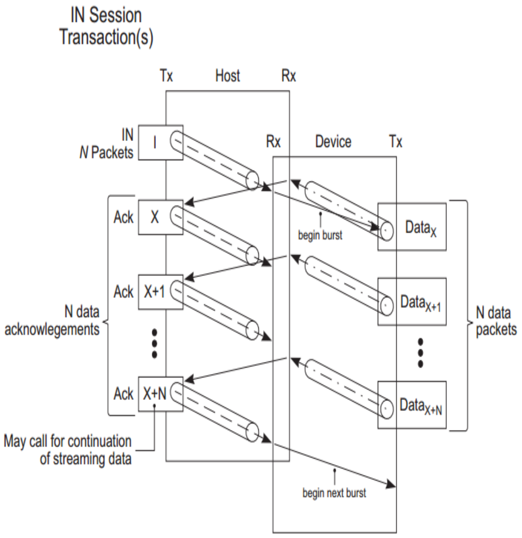


**Fig-6:** IN FLOW

An IN transfer on the SuperSpeed bus consists of one or more IN transactions consisting of one or more packets and completes when any one of the following condition
• All the data for the transfer is successfully received
• The endpoint responds with a packet that is less than the endpoint's maximum packet size.
• The endpoint responds with an error.

For IN FLOW latency is calculated from

1. ACK send by the host to the DPH send by the device in response.

2. DPH send by device to the LGOOD send by the host in response.

3. DPP send by the device together with DPH to ACK responded by the host to the DPP.

4. If device does not contain any data to send then device will send NRDY. Then host waits till it receives ERDY. so latency is checked from NRDY to ERDY.

**OUT FLOW**: Response latency is defined as host response to device request.

An OUT transfer on the SuperSpeed bus consists of one or more OUT transactions consisting of one or more packets and completes when any one of the following conditions
• All the data for the transfer is successfully transmitted.
• The host sends a packet that is less than the endpoints maximum packet size.
• The endpoint responds with an error.

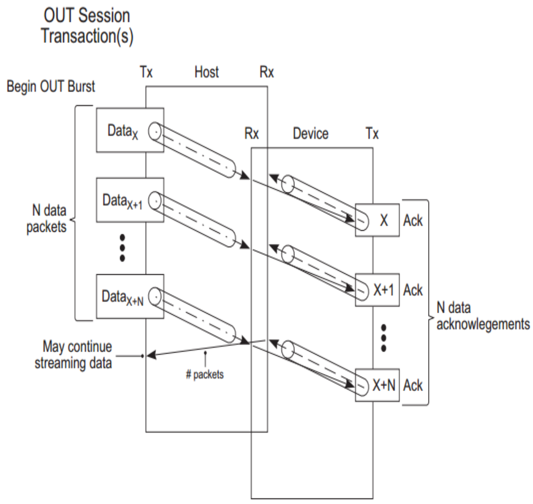


**Fig-7:** OUT FLOW

For OUT FLOW latency is calculated from

1. DPH send by the host to the LGOOD send by the device in response to DPH received.

2. DPP received by the device to the ACK responded by the device.

## 5. RESULTS

For both IN and OUT Transaction minimum and maximum latency is found out to improve the performance of the USB.

### 5.1 End point latency

In end point latency at each layer the latency is checked for both DPH and DPP. The results of which is shown in figure 8 and figure 9, results are in NANO seconds.

| OUT transmitted ( DPP ) | | | | | |
|---|---|---|---|---|---|
| Minimum latency | | | Maximum latency | | |
| link | fifo to link | fifo | link | fifo to link | fifo |
| 32 | 16 | 1659 | 32 | 16 | 1659 |

**Fig-8:** latency report in NANO seconds for IN Transaction of DPP

AT OUT flow latency is checked for both DPH and DPP. The results of which is shown in figure 10 and figure 11, results are in NANO seconds.

| DUT Received ( DPH ) | | | |
|---|---|---|---|
| Minimum latency | | Maximum latency | |
| link to protocol | protocol | link to protocol | protocol |
| 96 | 0 | 96 | 0 |

**Fig-9:** Latency report in NANO seconds for OUT Transaction of DPH

| DUT Received ( DPP ) | | | | | |
|---|---|---|---|---|---|
| Minimum latency | | | Maximum latency | | |
| link | link to fifo | fifo | link | link to fifo | fifo |
| 104 | 8 | 147 | 112 | 8 | 147 |

**Fig-10:** latency report in NANO seconds for OUT Transaction of DPP

### 5.1.2 Response latency

Response latency is calculated for IN and OUT flow. For IN flow from ACK to DPH, DPH to LGOOD, DPP to ACK and NRDY to ERDY latency is observed. Figure 12 shows the results of latency.

| Response Latency ( IN ) | | |
|---|---|---|
| | Minimum | Maximum |
| ACK To DPH | 238 | 302 |
| DPH To LGOOD | 82 | 98 |
| DPP To ACK | 104 | 132 |
| NRDY To ERDY | 0 | 696 |

**Fig-11:** Response latency for IN flow

Response latency out flow is calculated at DPH to ACK and DPP to ACK. Figure 13 shows the OUT latency.

| Response Latency ( OUT ) | | |
|---|---|---|
| | Minimum | Maximum |
| DPH To LGOOD | 134 | 170 |
| DPP To ACK | 260 | 370 |

**Fig-12:** Response latency of OUT flow

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