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Design and Analysis of Energy Efficient CMOS Arithmetic Circuits

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Abstract - *Energy efficiency is one of the most required features for modern electronic systems and those portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. For this purpose the two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). In this paper, we will present the design and performance of Arithmetic circuit featuring Centralized and CMOS design styles. We will carry out a comparison between these designs reported as having a low PDP (Power Delay Product), in terms of Speed, Power consumption and Area converted into prefabrication layout. Simulation of the schematic and layout realizations of the arithmetic circuit is performed using CMOS layout designing layout software and results are discussed.*

Key Words: **Arithmetic circuits, full-adder, high speed, low power.**

1. INTRODUCTION

As power dissipation has become one of the most important constraints in the design flow of electronic circuits. Therefore, under this common scenario, it has become extremely important to consider the power consumption of any proposed module. Fig.1 Shows the power consumption breakdown in a modern day high-performance electronics circuits.

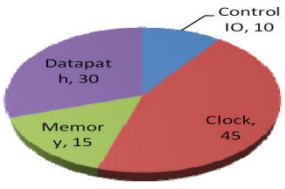

Fig. 1 Shows the power consumption breakdown in a modern day high-performance electronics circuits.

Due to rapid advances in electronic technology, electronics market is becoming more competitive, which results in consumer electronic products requiring even more stringently high quality. The design of consumer electronic products requires not only light weight and slim size, but also low power and fast time-to-market. Therefore, the integrated circuit (IC) designers have to consider more important issues such as chip area, power consumption, operation speed, circuit regularity, and so on. This is thanks to Moore's Law, which states that the number of transistors for a given die area doubles every eighteen months. However, as CMOS technology further scales down to allow faster IC with less energy consumption, continuous circuit innovation, in particular, logic implementation, is a necessity in order to avail its benefits.

2. LITERATURE REVIEW

VLSI systems has emerged as highly in demand because of the fast growing technologies low power building blocks to implement long-lasting battery operated system. Also VLSI has grown exponentially which helps designer to rely on increasing levels of automation to corresponding productivity gains.

Gauri Poshattiwar 1, Prof. Seema S Wasnik [1] in which ASIC and general purpose arithmetic circuits plays a very critical role. Multiple Valued Logic (MVL) provides the key benefit of a higher density per integrated circuit area compared to traditional two valued binary logic. As technologies are becoming more complex, multivalve logic (MVL) will be the future of circuit design. The advantages of lower power, higher performance, and reduced interconnect congestion motivate the use of quaternary circuits in a wide variety of applications.

1-bit CMOS full adder cells are studied using standard static CMOS logic style and are designed at the transistor level using 180nm CMOS technology by Manisha and Archana [3]. They carried out comparison using various parameters for selecting an adder which can give desired result according to a specific application.

3. PROPOSED WORK

In this paper, energy efficient CMOS arithmetic circuit will design with alternative internal logic structure in order to demonstrate its advantages and arithmetic

circuit will built in combination with pass-transistor powerless/groundless logic styles in order to reduce power consumption. Every step of proposed system design follows the design flow of Microwind 31 software the design methodology will be according to VLSI backend design flow. The main target is to design and analyze the hybrid architecture of CMOS for future high performance engines. Description proposed systems of flow chart are as follows:

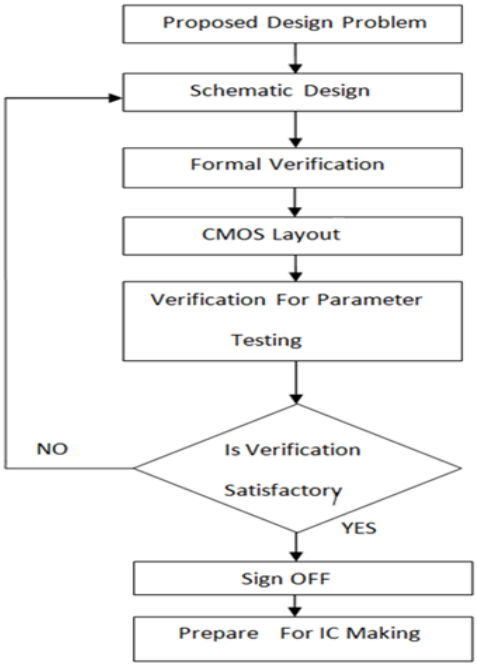

Fig. 2 Proposed system design flow

1. In this flow chart first we have to consider the proposed design problem, it is related to the PDP, area, frequency temperature.
2. Then we have to draw the schematic design related to the proposed system.
3. We make the formal verification.
4. After made the formal verification we have to draw the CMOS layout using Microwind 3.1 software.
5. After drawing CMOS layout we have to test and verify the each and every parameter related to the proposed system.
6. Then we check either the verification is satisfactory or not ,
   - If it is not satisfactory then we have to start repeating the process from step 2 respectively.
   - If it is satisfactory then we have to sign off the design procedure and move to the next step of design flow.
7. After sign off the design procedure we have to finally prepare for IC making.

4. RESULT AND DISCUSSION

The layout of all Arithmetic circuits is designed using Microwind 31 software for CMOS technology as shown below. These layout help as a reference model to construct a complete full adder and complete full substractor & multiplier circuit layout as well.

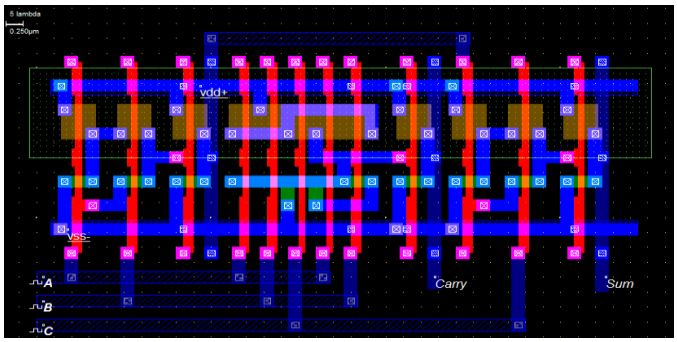

Fig. 3 CMOS Layout for Modified Full Adder

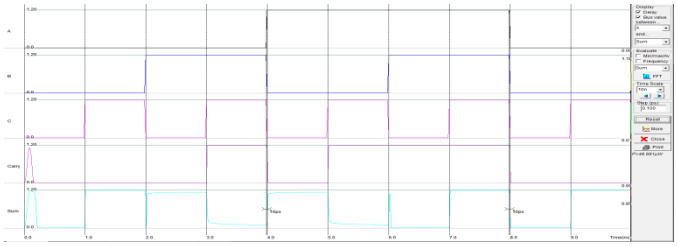

Fig.4 Response of Modified Full Adder

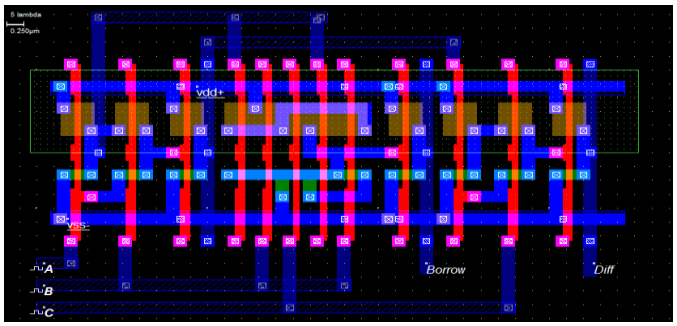

Fig.5 CMOS layout for Modified Full Substractor

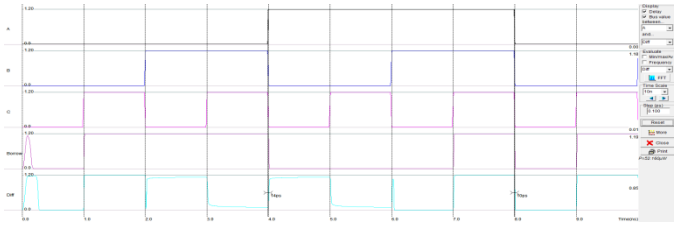

Fig.6 Response of Modified Full Substractor

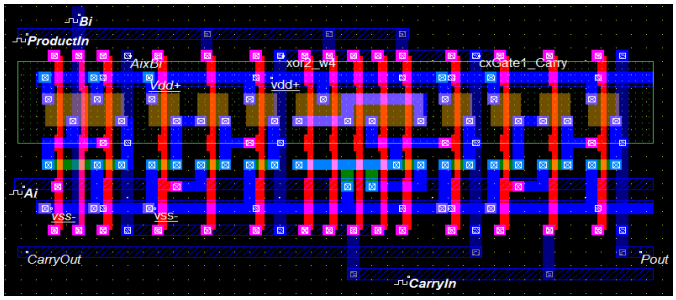

Fig.7 CMOS layout for Multiplier circuit

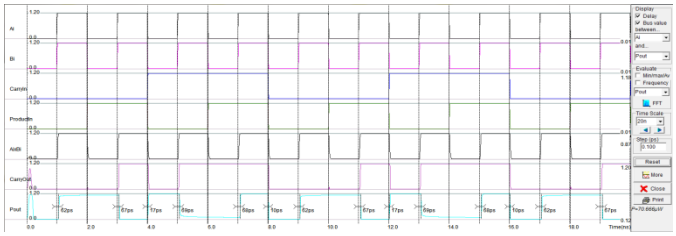

Fig.8 Response of the Multiplier circuit

We compare the conventional and modified Full adder and Full substractor using their CMOS schematic and CMOS layout. For this purpose the layout of conventional full adder and substractor is refer from the reference paper [4] and [5] respectively. In order to have a fair comparison we took the transistor sizes, Area, power, delay for both full adder as well as full substractor that were reported in the corresponding papers.

5. CASE STUDY

Summary of full Adder:

Circuit Parameters	Conventional Full Adder	Modified Full Adder
No. of transistor Required	28T	24T
Propagation Delay	17ps	10ps
Area	525.72um2	45.70um2
power	78.136uW	46.881uW
Maximum Freq.	58.82*10[9]Hz	1*10[11]Hz
PDP (Energy)	1.32*10[-15]	4.68*10[-16]

Table -1: Comparison table for Full Adder

From the above table-1 it is clear that convention full adder required maximum energy than the modified full adder and save energy is about 8.52*10[-16], so we can say that our project of energy efficient CMOS arithmetic circuit is energy efficient.

Summary of full Substractor:

Circuit Parameters	Conventional Full Substractor	Modified Full Substractor
No. of transistor Required	40T	32T
Propagation Delay	235ps	10ps
Area	3194.3um2	501.2um2
Power	2.74mW	52.160uW
Maximum Freq.	4.25*10[9]Hz	1*10[11]Hz
PDP (Energy)	6.43*10[-13]	5.216*10[-16]

Table -2: Comparison table for Full Substractor

From the above table-2 it is clear that conventional full substractor required maximum energy than the modified full substractor and save the energy is about 6.42*10[-13], so we can say that our project of energy efficient CMOS arithmetic circuit is energy efficient.

Summary of Multiplier:

Circuit Parameters	Binary	Ternary	Quaternary
Area	51.75um2	51.75um2	51.75um2
Propagation Delay	10ps	0.15ns	0.12ns & 21ps
Maximum Freq.	1*10[11]HZ	6.66*10[9]Hz	8.33*10[9]Hz 4.76*10[10]Hz
Power	70.66uw	0.107mW	49.03uw 0.167mw
PDP	7.066*10 [-16]	1.605*10 [-14]	5.88*10[-15] 3.507*10[-15]

Table -3: Comparison table for Multiplier

From the above table-3 clears summary of the multiplier in different logic system we can say that area for different logic system is same only power, propagation delay, and maximum frequency is different for different logic systems.

6. CONCLUSIONS

From the above table-1,2,3 it is clear that conventional full substractor & full adder required maximum energy than the modified full substractor as well as full adder and save the energy is about 6.42*10[-13], & 8.52*10[-16]. For the multiplier operated in different logic system required only different power, propagation delay, and maximum frequency. So we can say that our project of energy efficient CMOS arithmetic circuit is energy efficient.

7. FUTURE SCOPE

As in this project we design the modified full adder, full substractor, and multiplier circuits which consumes low power similarly by using the same logic we will design and simulate the application like comparator, ripple carry adder, divider circuits etc.

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BIOGRAPHIES

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