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COMPARATIVE ANALYSIS OF RDLMS

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Abstract - *The desired signal. Adaptive filters are having large range of applications as compare with other digital filters. Least mean square (LMS) algorithm is most popular and most commonly used on adaptive filtering for its simplicity, robustness, low hardware complexity and satisfactory convergence performance. Delayed LMS algorithm is a modified version or a variation in LMS algorithm suited in hardware implementation with performance degradation. To make this more achievable, this DLMS architecture is retimed to reduce the delay, speed, area and critical path and making it more responsive and less degradable. Analysis and design of LMS and DLMS algorithm is performed on MATLAB. RDLMS is implemented for 8 bit using Verilog code and the design of RDLMS is implemented by using Xilinx and ModelSIM software.*

Key Words*: *Adaptive filtering, LMS algorithm, Delayed LMS algorithm and RDLMS algorithm.

1. INTRODUCTION

The regular method of finding a signal which is corrupted due to additional noise has to pass it through a filter that tends to suppress the noise while leaving the signal relatively unchanged. For such a purpose fixed or adaptive filters can be used. The design of fixed filter is depend on previous knowledge of both the signal and the noise. On the other hand, design of adaptive filters requires little or no a priori knowledge of signal or noise characteristics. Also it has the ability to adjust their own parameters automatically. Here for noise cancellation, we have to use an adaptive filter. Noise cancellation technology is a growing field that aims to reduce unwanted signal. Adaptive noise cancellation is mostly used to get the desired signal from the given noisy signal. This is achieved by minimizing the mean square value of the error signal. The Least Mean Square (LMS) algorithm is the most popular and most widely used adaptive filter, because of its simplicity and satisfactory convergence performance. The LMS algorithm provides a powerful and computationally efficient means of realizing adaptive filters. LMS algorithm is used for the adaptation of the filter coefficients. The least mean square algorithm is popular for engineers involved in active noise control (ANC) [1].
A modified version of the least mean square (LMS) algorithm is a delayed LMS (DLMS) algorithm which has been introduced in order to obtain an efficient implementation of the LMS algorithm on VLSI circuits. In the DLMS algorithm, only one type of delay is considered.

Retiming is a transformation technique used to change the position of delay elements in a circuit without affecting the input/output characteristics of the circuit. In retiming, delay positions are changing from path so that critical path can be reduced to iteration bound. Retiming has many applications in synchronous designs such as reduction of the clock period of the circuit, reduction of the power consumption of the circuit and logical synthesis. RDLMS algorithm has many more advantages such as less critical path, computation time is less, high speed and less area.

1.1. Least Mean Square algorithm

Least Mean Squares (LMS) algorithm is one of the class of adaptive filter. It is used to imitate a desired filter by finding the filter coefficients that relate to producing the least mean squares of the error signal. A difference between the desired and the actual signal is called Error signal. It requires no calculations for correlation function and matrix inversion. It uses Mean Square Error (MSE) as a criterion.
The simplest estimation may use only the current available taps and the current desired response to estimate the autocorrelation matrix and the cross-correlation vector. The equation to adapt tap weights w(n) using the instantaneous taps x(n) and desired response d(n).
w (n+1) = w(n) + mu*x(n)e(n).....(1)
Where, mu is the step size, since the filter output is the convolution sum of the taps and tap weights
y (n) = x (n)w (n).....(2)
The estimated error signal e (n) is defined as the difference between the desired response and the filter response, or
e (n) = d (n) y (n).....(3)

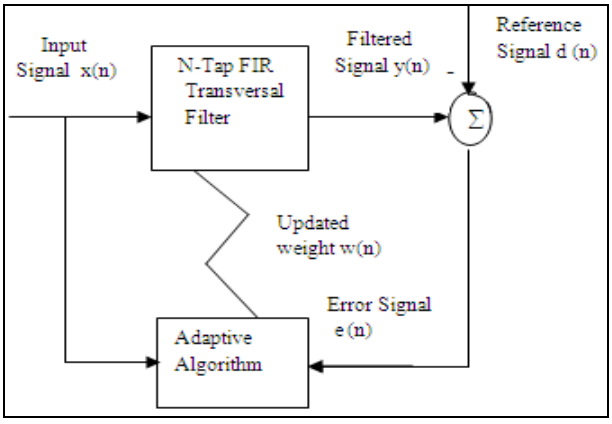

Fig-1: Schematic of LMS algorithm

1.2. Delayed Least Mean Square algorithm

A variation of the least mean square (LMS) algorithm is called the delayed LMS (DLMS) algorithm. The delay least mean squares (DLMS) algorithm is used to achieve lower adaption delay [4]. In DLMS algorithm, only one type of delay is considered. On the other hand, it is known that to implement fast adaptive filters working in real time, it is necessary to introduce different types of delay to allow a flexible architecture.

Error

e(n m) = d(n m) y(n m).....(1)

Delayed Coefficient Update

wn,i = wn1,i + enmxnim .....(2)

Where m is the delay in weight adaptive, N is the order of the filter and wn,i is the filter ith tap coefficient for the current time step n. in this case, the coefficients are updated using the error from the previous m time step, enm.

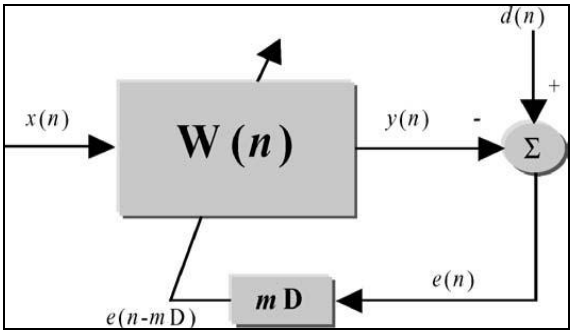

Fig-2: Schematic of DLMS algorithm

1.3. Retiming of Delayed Least Mean Square algorithm

Retiming is a transformation technique used to change the position of delay elements in a circuit. The purposes of retiming are to facilitate to minimize the clock period and to reduce number of registers needed. While pipelining produces a mechanism to reduce the critical paths and improve the speed performance. Pipelining of the adaptive LMS filter is difficult as it introduces delay in the error feedback loop. During the past two decades, many researchers have proposed several algorithms in order to overcome this difficulty. These approaches involve the modification of the adaptation algorithm to allow pipelining to be effectively implemented.

Retiming is used in synchronous designs including the reduction of the clock period of the circuit and the number of registers were reduced for a signal flow graph (SFG) by redistributing the delays. Retiming can be used to reduce the power consumption of a circuit by reducing switching, which can lead to dynamic power dissipation in static CMOS circuits. Unlike pipelining, retiming does not increase the circuit latency. By changing position of delays it makes us achieve to have critical path to iteration bound it is being explained in RDLMS more practically. Over that retiming have more advantages it slows circuit operation but computation time is less.

2. LITERATURE REVIEW

Retiming is considered as a transformation technique which is used in a circuit for changing the place of delay elements without affecting the input/output characteristics of the circuit. RDLMS algorithm has more advantages when it compare with LMS and DLMS algorithm.

2.1. The review in shows that the 8-bit/8-tap TF-FPDLMS and TF-RDLMS predictor systems are designed, simulated using VHDL netlist and implemented using the Xilinx Virtex-II FPGA technology resulting in a throughput rate of 170 Msample/s and critical path is 5.173ns which is less as compared to TF-FPDLMS predictor systems [1].

2.2. The three new fine-grained retimed DLMS (RDLMS) architectures is designed and achieved 66.7% reduction in delays, got 5 times faster convergence time, smaller area and a throughput rate of 182 Msample/s in the TF-RDLMS over the TF-FPDLMS circuit [2].

2.3. An efficient architecture for the implementation of a delayed least mean square Adaptive filter is presented and achieved less ADP and less EDP [4].

2.4. Now the authors presented the modified delayed LMS adaptive filter consist of Weight update block with Partial Product Generator (PPG) and achieved less ADP, less EDP and lower adaptation delay [5].

2.5. Performance Evaluation of LMS, DLMS and TVLMS Digital Adaptive FIR filters by using MATLB is presented and showed comparison among them [8].

3. DESIGN AND IMPLEMENTATION

An architectural implementation of the transposed DLMS is shown in Figure 3, where the algorithm is split into the weight update block and filter block. The filter block of the transposed form is identical to the transposed FIR with fixed coefficient [9].

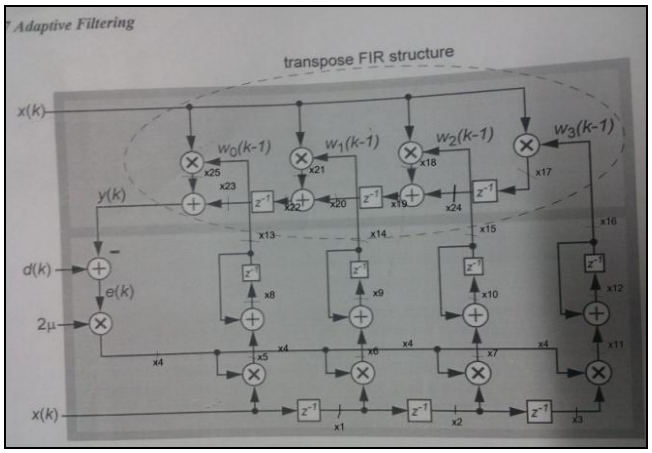

Fig-3: Transposed DLMS Architecture

An architectural implementation of the RDLMS is shown in Figure 4. The number of required registers such as delays, adders and multipliers in RDLMS architecture is very less as compare to DLMS. Due to less registers it takes less chip area, less delays, low critical path and higher speed.

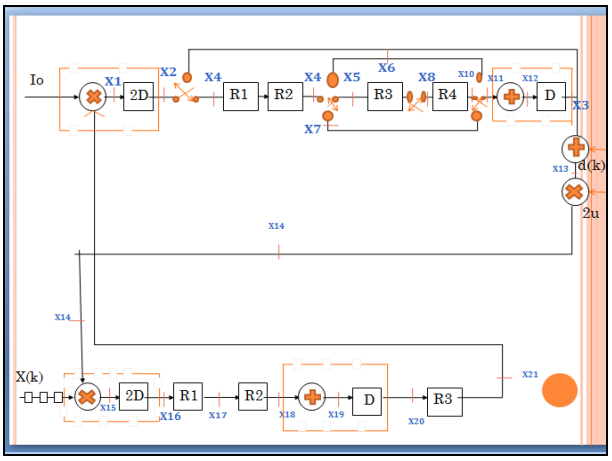

Fig-4: RDLMS Architecture

4. SIMULATION RESULT

As the figure 4 and figure 6 shows the output waveforms of the adaptive filter designed using LMS and DLMS algorithm. The design is coded and successfully simulated in MATLAB. First wave is an input sound wave, used as input signals for the design and it is a human speech signals acquired through audio player. During transmission noise get added in it and get noisy wave sound. The output of the filter is the noise free signal, getting after applying LMS and DLMS algorithm which is almost similar to the original audio signal. The command window shown in figure 5 and figure 7. The figure of merit used to measure the performance of the adaptive algorithms is the Mean square error or MSE. Minimum man square error (MMSE) for different sound signals are calculated. To perform the system improvement, peak signal to noise ratio (PSNR) is determined and it shows that SNR of filtered signal is improved.

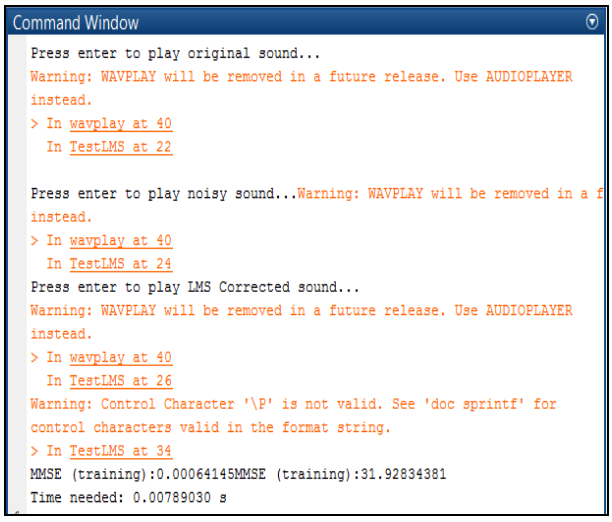

Fig-5: Output of LMS Adaptive filter in MATLAB

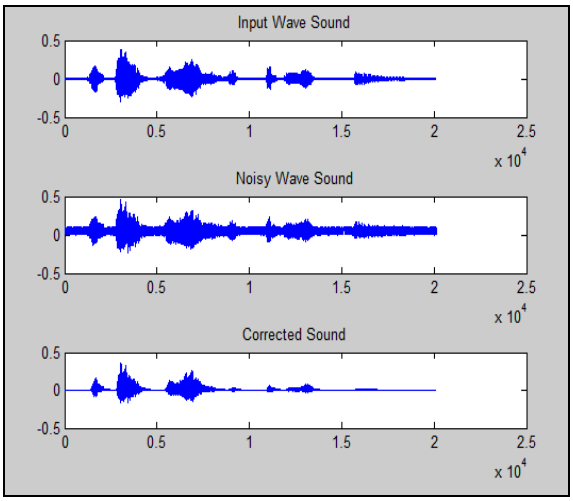

Fig-6: Result of LMS adaptive filter

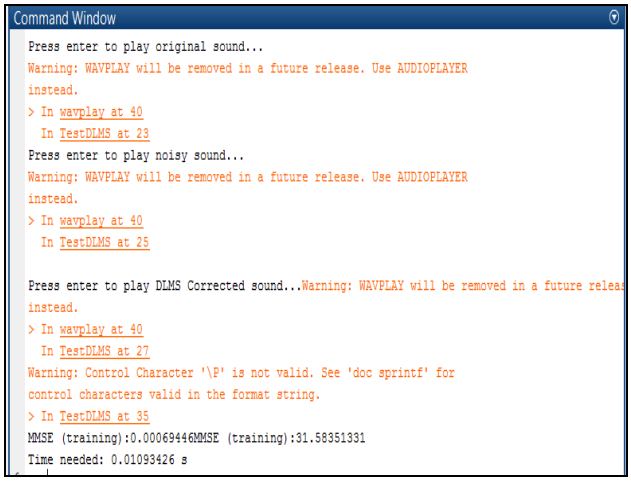

Fig-7: Output of DLMS Adaptive filter in MATLAB

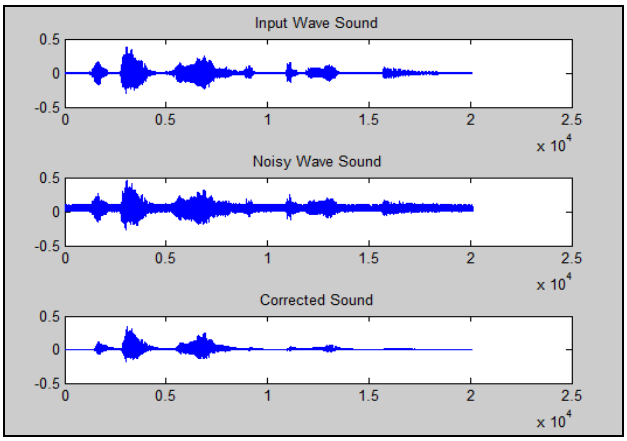

Fig-8: Output of DLMS Adaptive filter in MATLAB

The system tested for different sound signals. The output peak signal to noise ratio (PSNR) and minimum mean square error (MSE) of the different signals are measured for analysis.

The simulation result of RDLMS algorithm is shown in figure 9. The design is coded in Verilog and successfully simulated in ModelSim SE 6.2c software. Then it is implemented in Xilinx. Modelsim from Mentor Graphics is the tool used for pre-synthesis and post-synthesis simulation. Verilog language is used to model electronics systems and most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction.

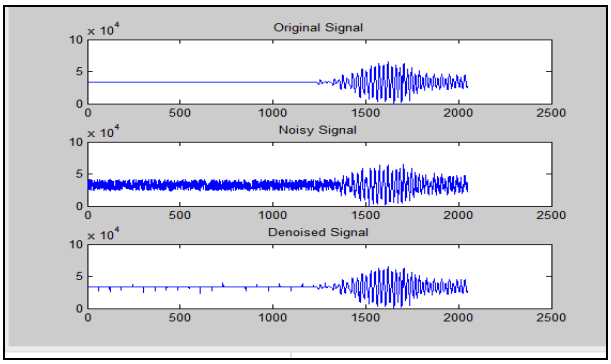

Fig-9: Result of RDLMS Adaptive filter

Due to less registers required in RDLMS architecture, it takes less chip area, less delays, low critical path and higher speed.

5. IMPLEMENTATION RESULTS

The aim of this project is to implement retimed delayed-LMS (RDLMS) algorithm for 8 bit which is mainly used for sound denoising and suitable for all types of VLSI filters and compare the behaviour of DLMS and RDLMS adaptive algorithms in terms of delay, chip area utilization, critical path and speed. The system is coded in Verilog, simulated in ModelSim SE 6.2c software and implemented in XILINX ISE software. The synthesis results are observed and shown in below figures.

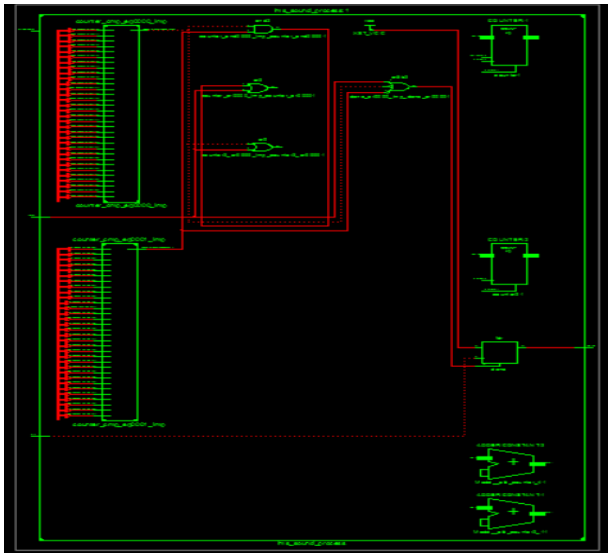

Fig-10: RTL View of 8 Bit RDLMS algorithm for adaptive filter

```
Offset:             2.826ns (Levels of Logic = 1)
  Source:           done (FF)
  Destination:      done (PAD)
  Source Clock:     clk rising

  Data Path: done to done
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               1    0.396    0.286  done (done_OBUF)
     OBUF:I->O                  2.144           done_OBUF (done)
    ----------------------------------------
    Total                       2.826ns (2.540ns logic, 0.286ns route)
                                        (89.9% logic, 10.1% route)
```

Fig-11: Delay required in RDLMS algorithm for adaptive filter

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	65	28800	0%
Number of Slice LUTs	210	28800	0%
Number of fully used LUT-FF pairs	65	210	30%
Number of bonded IOBs	3	480	0%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig-12: Device utilization summary of RDLMS algorithm for adaptive filter

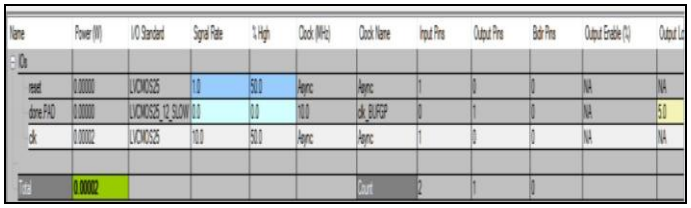

Fig-13: Power utilization summary of RDLMS algorithm for adaptive filter

6. CONCLUSION

In this paper, 8 bit implementation of RDLMS algorithm for adaptive filter is designed. The design is simulated in ModelSim SE 6.2c software and implemented using Xilinx ISE tool. A test bench is used for the generation of stimulus result and by implementing it for 8 bit using Verilog code, it become more efficient. Hence it can be used in more applications where maximum throughput matters. It is mainly used for sound denoising and suitable for all types of VLSI filters. The 8 bit implementation of RDLMS algorithm has delay of 1.2ns.

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