International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 07 | July-2016 www.irjet.net p-ISSN: 2395-0072

IC Layout Design of Decoder Using Electrical VLSI System Design

1.UPENDRA CHARY CHOKKELLA
Assistant Professor
Electronics & Communication Department,
Guru Nanak Institute Of Technology-Ibrahimpatnam (TS)-India
Mail: upendra433@gmail.com

2.ARAVIND ALAMPALLY
Assistant Professor
Electronics & Communication Department,
Guru Nanak Institute Of Technology-Ibrahimpatnam (TS)-India
Mail:aravind_alampally20@yahoo.com

Abstract*—This paper discusses the design of an Integrated Circuit (IC) layout for a decoder. The layout was designed by using an open source software namely Electric VLSI Design System as the Electronic Design Automation (EDA) tool. In order to produce the layout, the basic knowledge of fabrication process and IC design rules are expounded. The complete layout of the decoder was designed based on its schematic circuit, which consists of NOT gates, 2-input NAND gates, 3-input NAND gates, 4-input NAND gates, 2- input AND gates and 3-input AND gates. The layout had undergone Design Rule Check (DRC) set by the Electric VLSI Design System to check for any design rule error. Both layout and schematic circuit of the decoder were then simulated through Layout versus Schematic (LVS) to ensure they were identical. LTspice is used as simulator to carry out the simulation work and verify the validity of the function. The simulation output indicated that results of the layout and schematic circuit for decoder were essentially identical and matches the theoretical results.*

***Index Terms*—decoders, schematic circuit, IC layout, electric VLSI Design System, NAND gates, AND gates and simulation output**

I. INTRODUCTION

Electronic devices have been widely used in many different fields and the size of these devices has been gradually reduced. An example of this is the mobile phone which is made smaller to enhance user's mobility and usage time. These are the contribution of integrated circuit (IC) technology. With this technology, the modern devices have been reduced to convenient sizes. Besides that, mass production of IC has lowered the cost of production and made most electronic devices affordable. Today, an IC is smaller than a coin and can hold millions of transistors. Hence, further research in the design of IC is important to enhance the production of a more efficient and viable IC.

The main objective of this paper is to design an IC layout of a 7-segments decoder by Electric VLSI Design System. It is a free open source EDA system that provides service in handling IC layout, schematic drawing, textual hardware description language, and other features [1]. By using this software, a micrometer sized IC can be easily designed due to the availability of various features that can be used to design and check the IC layout. Moreover, Electric VLSI Design System also allows the schematic and layout design to be done in a systematic and efficient manner, thus saving time and reducing the production cost of the IC chip.

There are different technologies to construct integrated circuits such as bipolar integrated technology, NMOS technology and CMOS technology. In this project, CMOS technology is used. The main reason in using CMOS technology is due to its scalable high noise immunity and low power consumption. Basically, CMOS technology uses both NMOS and PMOS, which means only either one of both types of transistors will be ON at a time during the operation. Thus, CMOS IC consumes less power as power is used only when the NMOS and PMOS transistors are switching between on and off states [2].

II. LITERATURE REVIEW

A. 7-Segments Decoder

A 7-segments decoder is able to convert the logic states of inputs into seven bits of outputs and displays in 7-segments display. It is used widely in devices where its main function is to display numbers from a digital circuitry. Examples of these devices includes calculators, displays in elevator, digital timers, digital clocks and etc. There are many types of decoders such as 2-4 decoder, 3-8 decoder and 4-16 decoder. Since there are ten decimal numerals (0–9) to be displayed in the 7-segments display, a 4-16 decoder was used.

The structure of a 7-segments display is shown in Fig. 1. It is used to display decimal numerals in seven segments and each segment is represented by an alphabet '*a*' to '*g*'. By setting the required segments to be turned on, the desired decimal numeral can be displayed on the 7-segments display. The logic diagram of 7-segments decoder is shown in Fig. 2

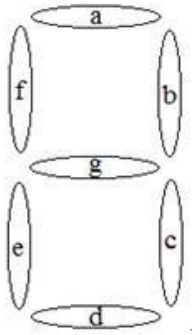


Figure 1. Structure of a 7-segments display

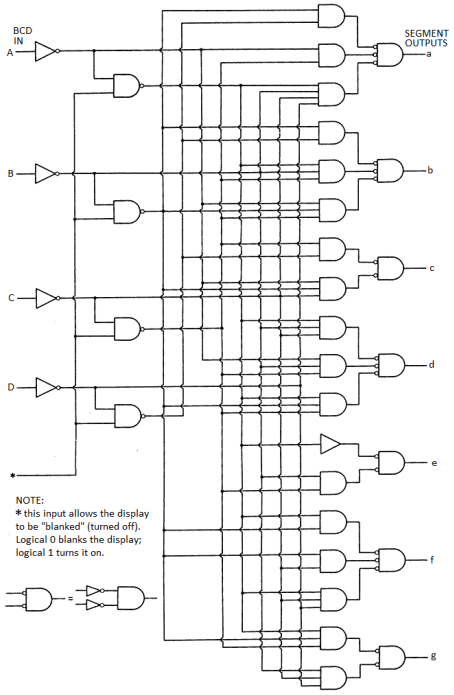


Figure 2. The logic diagram of a 7-segments decoder [3]

B. IC Design

IC layouts are built from three basic components which are the transistors, wires and vias. During the design of the layouts, the design rule has to be considered. Design rules govern the layout of individual components and the interaction between those components. When designing an IC, designers tend to make the components as small as possible enabling implementation of as many functions as possible onto a single chip. However, since the transistors and wires are extremely small, errors may happen during the fabrication process. Hence, design rules are created and formulated to minimise problems during fabrication process and helps to increase the yield of correct chips to a suitable level. Therefore, it is important to adhere to the design rules during layout design.

C. Physical Verification of Design [1], [4]

Physical verification is a process where an IC layout design will be checked via EDA tools to ensure it meets design criteria and rules. The verification process used in this project involves DRC (Design Rule Check), LVS (Layout Versus Schematic) and ERC (Electrical Rule Check). These are important procedures in IC layout design and cannot be treated lightly.

i) Design Rule Check (DRC)

DRC is a verification process that determines whether the physical layout of a chip design satisfies the Design Rules or not. It ensures that all the polygons and layers meet the manufacturing process rules that defines the limits of a manufacturing design such as the width and space rules. DRC is the first level of verification once the layout is ready. In this verification stage, the connectivity and guidelines rules will be checked as well. DRC will not only check the designs that are created by the designers, but also the design placed within the context in which it is going to be used. Therefore, the possibility of errors in the design will be greatly reduced and a high overall yield and reliability of design will be achieved.

ii) Layout Versus Schematic (LVS)

LVS is a process to check if a particular IC layout corresponds to the original schematic circuit of the design. The schematic acts as the reference circuit and the layout will be checked against it. In this process, the electrical connectivity of all signals, including the input, output and power signals to their corresponding devices are checked. Besides that, the sizes of the device will also be checked including the width and length of transistors, sizes of resistors and capacitors. The LVS will also identify the extra components and signals that have not been included in the schematic, for example, floating nodes. In Electric VLSI Design System, this type of checking is known as the Network Consistency Checking (NCC) as is able to compare any two circuits, which includes two layouts or two schematics.

iii) Electrical Rules Check (ERC)

ERC is usually used to check the errors in connectivity or device connection. It is an optional choice of checking and seldom used as an independent verification step. ERC is usually used to check for any unconnected, partly connected or redundant devices. Also, it will check for any disabled transistors, floating nodes and short circuits. ERC is very useful in accelerating debugging problems such as short circuits as can speed up the design process.

III. METHODOLOGY

The schematic circuit of the 7-segments decoder was drawn and debugging process had been carried out to ensure the design is error free. In this project, the layout of the 7-segments decoder was designed using Electric VLSI Design System to exploit its powerful editing tools.

Electric VLSI Design System is a high performance EDA tool that provides complete aids in designing the IC layout. It integrates the schematic editor, circuit simulator, schematic driven layout generator, layout editor, layout verification and parasitic extraction. Another advantage to Electric VLSI Design System is that it allows

swapping between the designs data with other standard
EDA tools in the industry. [1]

waveform viewer. It is used to simulate the outputs of both schematic circuit and layout during DRC and LVS.

There are basic design rules to be followed in order to design an IC layout successfully. These rules uses a universal parameter, λ. Fig. 3 shows the basic design rules commonly used in Electric VLSI Design System.

TABLE I. LIST OF FUNDAMENTAL RULE OF DESIGNING AN IC LAYOUT [5]

Well	
Minimum well size	12
Between wells	6
Between N-well and P-well	0
Minimum well area	144 ^{2}
Polysilicon1	
Polysilicon1 width	2
Between polysilicon1s	3
Between polysilicon1 and metal	N/A
Minimum polysilicon1 area	4 ^{2}
Polysilicon2	
Polysilicon2 width	7
Between polysilicon2s	3
Between polysilicon2 and metal	N/A
Minimum polysilicon2 area	49 ^{2}
Metal1,2,3,4,5	
Metal width	3
Between metals	3
Between metal and other metal	N/A
Minimum metal area	9 ^{2}
Via1,2,3,4	
Via width	2
Minimum via area	4 ^{2}
Metal6	
Metal6 width	5
Between metal6s	5
Between metal6 and other metal	N/A
Minimum metal6 area	25 ^{2}
Via5	
Via5 width	3
Minimum via5 area	9 ^{2}

Table I shows the basic design rule in a list. As shown in Fig. 3, the minimum distance between two same metals or polysilicons must be at least 3λ. Besides, the width of metal from 1 to 5 must be at least 3λ wide. Notice that in Table I, some parameter's rule are labeled as 'N/A'. This is because there are not such spacing rules. In other words, the respective components can be placed overlapping each other. Also, there are rules where the parameter is 0λ. This indicates that the respective components can be placed side by side without any space in between. There is also no minimum distance between vias or with other components listed in the table. This is because the vias available in Electric VLSI Design System are combined with 2 metals, covering every side of the vias. Therefore, before the vias can be placed nearer to each other, the metal surrounding it will connect each other first. The distance between the metal of vias has to obey the rules before the vias have the chance of contact. In other words, it also indicates that the minimum distance between vias or with other components can be determined through the metal's rule.

Besides that, LTspice IV simulation software was also used in this project. It is a high performance SPICE simulator that provides a schematic capture a

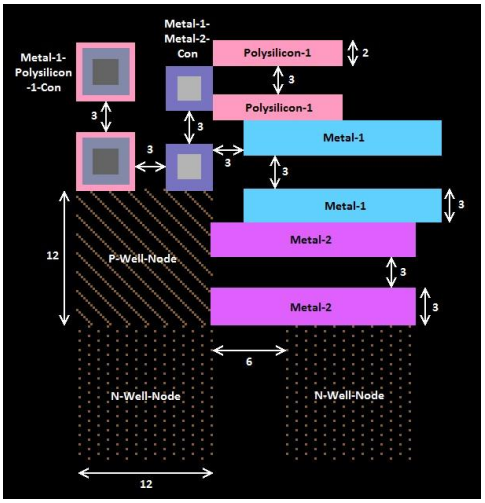


Figure 3. Fundamental rule of designing an IC layout (All values are in lambda) [5]

IV. FINDINGS

In this project, an IC layout of a decoder that displays the decimal numeral in 7-segments display was designed. It consists of NOT gates, 2-input NAND gates, 3-input NAND gates, 4-input NAND gates, 2-input AND gates and 3-input AND gates. The schematic circuits and layouts of all these gates were drawn and simulated using Electric VLSI Design System. Also, LTSpice was used as external simulator to generate the simulation waveforms.

A. 2-Input NAND Gates

Fig. 4 and Fig. 5 shows the schematic diagram and layout design of a 2-input NAND gate using Electric VLSI Design System.

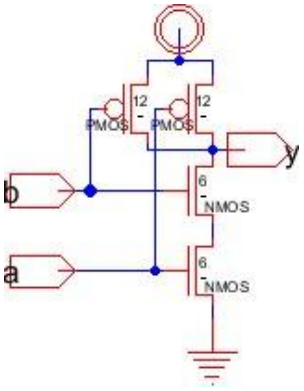
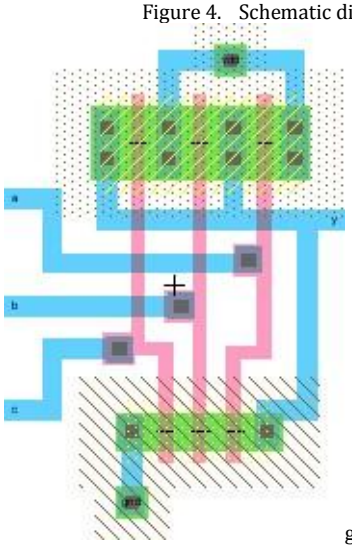


Figure 4. Schematic dia



gram of a 2-input NAND gate

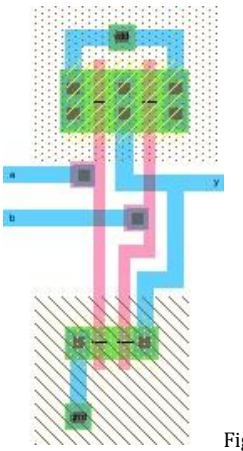


Figure 5. Layout design of 2-input NAND gate

B. 3-Input NAND Gates

Fig. 6 and Fig. 7 show the schematic diagram and layout of a 3-input NAND gate.

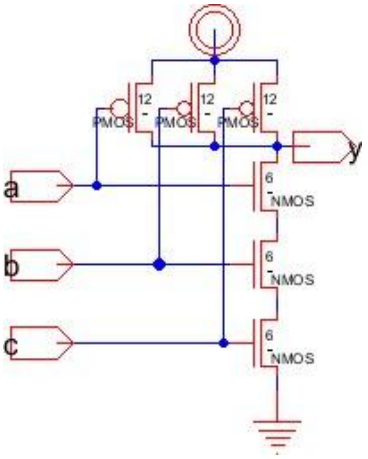


Figure 6. Schematic diagram of a 3-input NAND gate

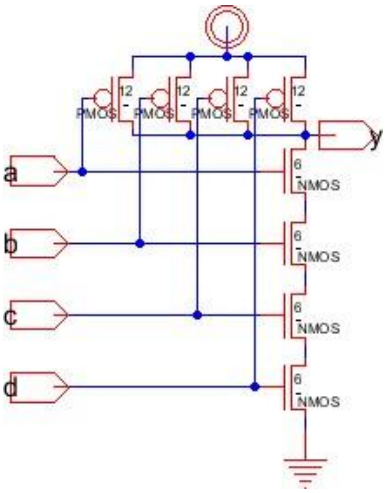


Figure 7. Layout design of a 3-input NAND gate

C. 4-Input NAND Gates

Fig. 8 and Fig. 9 show the schematic diagram and layout of a 4-input NAND gate, respectively.

Figure 8. Schematic diagram of 4-input NAND gate

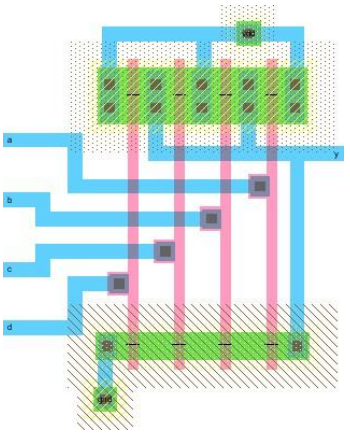


Figure 9. Layout design of 4-input NAND gate

Fig. 10 shows the 4-input NAND gate symbol and spice code. The code was required and used to complete the simulation process. The input wire are named as '*a*','*b*', '*c*' and '*d*'; whereas output wire is named as '*y*'. Simulation result of the 4-input NAND gate is shown in Fig. 11. If all the inputs of the 4-input NAND gate are '1', the output will be '0'. Meanwhile, whenever there is '0' among the inputs, the output will be '1'. In addition, due to the capacitance, the fall in the waveform actually indicates a logic '0' whereas the rise in waveform indicates a logic '1'. From the waveform generated, as shown in Fig. 11, the results are match with the theoretical 4-input NAND gate. It can be deduced that the

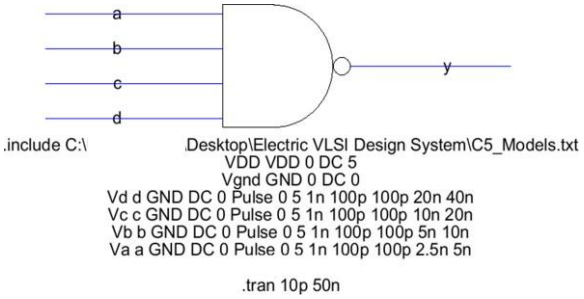


Figure 10. Icon of 4-input NAND gate and spice code

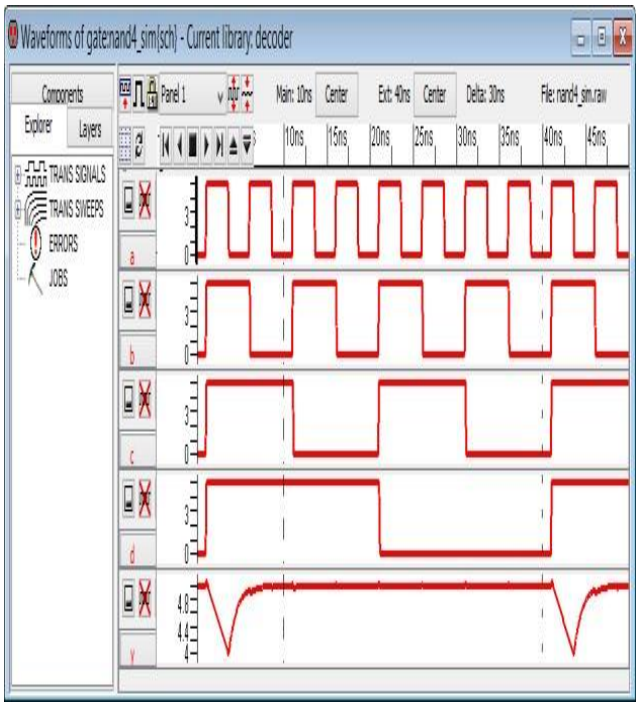


Figure 11. Simulation result of the 4-input NAND gate

D. 7-Segment Decoder

All the schematic diagrams and layouts of the basic gates drawn have to go through the physical verification process before simulation. These are the essential procedures to ensure the validity outputs results of the system.

Based on the logic diagram of 7-segment decoder, the schematic circuit and its IC layout was designed using Electric VLSI Design System tool, as shown in Fig. 12 and Fig.13,respectively 4-input NAND gate drawn by using Electric VLSI Design System operates correctly.

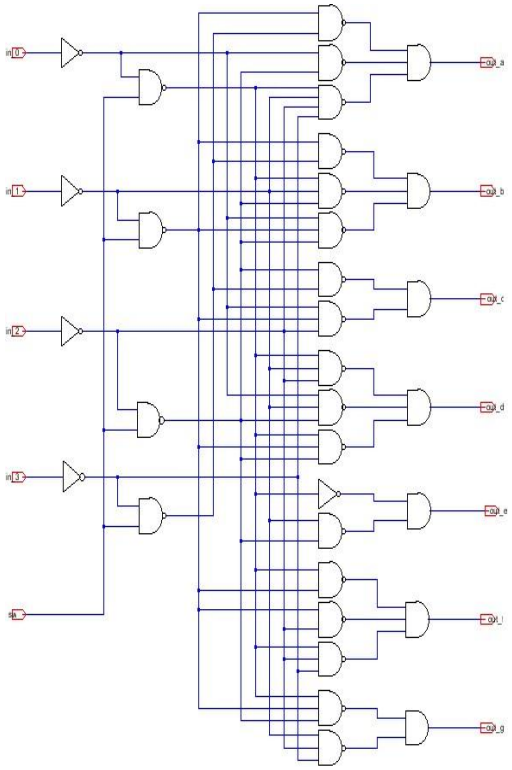


Figure 12. Schematic diagram of a 7-segments decoder

However, Fig. 14 shows the icon view of the decoder with spice code, which is ready for simulation. It shows the inputs and outputs port and also the spice code that specifies the input pulses of the decoder for simulation. There are five inputs: 'in_0', 'in_1', 'in_2', 'in_3' and 'sw', where 'in_0' is the least significant bit and 'in_3' is the most significant bit. Since it is a 7-segment decoder, seven outputs will be needed. These outputs are labelled as 'out_a', 'out_b', 'out_c', 'out_d', 'out_e', 'out_f' and 'out_g'. Notice that there is a 'sw' input which represents the switch. When the switch is to '0', no matter what other inputs are, the outputs will always be '0'. When the switch is to '1', the outputs will be varied according to the binary combination of the inputs.

Fig. 15 is the simulation waveform generated with different inputs. It is known that as long as the 'sw' is off, truth table of the binary-convert-decimal, as shown in Table II, the designed decoder is match with the theoretical work and said to function as expected.

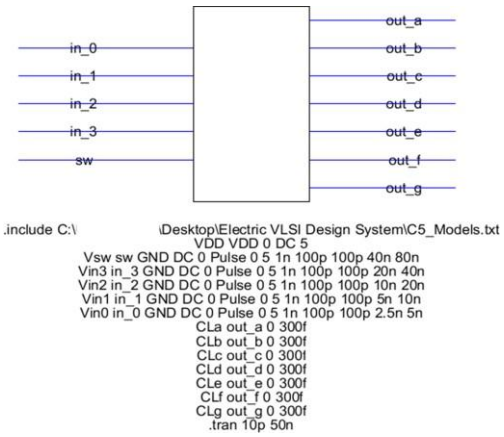


Figure 14. Icon of decoder and spice code

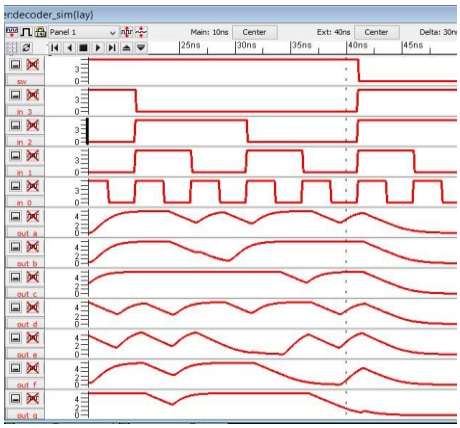


Figure 15. Simulation result of the 7-segments decoder

TABLE II. TRUTH TABLE OF BINARY-CONVERT-DECIMAL (BCD)

	INPUT				OUTPUT						
No	in_3	in_2	in_1	in_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

V. TROUBLESHOOTING

In order to avoid inability to run the simulation, the following steps have to be taken:

the outputs will be '0'. This figure shows simulation waveform for when the 'sw' is off. In reference to the

A. Setting and Installation

Before start drawing the schematic circuit, all the setting of the Electric VLSI Design System must be done properly. These include the installation of external simulator of LTSpice, setting of spice engine and its path, technology and scale used.

B. Verification Process

As mentioned earlier, physical verification process is an essential procedure. The schematic diagram and layout design can be checked through DRC. It is recommended that the schematic diagram is free of warning and error before designing its layout.

LVS is used to ensure that the schematic diagram and its layout are identical. This process will check the number of exports, ports, transistor size between schematic and the layout. Error may occur if they are not consistent.

While running the LVS, the library names for both schematic and layout have to be same and place under the same group. This is to ensure that the software compares the correct library.

C. Spice Code

In Electric VLSI Design System, spice code is used as function to be read by LTspice in order to simulate the waveform. A proper and correct spice code will generate correct waveform through this simulator. Spice code is written and inserted in the icon view of the decoder before running simulation. It specifies the input pulses and all the ports of decoder. The code written must be consistent with the icon drawn.

VI. CONCLUSION

In conclusion, 7-segments decoder IC is to display the numbers in 7 segments. It converts the binary input to 7 bits according to the input. The IC layout of the decoder is designed and successfully proves that the output waveforms generated matches the theoretical decoder.

In addition, the open source Electric VLSI Design System is a user friendly software to be used in designing a layout of 7-segments decoder. It is expected that the software is able to cope with more complex digital IC design with its suite of verification and design tools.

REFERENCES

[1] About Electric. (May 2013). [Online]. Available: www.staticfreesoft.com/electric.html
[2] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, John Wiley & Sons, 2010, pp. 6-12.
[3] M. M. Forrest, *Understanding Digital Computers*, Radio Shack, 1987.
[4] S. H. Teen and S. Y. Lee, "CMOS IC layout design: 7-segments counter," *Lecture Notes on Photonics and Optoelectronics*, vol. 1, no. 2, pp. 52-55, December 2013.
[5] A. P. Douglas and E. Kamran, *Basic VLSI Design*, 3rd ed., Prentice Hall, 1994, pp. 72-76.