DESIGN AND SIMULATION OF SIGMA DELTA MODULATOR USING SWITCH CAPACITOR ARCHITECTURE

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Abstract - *The paper presents deep insights of design and simulation of the Delta-sigma modulation scheme to convert Analog signals to Digital Signals using Cadence Virtuoso Design tool. Here Sigma Delta Modulator analog signals are encoded into digital signal as in regular ADC. The main thrust behind the Delta modulation was to accomplish higher transmission proficiency by transmitting the progressions (delta) in quality between the back to back examples instead of genuine samples themselves. Since there is no restriction to the quantity of pulses of the similar sign that may happen, this frameworks are equipped for following signals of any adequacy. In this work, it is explained about the design and simulation of Integrator, Latched Comparator, Ring Oscillator, Digital To Analog converter which are combined together to form the Sigma Delta Modulator using the 350nm CMOS technology, which has been simulated using Cadence Virtuoso tool.*

Key Words: **Comparator, DAC, Integrator, Ring Oscillator, Sigma-delta conversion.**

1. INTRODUCTION

Delta-sigma modulation *(ΔΣ; or sigma-delta, ΣΔ)* is a digital signal preparing, or DSP technique for encoding continuous data into digital data as found in an ADC. It is additionally used to exchange higher-determination digital data into lower-determination digital data as a feature of the procedure to change over digital data into analog. In an ordinary ADC, an analog data is coordinated, or tested, with an examining recurrence and in this way quantized in a multi-level quantizer into a digital data. This procedure presents quantization mistake clamor [1].

The initial phase in a delta-sigma balance is delta modulation. In delta modulation the adjustment in the data (its delta) is encoded, as opposed to the total worth. The outcome is a flood of pulses, instead of a surge of numbers just like the case with PCM. In delta-sigma modulation, the precision of the modulation is enhanced by passing the digital yield through a 1-bit DAC and including (sigma) the subsequent analog data to the information data, along these lines lessening the mistake presented by the delta-modulation.

The most striking element of a sigma delta modulator, which is the primary segment of sigma delta ADCs, is that these modulators utilize a high sampling rate. The sampling rate utilized is as a part of the scope of MHz, which is greater than the Nyquist rate, for the most part in the scope of kHz. Thus, the oversampling proportion is great, in light of which these are now and then alluded to as oversampling ADCs. The upside of utilizing this high sampling proportion is greater resolution of the digitized yield and better noise shaping. Fig. 1 shows the block digram of sigma delta modulation block.

Sigma-Delta modulation [2] changes over the continuous voltage into a pulse recurrence and is on the other hand known as Pulse Density modulation (PDM) or Pulse Frequency modulation. All in all, recurrence may change easily in tiny steps, even voltage, and both may serve as an analog of an imperceptibly fluctuating physical variable, for example, acoustic pressure, intensity of light and so on. The substitution of recurrence for voltage is along these lines altogether common and conveys in prepare the transmission upsides of a pulse stream.
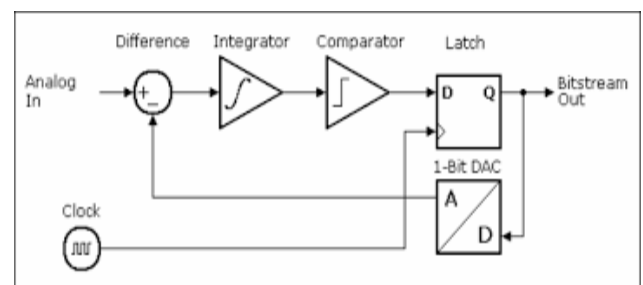

Fig 1: General block diagram of Sigma delta modulator [1].

The *Switch Capacitor principle* is used mainly because it controlled movement of charge and other importance is Integrated capacitors are easier to fabricate than resistors [3]. The average resistance approximated through charge movement. Fig 2 shows the operation of switch capacitors where the Mosfets acts as switches and helps in charging and discharging of the capacitor.

$$I = V / R, \quad Q = C V \qquad (1.1)$$

$$I_{average} = Q \, f_s = C V \, f_s \qquad 1.2)$$
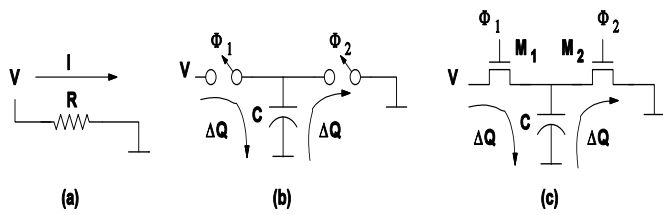
$$\Rightarrow \quad R_{eq} = 1 / Cf_s \qquad (1.3)$$

Fig 2: Switch capacitors working [3].

For switch capacitors there are some constraints which has to be followed like,

❖ Switches Φ_1 and Φ_2 can never be closed at the same time.
❖ Switch Φ_1 must have time to open before switch Φ_2 closes.
❖ Switch Φ_2 must have time to open before switch Φ_1 closes.
❖ Frequency f_s must allow enough time for the circuits to fully   charge and discharge.

For any circuit clock is very important. In this work, a ring oscillator is acknowledged by setting a few number of open-loop transforming amplifiers in a feedback circle. The least complex sort of amplifier that can be utilized is a straightforward digital inverter [4], as shown in Fig. 3.
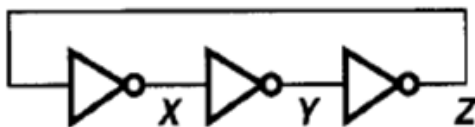

Fig 3: Ring oscillator using inverters

The circuit will oscillate and for every half-period, the data will spread around the circle with a reversal. This change will proliferate through every one of the three inverters in a period of T/2, at which time the yield of the main inverter will change to 0 and after an extra time of T/2 the principal inverter's yield will change back to 1. Expecting every inverter has a delay of τp and N number of inverters we can write,

$$\frac{T}{2} = N\tau_p \qquad (1.4)$$

Thus, $f_{osc} = \dfrac{1}{2N\tau p}$ \qquad (1.5)

With these things in mind, authors have designed different blocks of sigma delta modulator. Second section of this paper shows the details of the design of sub blocks like inverter for ring oscillator, op amp as integrator and comparator, DAC design followed by the third section which gives all the simulation results. Towards the end of this paper, the writers have concluded the work with the analysis of their results followed by the future scope.

2. DESIGN PROCEDURE

The designed circuit's simulation is carried out using *Cadence virtuoso tool,* here we need to find out few parameters which are important for design procedure. The several parameters are shown below,

❖ μ_p = 55μ m^2
❖ μ_n = 350μ m^2
❖ C_{ox}= 8.78mF.
❖ V_{tp} = -512.817mV
❖ V_{tn} = 547.66mV

2.1. Inverter design for ring oscillator

Inverter is the basic circuit for any system, since it is digital circuit we need to concentrate on making switch on and switch off time equal with the help of DC operating point= Vdd/2. The aspect ratios of the mosfets used for inverter after design are shown in table 1

Table 1: Aspect ratios of Inverter.

MOSFET	WIDTH (w)	LENGTH (l)	Aspect ratio w/l
M1 (PMOS)	3.5μ	350n	10
M2 (NMOS)	700n	350n	2

The required ring oscillator has be working at the frequency of 1.2MHz and with a power supply of 1.8V. Using the cmos inverter design, five stages of same inverter are used, and a capacitor of 21.5pF is used at the end of each stage for better charging and discharging of the signal generated. Further two inverter stages are added for getting proper square shaped signal of uniform frequency.

2.2. Op Amp design for integrator and comparator

For any analog circuit design, choose the lowest gadget length which will keep the channel modulation component constant and provide proper toning for current mirrors.

❖ Capacitance C_c is found using the equation,
$$C_c \geq 0.22\ C_L \qquad (2.1)$$
❖ I_5 is found using the equation,

$$SR = \frac{I5}{Cc} \qquad (2.2)$$

❖ M_1 and M_2 are found using the equations,

$$gm1 = GBW \times C_c \times 2\pi \qquad (2.3)$$

$$I_D = \frac{\mu n C_{ox}}{2} \left(\frac{W}{L}\right)(V_{gs} - V_t)^2 \qquad (2.4)$$

❖ M_3 and M_4 are found using the equations,

$$V_{d1} > V_{g1} - V_{t1} \qquad (2.5)$$

$$I_D = \frac{\mu n C_{ox}}{2} \left(\frac{W}{L}\right)(V_{gs} - V_t)^2 \qquad (2.6)$$

❖ M_5 and M_8 are found using the equation,

$$V_d = V_{gs} - V_t, \qquad (2.7)$$

❖ M_1 and M_2 are found using the equations,
$$Gm6 \geq 10\, gm1 \qquad (2.8)$$

❖ M_6 and M_7 are found using the equations,

$$\frac{I6}{I4} = \frac{\left(\frac{W}{L}\right)6}{\left(\frac{W}{L}\right)4} \quad \text{and} \quad \frac{I6}{I5} = \frac{\left(\frac{W}{L}\right)7}{\left(\frac{W}{L}\right)5} \qquad (2.9)$$

Using these equations, any two stage op amp can be designed. Thus the designed op amp can be modified as integrator or comparator depending on our application.

For integrator we need frequency operation of 50MHZ, and feedback resistance of 1KΩ. The switch capacitor is used to replace the feedback resistor using the relation,

$$f = 1/CR \qquad (2.10)$$

Using equation 2.10, the switch capacitance value is found to be 20pF and the aspect ratios of the mosfets used for op amp are shown in table 2.

Table 2: Aspect ratios for Op amp

MOSFET	WIDTH (w)	LENGTH (l)	ASPECT RATIO $\left(\frac{w}{l}\right)$
M1 , M2	2.1μ	350n	6
M3 , M4	4.9μ	350n	14
M5	4.2μ	350n	12
M6	60.9μ	350n	174
M7	22.75μ	350n	65

The same Op amp can be modified into comparator, the clock signal which is generated from ring oscillator is latched to the comparator and the desired operating frequency is 1.2MHz.

2.3. Digital to analog converter

A one bit DAC has to be designed in order to convert the digital output signal into analog and fed back to the summer circuit, so the difference in the feedback signal and input can be again used for precise modulation.

DAC consists of a CMOS inverter along with two transmission gates. The designed and obtained aspect ratios are shown in table 3.

Table 3: Aspect ratios for DAC

MOSFET	WIDTH (w)	LENGTH (l)	ASPECT RATIO $\left(\frac{w}{l}\right)$
Inverter PMOS	10μ	350n	28.58
Inverter NMOS	1μ	350n	2.85
T1 PMOS	1μ	350n	2.85
T1 NMOS	30μ	350n	85.72
T2 PMOS	1μ	350n	2.85
T2 NMOS	400n	350n	1.14

3. SIMULATION RESULTS

3.1. Ring oscillator

The Simulation of the designed circuits are carried out in *ADEL* using *Cadence EDA tool* using *gpdk350nm* technology.

The schematic of the ring oscillator having five stages of inverter followed by two inverters for better shaping of signal is shown in fig 4.
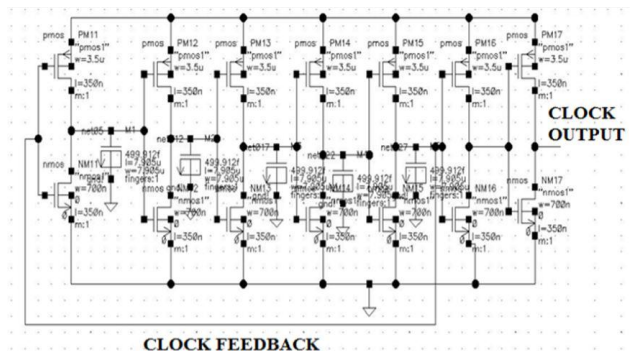

Fig 4: Schematic of Ring oscillator.

The simulated waveforms of the ring oscillator is shown in fig 5. Here we can see the circuit has taken initial delay of 500ns for generating sustained oscillations and the uniform frequency of 1.2MHz has been generated which is used as clock signal for comparator stage.
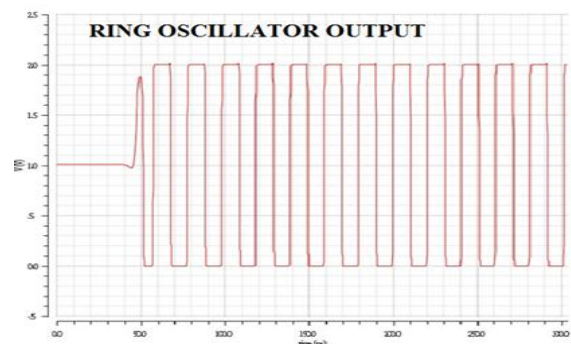

Fig 5: Clock signal generated by Ring Oscillator.

3.1. Comparator design

Two stage Op amp is used for comparison purpose. Fig 6 shows the schematic of designed operational amplifier and Fig 7 shows the gain and phase plot of the same circuit. The gain is found to be 60dB which is sufficient for two stage Op amp.

The designed Op amp is latched by the clock signal generated by ring oscillator in order to perform as comparator, where the output of integrator is compared with the clock frequency to provide final modulated signal.
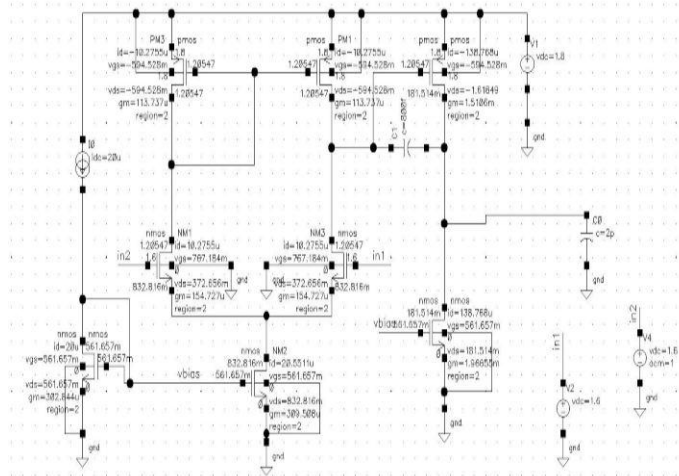

Fig 6: Two stage Op amp.
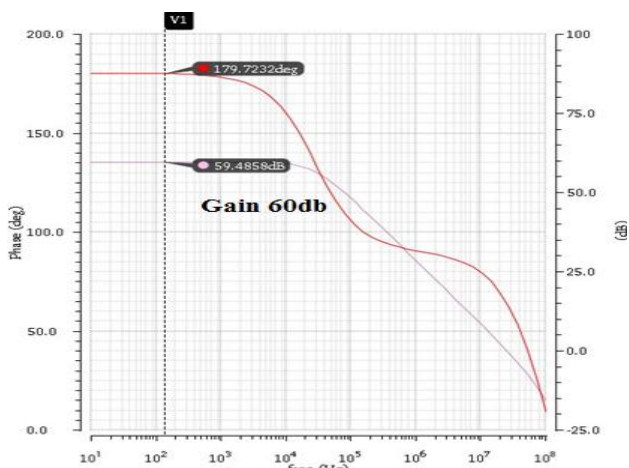
Fig 7: Gain plot of two stage Op amp

The schematic of the comparator is shown in fig 8. Where the comparator provides with two outputs which are shown in fig 9.
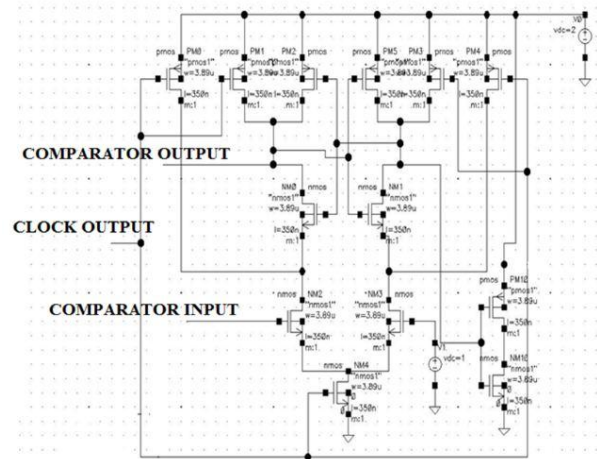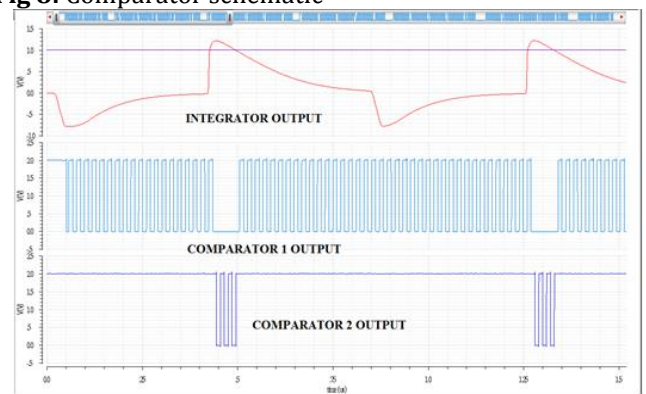

Fig 8: Comparator schematic

Fig 9: Simulated output of comparator.

3.2. DAC and integrator design

The schematic of DAC is shown in fig 10 and the designed integrator circuit is shown in fig 11.
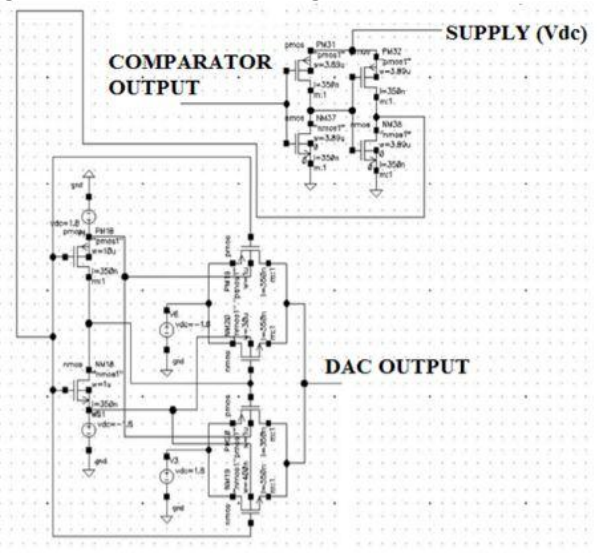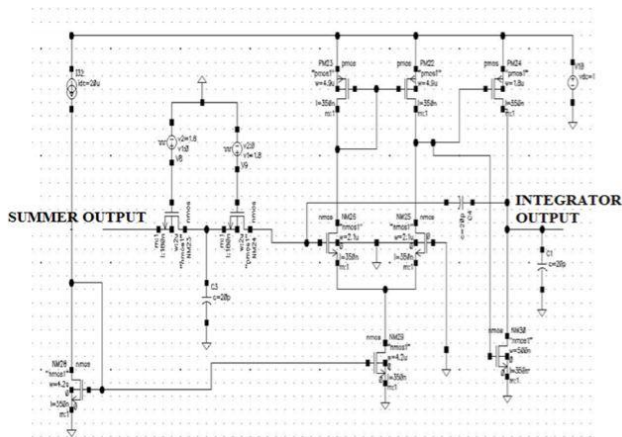

Fig 10: DAC schematic

Fig 11: Integrator schematic.

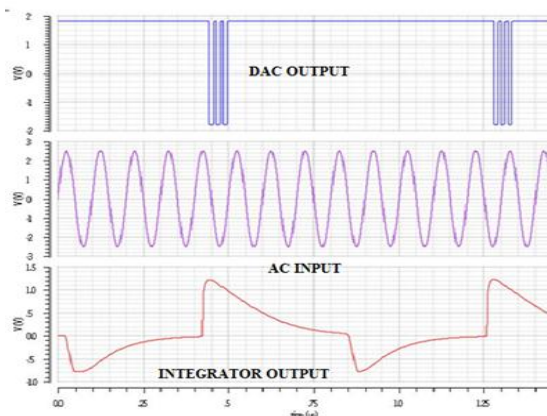The simulated waveforms for both circuits are in fig 12.

Fig 12: simulated waveforms for DAC and integrator.

3.3. Complete circuit of Sigma delta modulator.

The complete schematic of the sigma delta modulator is shown in fig 13 and the corresponding waveforms are shown in fig 13.
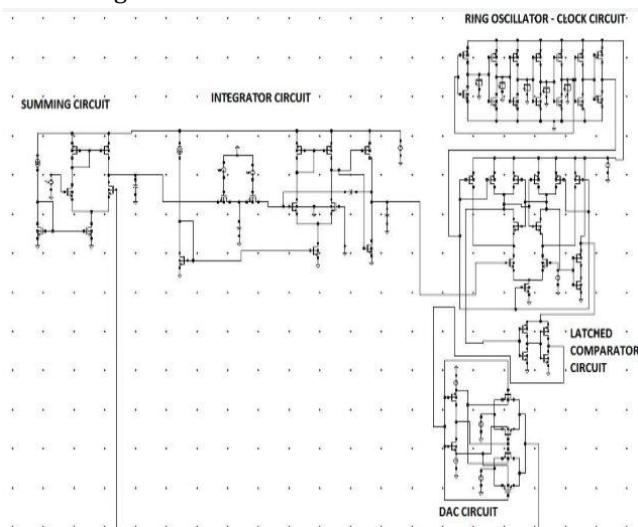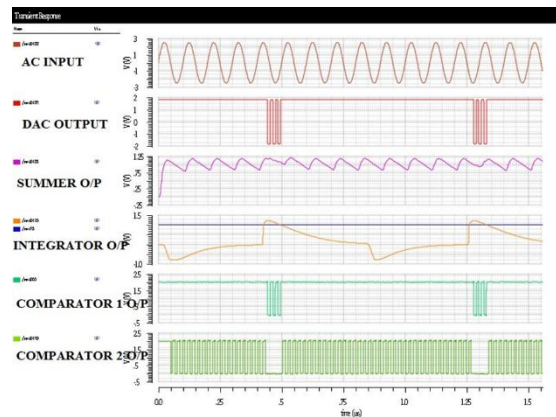

Fig 13: Complete sigma delta modulation circuit.

Fig 14: Waveforms of complete $\Sigma\Delta$ modulation.

4. CONCLUSION

In this work, the Sigma-Delta Modulator is designed and simulated with Switched Capacitor architecture. The incoming analog signal of frequency 1 KHz is encoded into digital pulses of 1.2 MHz frequency, thus high oversampling is achieved. In the integrator a resistor of 1K ohms is replaced by Switched capacitor of 20pF. The Digital to Analog Converter is used in the feedback loop to convert back the digital output into an analog signal and gets added with the incoming analog signal to reduce the delta noise. Thus the high oversampling ratio is achieved using the Sigma-Delta Modulator.

5. FUTURE SCOPE

The layout of the Sigma-Delta Modulator can be done using the Cadence Virtuoso Tool and it can be fabricated. The input can be given from an MEMS sensor. The output of the modulator can be processed using various digital processing techniques which help us to understand the signal better. The Sigma-Delta Modulator designed and simulated is of the first order, as it has only one feedback loop. As the order of the modulator increases the noise decreases (SNR increases). Thus increasing the number of integrators we can achieve higher orders of Sigma-Delta Modulators.

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