A REVIEW IN DESIGNING OF ADDERS USING SUBMICRON TECHNOLOGY

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Abstract - *A method proposed in this is is to design carry look ahead adders using SCMOS technology, also analyze the effect of various parameters on the characteristics of adders, using 50 nm, spice model for CMOS technology. The design was implemented for 16 bit and then extended for 32 bit also. Here parameters are computed and response curves are computed between all characteristics, DC and transient characteristics. The design and simulations are carried out to achieve these values approximately. Design will be carried out in either Electric CAD or Xilinx. Simulation results are verified using Modelsim and LTSpice. The DRC, LVS/NCC, transient checks are performed in the proposed design. Noise analysis is also done. In comparison with the existing full adder designs, the present implementation will offer significant improvement in terms of frequency.*

Key Words: CMOS Circuit, C5 Process, Full adder, carry look ahead adder, transient analysis

1.INTRODUCTION

A carry-look ahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits[1]. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The Kogge-Stone adder and Brent-Kung adder are examples of this type of adder.

A ripple-carry adder works in the same way as pencil-and-paper methods of addition. Starting at the rightmost (least significant) digit position, the two corresponding digits are added and a result obtained. It is also possible that there may be a carry out of this digit position (for example, in pencil-and-paper methods, "9+5=4, carry 1"). Accordingly all digit positions other than the rightmost need to take into account the possibility of having to add an extra 1, from a

carry that has come in from the next position to the right. The advantages of standard complementary (CMOS) style-based adders with twenty eight transistors are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and

requirement of buffers. Full adders are one of the most fundamental building block for circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart.

1.1 Full Adder

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The advantages of standard complementary (CMOS) style-based adders with twenty eight transistors are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count but the maximum carry Propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing thirty two transistors.
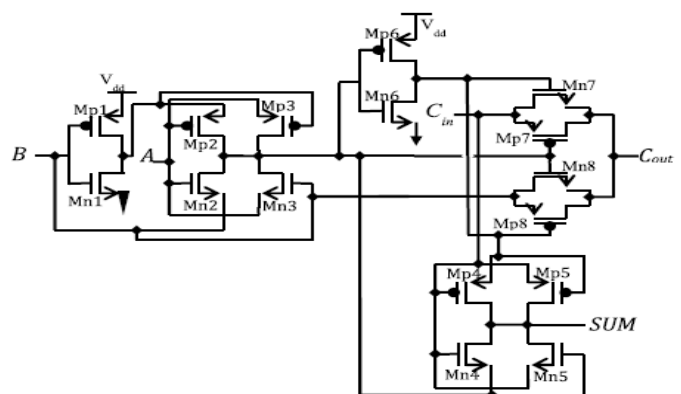

Figure 1 Full Adder[1]

2. Literature Review

Basant Kumar Mohanty and Sujit Kumar Patel in their paper entitled "Area–Delay–Power Efficient Carry-Select Adder" explained the logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to study the data dependence and to identify redundant logic operations. They have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation of *final-sum*, which is different from the conventional approach. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT) CSLA.

Yu Pan and Pramod Kumar Meher in their paper entitled "Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation" explained the Multiple constant multiplication (MCM) scheme is widely used for implementing transposed direct-form FIR filters. While the research focus of MCM has been on more effective common subexpression elimination, the optimization of adder trees, which sum up the computed sub-expressions for each coefficient, is largely omitted. In this paper, we have identified the resource minimization problem in the scheduling of adder-tree operations for theMCMblock, and presented amixed integer programming (MIP) based algorithm for more efficient MCM-based implementation of FIR filters.

Ahmed M. Shams, arek K. Darwish, and Magdy A. Bayoumi in their paper entitled "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells"explained the performance analysis of 1-bit full-adder cell is presented. The adder cell is anatomized into smaller modules. The modules are studied and evaluated extensively. Several designs of each of them are developed, prototyped, simulated and analyzed. Two realistic circuit structures that include adder cells are used for simulation. A library of full-adder cells is developed and presented to the circuit designers to pick the full-adder cell that satisfies their specific applications.

Chiou-Kou Tung, Yu-Cherng Hung, Shao-HuiShieh, and Guo-Shing Huang in their paper entitled" A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System " explained the low-power high-speed CMOS full adder core is proposed for embedded system. Based on a new three-input exclusive OR (3-XOR) design, the new hybrid full adder is composed of pass-transistor logic and static CMOS logic. The main design objectives for the full adder core are providing not only low power and high speed but also with driving capability. The circuit is proven to have the minimum power consumption and the fastest response of carry out signal among the adders selected for comparison. Due to the low-power and high-speed properties, both the new exclusive OR circuit and the new full adder can be efficiently integrated in a system-on-a-chip (SoC) or an embedded system.

K. N. Bhargav, A. Suresh, GauravSaini in their paper entitled "Stacked Keeper with Body Bias: A New Approach to Reduce Leakage Power for Low Power VLSI Design" explained technique named as stacked keeper with body bias (SK-BB). It uses stack effect to existing sleepy keeper technique along with body bias for ultra low static power consumption. A 4-bit CMOS adder circuit is designed using existing techniques like sleep, zig-zag, sleepy-stack, dual stack, sleepy-keeper and proposed techniques SK-BB and SK-BB with High Vth (SK-BBH). The dynamic power of SK-BB and SK-BBH are 1% more and 9% less than sleepy keeper approach. However, the delay of the SK-BB and SK-BBH increases by 59% and 4% than sleepy keeper.

3. TECHNOLOGY USED

This non silicided CMOS process has 3 Metal layers and two poly layers and a high resistance layer. Stack contact are supported. The process is for 5V applications.
FEATURES
- 2 or 3 metal layers
- Poly to poly capacitors
- High voltage I/O – 12/20 V
- High-resistance poly
- Low-voltage modules

4. DESIGN PROCEDURE

Defining the requirements and setting the specifications. Design according to the Tool flow (EDA based). Design of the Test circuits. Simulating the Test results and optimization of the parameters.

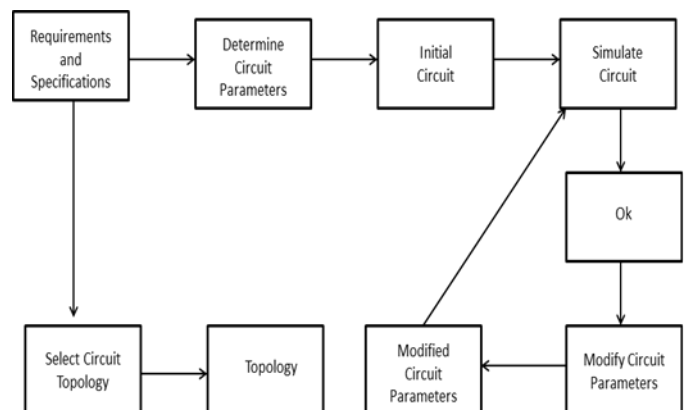Following is the flow graph that illustrates the design of mixed analog integrated circuits.

Figure 2 Design Flow

5. ADDER DESIGNS USING VARIOUS TECHNOLOGIES

There are numerous topologies and designs exist in literature. Few of them are as follows
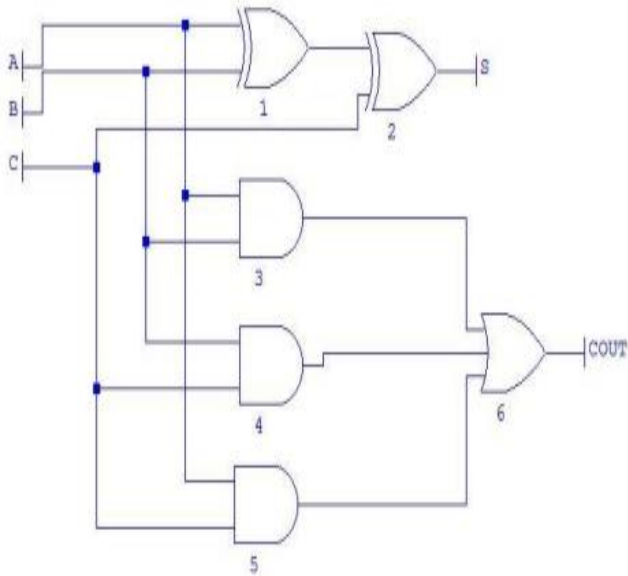

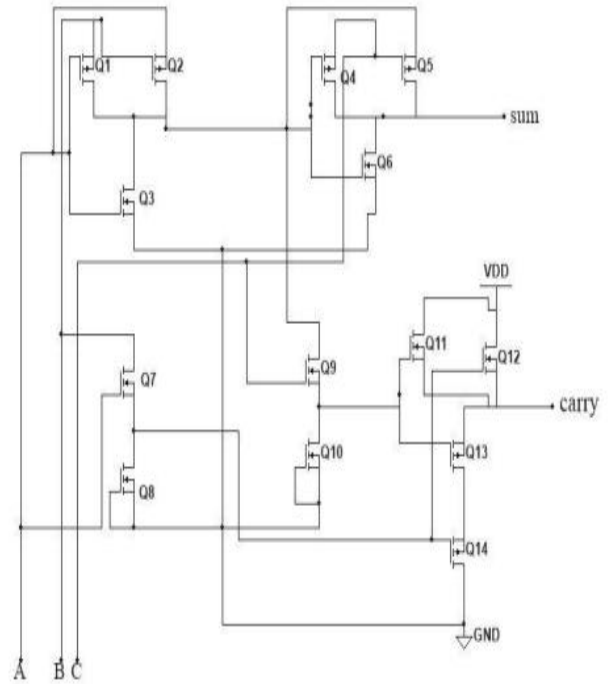Figure 3 Gated design for Adder Circuits

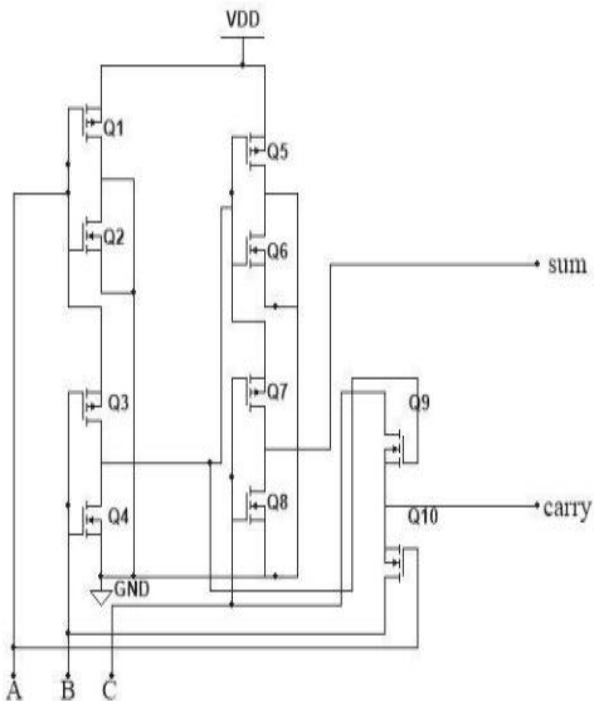Figure 5 14T transistor Adder circuit

Figure 4 Schematic for SERF Adder

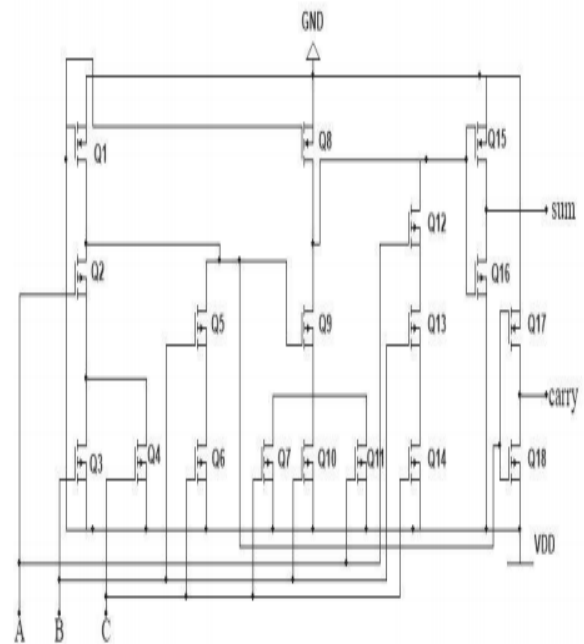

Figure 6 Pseudo nMOS Adder Circuit
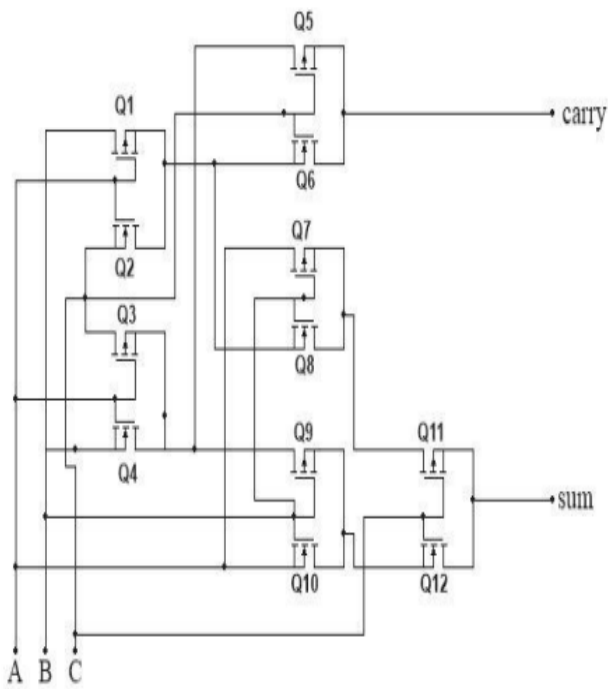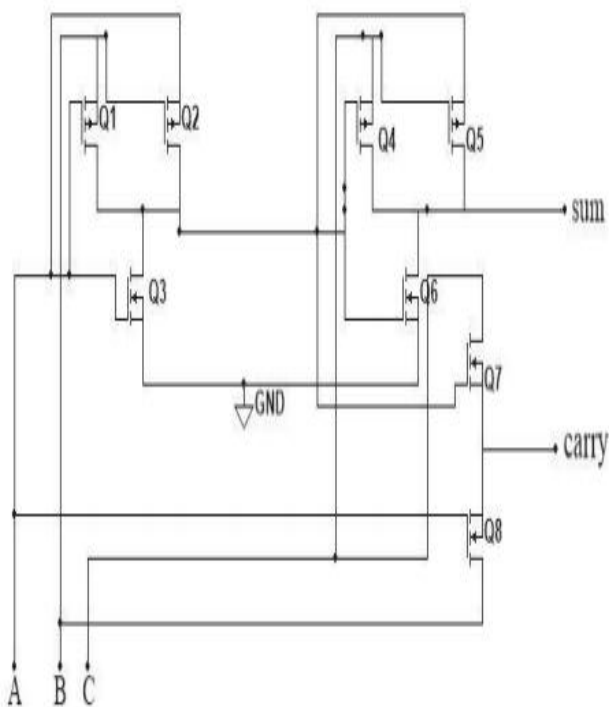
Figure 7 Multiplexer based Adder circuit design

Figure 9 Inverter and Transmission Gate based adder design

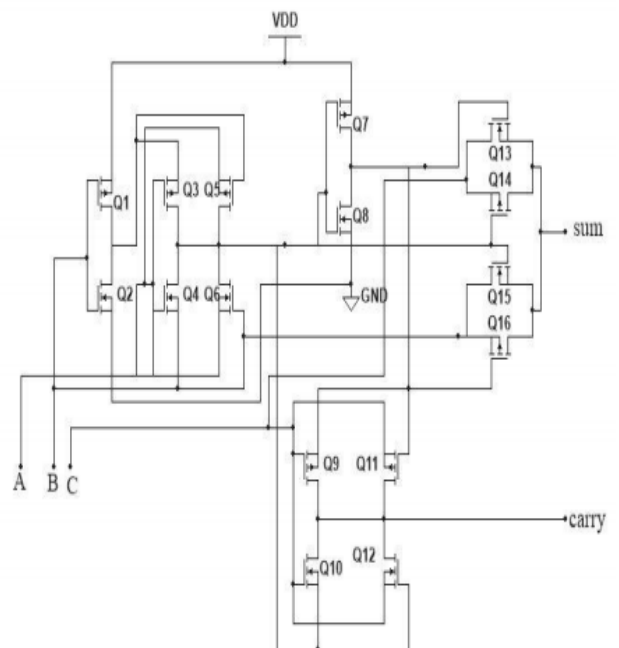

Figure 8 8T Adder circuit design

Figure 10 Hybrid Adder circuit design

6. Comparison of various adders based on their delay analysis and associated process technologies

The performance analysis of several full adders drawn in table- 1 shows different adders with different parameter values and different technology, no single adder have less delay,. thus, there exist tradeoff between these parameters. the results are helpful in selection of an adder according to desired result and application.

Table 1

Comparison Table of Various adder circuits on the basic of delays and associated process technologies

Design Name	Process Technology	Delay (in ns)
6 Transistor	350 nm	0.133 ns
8 Transistor	150 nm	0.010 ns
9 Transistor	120 nm	0.295 ns
10 Transistor	180 nm	1.057 ns
12 Transistor	350 nm	0.217 ns
14 Transistor	180 nm	0.338 ns
20 Transistor	180 nm	0.250 ns
Pseudo NMOS	180 nm	0.182 ns
CMOS	180 nm	0.127 ns

A kind of activity which uses a computer to assist on the creation, modification and analysis of design. CAD tools generally consist of the following components, input handler (input from mouse or keyboard), data structure and algorithms (in memory), output handler (output to display). CAD environment generally consists of a simulator, design space exploration and design sign off.

The front end tools are used for design entry editors, simulation synthesis and timing analysis and test generation tools. The back end tools include floor planning place and route, extraction etc. Editors ,simulators, analyzers and synthesizers together contributes in computer oriented design.

7. Conclusion

Keeping in view different applications the carry look ahead adder design has been proposed. For this first a selection is made for the active device used. The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to

redesign the circuit for various set of specifications. The responses are simulated using LTSpice and Electric VLSI CAD design tool. The simulated results of the carry look ahead adder will be in compliance with the theoretical values.

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