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A New design Approach to Synchronous 8 bit counter

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Abstract - *This paper introduces a new design approach to the Synchronous 8-bit counter, which reduces the area, a cost effective factor. In this paper a Synchronous 8 bit counter using Edge Triggered D flip flop is designed and Area comparison is made with our new Design in terms of number of slices occupied.*

Design is Implemented in XilinX9.1 using Structural code Verilog and finally. Synthesized on Vertex5 FPGA.

***Key Words*: D flip flop, 8 bit counter, vertex 5.**

1. INTRODUCTION

Counting plays a vital role in the digital logic. It is a Sequential circuit, Collection memory elements like flip-flop, which change it states in a certain sequence .These are also called Pattern generator which changes it states with occurrence of events [2].

Counter has mainly two parts Combinational logic, implemented using logic gates to satisfy the basic rule of counting and, memory bocks, implemented using flip-flops. The basic rule of a counter is the bit toggles only when all least significant bits are 1.Memory block, Flip-flop can be in either of two states i.e., 1 or 0 and it gives its State as output [5].

Various types of Counters are there which comes under two groups Asynchronous and Synchronous. In Synchronous type all the flip-flops changes states simultaneously, while in Asynchronous type flip flop changes it states only when preceded flip-flop change its state. In this paper

Depending on States of memory elements, counter name changes i.e., MOD-n counter if it has n states. A group of Flip-flops also acts as register also [5], found place in applications like digital memories.

Applications of a counter in the digital consumer electronics market are tremendous, you can find from a simple display to complex microcontroller circuits, Com. Some applications are: frequency divider in phase-locked loops, signal generation, frequency synthesizers and, processing circuits, Microcontrollers, digital memories and in digital clock and timing circuits [4].

Area is a Cost effective factor, which sets the need to decrease it. In this paper we tried to reduce the area consumed by the counter, with new design. In Section 2, General 8 bit synchronous counter using Positive edge triggered D flip-flop is introduced and the schematic layout is presented. In section 3, our newly designed 8 bit counter is introduced and the schematic layout is presented. In Section 4, Area comparison is made from simulation results, are given and finally conclusion will be made in the last.

as output pin assert to Vcc if single master, for slave acts as input pin grounded to 0 if single slave. LSBFE-This bit decides which bit to shift either LSB (least significant bit) or MSB (most significant bit) to shift.

2. SYNCHRONOUS COUNTER [2]

Synchronous counter is a fastest counter which reduces propagation delay by changing all

Outputs simultaneously under control of Clock, thus became more popular and preferable than Asynchronous.

Synchronous 8 bit up counters which counts from 000, 001 … up to 111 and becomes 000 again, by resulting overflow pulse. Generally counter consists Combination logic part and Sequential part. Sequential is implemented by positive edge triggered D flip-flop and Logic gates works for combinational logic which reduces cost for counter.

Logic gates are simple logic circuits having two or more inputs and produces output

Either 1 or 0. E-Xor, AND gates are used to implement combinational logic part. A master slave Edge triggered D-flip flop has use which reduces glitches [7] & [6].

2.1. Alternative design of Master Slave D flip flop [1]

Positive Edge triggered D flip-Flop using three SR latches changes its output states for every rising edge which reduces glitches whereas level triggered flip-flop don't[7]&[6].

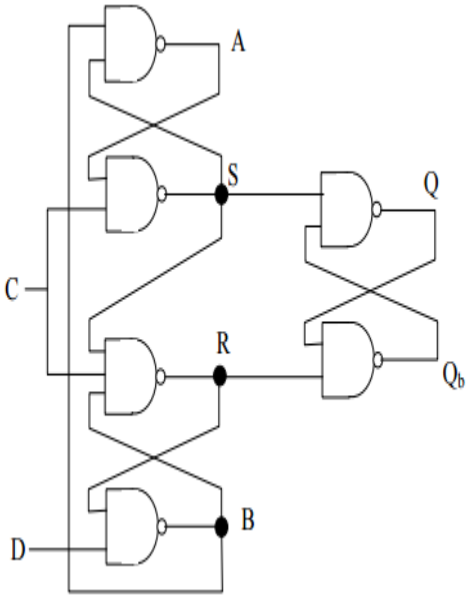

Figure 1. Traditional positive edge triggered D flipflop

Above circuit have three SR latches, each SR latch sets and rests its output to 1 or 0. Above circuit works as follows,

- When C=0, S and R high, keeps Q, Qb impact. At the same time B = ~D and A=D
- Now C transist from 0 to 1, the value of A and B passes through S, R, finally appear D as output.

Since it ignores changes in D when C=1(after rising edge), it acts as positive triggered D flip-flop.

2.2 Synchronous 8 bit up counter

This Synchronous up counter counts from 0 to 255, has 8 E-Xor gate, a 8 AND gates and, 8 Positive edge triggered D flip-flop's. Exor gates , AND gates combindly satisfy the basic principle of a counter and D flip-flop latches the outputs from combinational part on rising edge of a clock. As you can observe in the figure , it have asynchronous load_bar and count input through the MUX to load parallelly as shown in figure below .

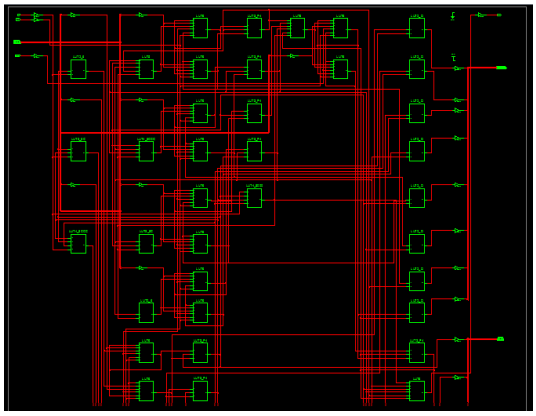

Figure 2. Shows Schematic view of general counter module

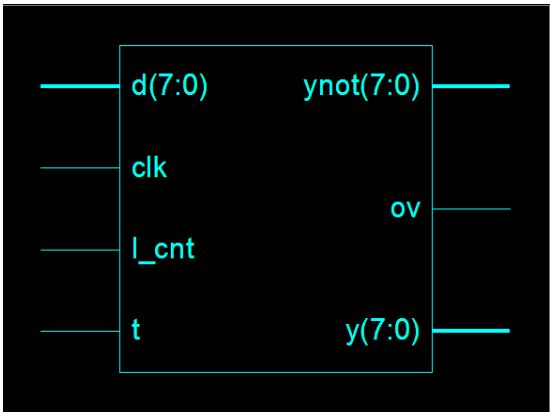

Figure 3. Shows RTL view of general 8-bit counter design

3. NEW DESIGN

As we know D flip-flop acts as a sequential part in the counter, in our new approach, a Mux acts as D latch used instead of D flip-flop which consumes less area than D latch. By using this newly designed latch in many places of Counter, reduces Counter area as well.

Since D flip-flop is edge triggered, an edge triggered circuit is used along with MUX in order to work as Edge triggered D latch. It has Asynchronous clear, which can be achieved by passing clear and input to Mux through OR gate.

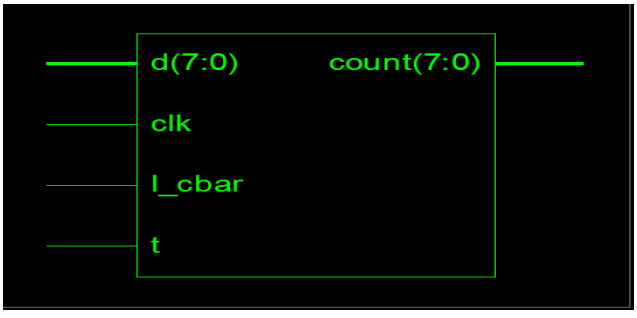

Figure 4. Shows RTL view of new counter.

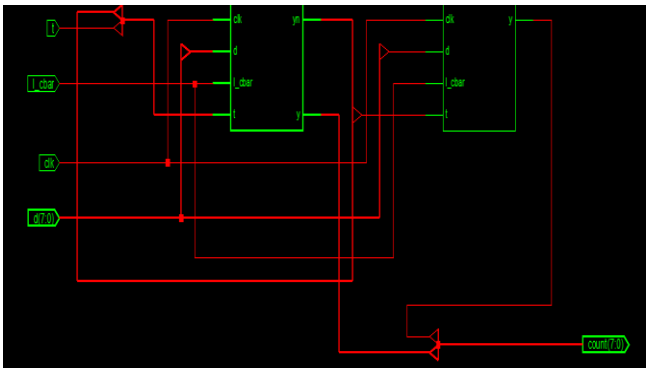

Figure 5. Shows Schematic view of new counter.

4. AREA ANALYSIS

In this section, synthesis results are presented .the main objective of the paper is Area optimization, below table shows area consumed by two counters.

Table1: Synthesis results on Vertex 5 xc5vlx30-3ff324.

comparison	Previous design	New design	Available
Number of slices fully occupied	0 out of 17	0 out of 8	-
Number of LUT's	42	8	19200
Number of Bounded IOB's	28	17	220

5. CONCLUSION:

This new design has consumed less area than previous design. Synthesis results on Vetex5 FPGA shows reduction of area in terms of LUT's. Since area is Cost effective factor and counter has place in almost every digital circuits, this new design plays vital role in coming days.

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