POWER EFFICIENT SRAM CELL USING T-NBLV TECHNIQUE

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Abstract -*SRAM (Static Random Access Memory) fulfills two needs of electronic industry. The first one is the provision of direct interface with the CPU at speeds not attainable by DRAMs and the second one is the replacement of DRAMs in systems that requires very low power consumption. SRAM cells are extremely small device which makes them highly sensitive to process variations in nanoscale CMOS technologies. The random changes in the device characteristics may leads to read and write failures in SRAM cell. This works presents the implementation of UDVS (Ultra Dynamic Voltage Scaling) and Transient Negative Bit Line Voltage (T-NBLV) techniques in SRAM cell and a performance comparison of both in terms of power and delay. The design is implemented using TANNER tool in 90nm technology and the performance is analysed based on the simulation results. The result shows better performance for T-NBLV SRAM compared to UDVS SRAM.*

KEYWORDS – SRAM, PMOS, NMOS, TFT, *Tran-NBL, NBLV, U-DVS*

1. INTRODUCTION

Static Random Access Memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The speed advantage of SRAM over another memories resulted in wide range of high speed applications in electronic industry. There are currently 3 types of SRAM cells namely 4 transistor SRAM (4T), 6 transistor SRAM (6T) and thin film transistor SRAM (TFT). SRAM cell usually consumes more area in integrated circuit fabrication. So reducing power consumption in SRAM cell is an important design criterion for the efficient performance of a SRAM occupied system. Different approaches can be used for reducing the power consumption of SRAM. UDVS (Ultra Dynamic Voltage Scaling and Transient Negative Bit Line Voltage (T-NBLV) approaches are best techniques for the reduction of power consumption in SRAM.

This works intended to evaluate the performance efficiency of UDVS and T-NBLV approaches for reducing power consumption in 6T SRAM cell. The 6T SRAM is designed by using both approaches in tanner tool. The parameter comparison is done based on the simulation results.

The rest of this paper is organized as follows. Section 2 presents 6T SRAM design. Section 3 describes 6T SRAM using UDVS technique. Section 4 includes T-NBLV based SRAM design. Section 5 involves results and discussions as well as simulated waveforms and finally concluded in Section 6.

2. 6T SRAM CELL

As the name implies 6T SRAM cell consists of six transistors out of which four transistors act as back to back inverters and remaining two are access transistors as shown in figure 1. In inverter configuration two are NMOS and two are PMOS transistors. The pull up section consists of PMOS and pull down section include NMOS transistors. Pull up and pull down section build two inverters and they can be accessed by two access transistors [1].

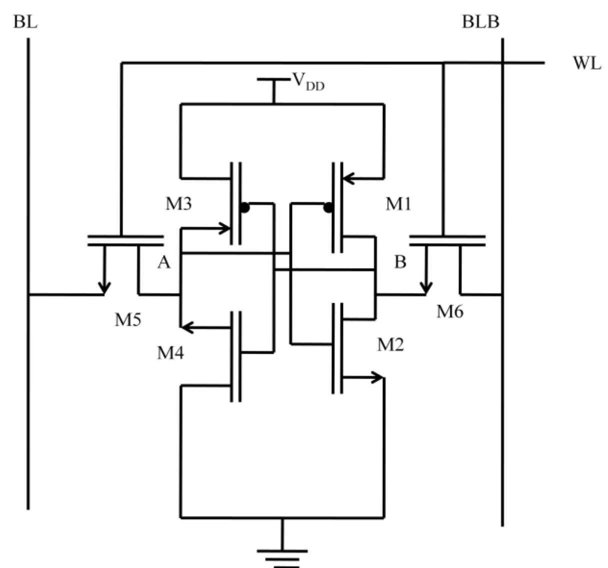


Fig-1: Basic 6T SRAM Cell

The read and write operations can be controlled by using access transistors. The access transistors are under the control of word lines. If WL is low transistor can holds the data and if WL is high it can perform read and write operations. The write operation makes the WL value high and it activates the access transistors. The

new data can be applied through Bit and Bit-Bar lines. Data in the flip-flop/latch circuit is over written with New Value during the write operation [2].

3. SRAM USING UDVS TECHNIQUE

The UDVS based 6T SRAM cell is shown in figure 2. It is a combination of UDVS circuit, write circuit, SRAM cell and Read circuit. The write driver circuitry can be used to read the appropriate data values to the bit line. The write driver circuitry is shown in figure 3. The connection of four vertical devices in series can be referred as a gated inverter. In write driver circuitry the transistors are similar sized.

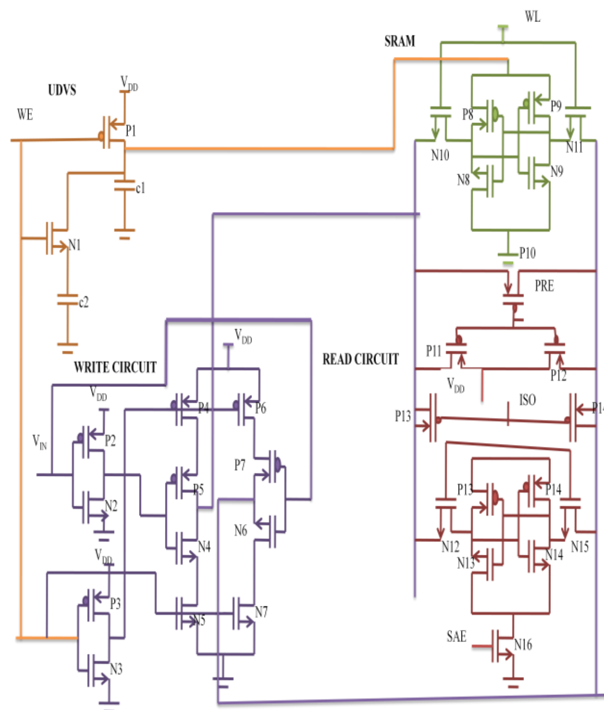


Fig-2: U-DVS based 6T SRAM cell

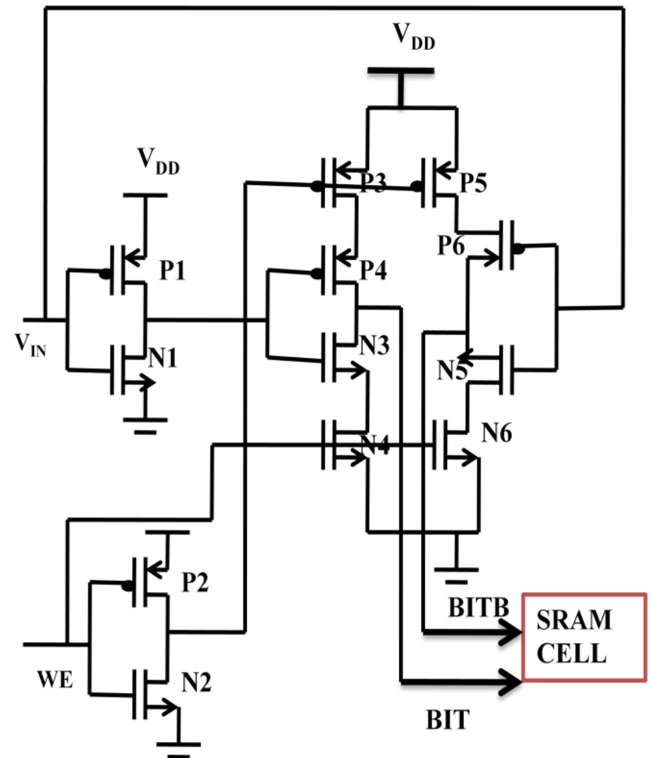
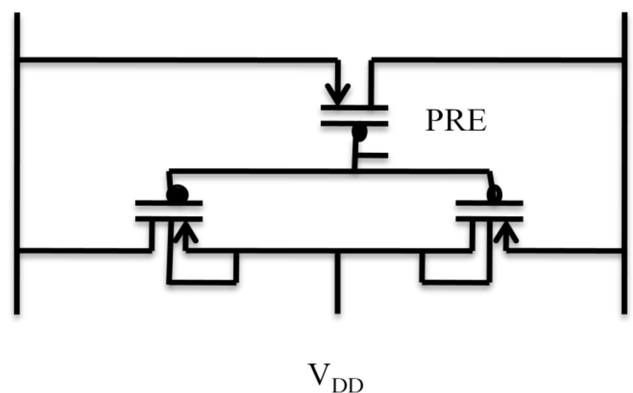


Fig-3: Write Driver Circuit

The read circuit is used to read the data from SRAM cell. Read circuit is combination of pre-charge circuit, isolation circuit and sense amplifier. The main part of the read circuitry is the precharge circuit which is shown in figure 4. The two transistors can be used to pre-charge the bit lines and the remaining transistor can be used to avoid the capacitive coupling between the bit lines.



V_{DD}

Fig-4: Pre-Charge Circuit

The PMOS transistors in the precharge circuitry are connected to VDD through drain terminal and are connected to the bit lines through source terminal. The connection helps to maintain precharge voltage V_{DD} at the bit lines. In read operation any one of the bit line discharges via the node storing '0' and at the same time

other bit line maintains V_{DD}. This develops a differential voltage between the bit lines.

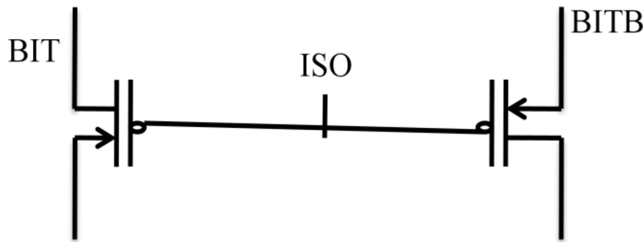


Fig-5: Isolation Circuit

Isolation circuit is a two PMOS transistor circuit. The PMOS transistor helps to achieve connection between bit line and the sense amplifier and is shown in figure 5. After maintaining particular voltage difference between the two bit lines, isolation circuit isolates the SRAM cell and Sense Amplifier [4].

Sense amplifiers place a major role in SRAM cell read operation. The sense amplifier is shown in figure 6. It reduces the overall SRAM chip Delay and Power Consumption. In READ operation lower voltage swing may occur. Sense amplifier can amplify the voltage coming from bit lines [3].

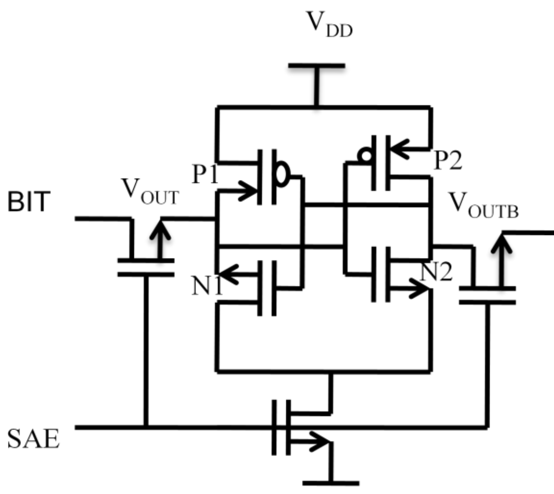


Fig-6: Sense Amplifier

4. SRAM USING T-NBLV TECHNIQUE

The transient negative bit line voltage (T-NBLV) approach is a write assist technique. It can make the write operation faster. This technique applies negative voltage to pass transistor terminal when WL is high. The negative voltage and the gate voltage increase the channel band width between the sources and drain terminal of the pass transistor. The increased channel width makes the write operation easier [7].

$$I_D=\mu C_{OX}W/L\ (V_{gs}-V_{th})^2$$

Here $V_{gs}=V_g-V_s$

If the source voltage is negative

$$V_{gs}= V_g-(-V_s)$$
$$= V_g+V_s$$

As V_{gs} increases, Id also increases which leads to more channel width.

The 6T SRAM cell write and read circuit using transient negative bit line scheme is shown in figure 6. The circuit consist of write as well as read circuitry. Write circuitry makes use of two capacitors for implementing coupling. Capacitors are connected in series and one end of the capacitor is connected to Bit and BitB and other end is connected to BIT-EN (BE).

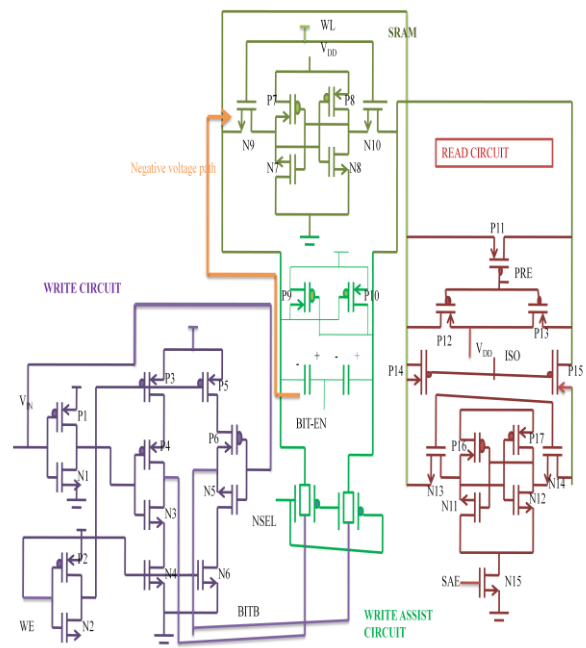


Fig-7: Tran-NBL 6T SRAM cell

If the BIT-EN is low then the capacitive coupling will generates negative voltage, then one end of capacitor is '0' and other end maintains V_{DD}. Because of slow discharge of capacitor if the positive terminal is '0', then negative terminal will be high at least for some time. The high value of WL voltage and gate to source voltage makes more width to access transistor channel. If channel width is more data will be easily passes into the SRAM cell. This improves the write operation efficiency of SRAM cell [6] [7].

5. RESULTS & DISCUSSIONS

The design is implemented using tanner tool in 90nm technology. The output waveforms for simple 6T SRAM, UDVS SRAM and T-NBLV SRAM is shown in figure

8, 9 and 10 respectively. Table 1 shows the comparative analysis of UDVS and T-NBLV techniques in terms of certain number of parameters.

Sl. No.	Parameter	SRAM Using UDVS	SRAM Using T-NBLV
1.	Avg. power(mw)	2.61	0.24
2.	Delay(ns)	1.57 X10^{-2}	8.68 X10^{-4}
3.	Memory(Kbytes)	338	197
4.	CPU time(sec)	47	42

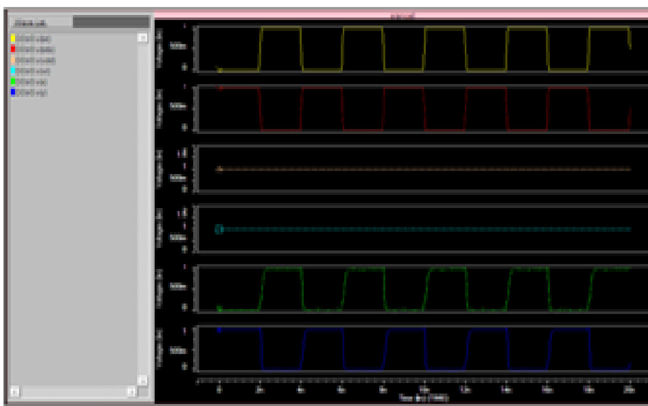


Fig -8: Output waveform for Basic 6T SRAM Cell

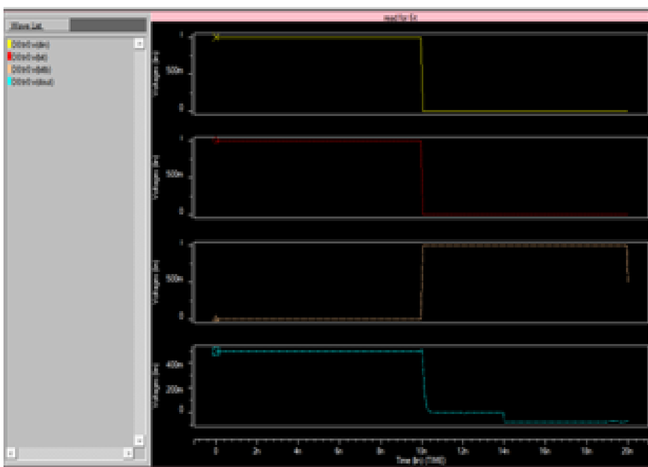


Fig-9: Output Waveform for UDVS based 6T SRAM Cell

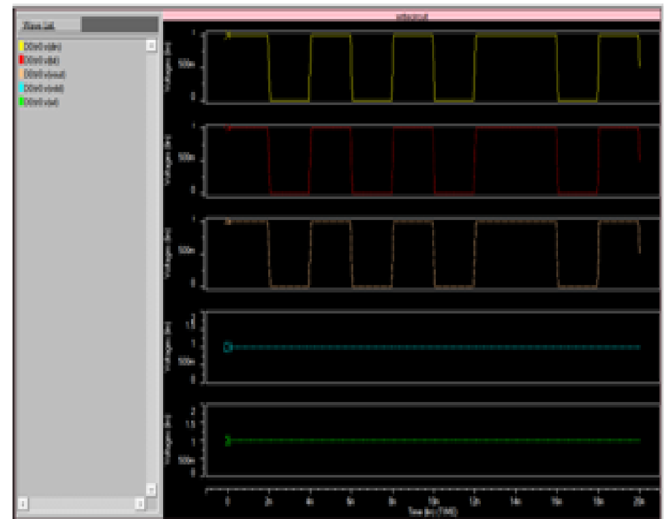


Fig-10: Output Waveforms for T-NBLV 6T SRAM Cell

Table-1: Comparative Analysis

6. CONCLUSION

An efficient 6T SRAM cell is developed using Transient Negative Bit line voltage (T-NBLV) technique. The design is implemented in tanner tool with 90nm technology. The evaluated simulation parameters are compared with the SRAM implemented using ultra Dynamic Voltage Scaling (UDVS) technique. The obtained results shows that the SRAM implemented using Tran- negative bit line voltage (T-NBLV) technique gives better results as compared to SRAM implemented using UDVS technique.

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