

Aging Effect Tolerant Multi-precision Multiplier

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Abstract -Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias ($V_{gs} = -V_{dd}$), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. The experimental results show that our proposed architecture with 32×32 and 64×64 column-bypassing multipliers can attain up to 62% and 65% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column-bypassing multipliers. Furthermore, our proposed architecture with 32×32 and 64×64 row-bypassing multipliers can achieve up to 70% and 69% performance improvement as compared with 32×32 and 64×64 fixed-latency row-bypassing multipliers.

Key Words: Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

1. INTRODUCTION

DIGITAL multipliers are the most commonly used arithmetic functional units in many applications. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance will be reduced. Furthermore, when a pMOS transistor is under negative bias ($V_{gs} = -V_{dd}$), the negative bias temperature

instability (NBTI) occurs. During this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaks the Si-H bond generated during the oxidation process, by generating H or H₂ molecules. Because of diffusion interface traps are left. The accumulated interface traps increases threshold voltage (V_{th}), which reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs reducing the NBTI effect. But the reverse reaction does not eliminate all the interface traps generated during the stress phase, and V_{th} is increased in the long term. Hence, it is important to design a reliable high-performance multiplier. The nMOS transistor is under positive bias, positive bias temperature instability (PBTI) undergoes with similar effect to that of pMOS. To avoid these problem, many NBTI-aware methodologies have been proposed. An NBTI-aware technology [7] mapping technique was proposed to guarantee the performance of the circuit during its lifetime. An NBTI-aware sleep transistor [8] was designed to reduce the aging effects on pMOS sleep-transistors and the lifetime stability of the power-gated circuits under consideration was improved. These techniques, however, require circuit modification or do not provide optimization of specific circuits. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. This will result in significant timing waste. Hence, the variable-latency design was proposed to reduce the timing waste.

1.1 Design and Implementation

1.1.1 Adoptive hold logic Model

The adoptive hold logic circuit associated with an aging aware indicator, two blocks for judging, one multiplexer, and another for D flip-flop. The aging aware indicator indicates whether the circuit has been suffered by significant performance degradation because of the aging effect. Simple counter is implemented as the aging aware indicator in that, number of error were counted over a certain amount of operations which hadn't met the deadline and is reset to '0' at the end of those operations. If the cycle period is too short, these operations cannot be completed successfully by the column or row-bypassing

multiplier, causing timing violations of the operations. The Razor flip-flops find these timing violations, and generate error signals. If errors occurs frequently and exceed a threshold which is predefined, it means that the circuit has affected by significant timing degradation due to the aging effect or violation of deadline, and the aging aware indicator will output signal '1' or

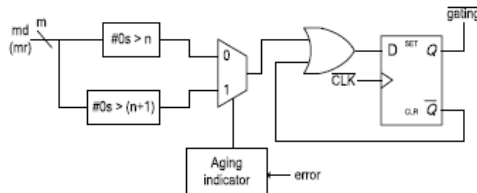


Fig 1: Diagram of ADOPTIVE HOLD LOGIC

Otherwise '0'. To indicate the Deadline violation effect is still not significant and no actions are needed. If the number of zeros in the multiplicand (multiplier) for the row-bypassing multiplier is larger than n then the first judging block in the adoptive hold logic circuit will output 1, and if the number of zeros in the multiplicand (multiplier) is larger than $(n + 1)$ then the second judging block in the adoptive hold logic circuit will output 1. Both blocks are employed to decide, whether an input pattern requires two or one cycles, but they choose only one block at a time. In the earlier, the Deadline violation effect is not significant and the aging aware indicator produces 0. So the first judging block is used. After some period of time when the Deadline violation effect becomes significant instead of choosing first judging block the second judging block will be chosen. Comparison between the first judging block and the second judging block allows a smaller number of patterns which are accommodated/employed in one-cycle patterns since it provided with more zeros in the multiplicand (multiplier). The detailed operation of the adoptive hold logic circuits as follows: when arrival of an input pattern occurs, first judging blocks and second judging block will decide whether the arrived input pattern requires one cycle or two cycles to complete the operation. Both results are passing to the multiplexer.

Either the result was selected based on output of the aging aware indicator by the multiplexer. Then, both the result of the multiplexer an OR operation performed and the Q signal is used to determine D flip-flop input. When the pattern requires one cycle, the output of the multiplexer is 1. If the $!(gating)$ signal will become 1, the input flip flops will latch new data in the next cycle. On the other hand, the output of the multiplexer is 0, that means to complete the input pattern requires two cycles and the OR gate will output 0 to the D flip-flop. Therefore, to disable the clock signal of the input flip-flops in the next cycle, the $!(gating)$ signal will be 0. Note that only a cycle

of the input flip-flop will be disabled since the D flip-flop will latch 1 in the next cycle.

The overall flow of the proposed architecture is as explained below: when input patterns arrive, the Adoptive hold logic circuit and the column/row-bypassing multiplier execute simultaneously. Depending on the number of zeros in the multiplicand (multiplier), the Adoptive hold logic circuit decides whether the input patterns require one or two cycles. In case if the input pattern requires two cycles to complete, the adoptive hold logic will output 0 to disable the clock signal of the flip-flops. Otherwise, the adoptive hold logic will output 1, for normal operations. When the operation finished by the column/row-bypassing multiplier, that the result will be passed to the Razor flip-flops. As there is the path delay timing violation checked by the Razor flip-flops. If the timing violations occur, it means that the cycle period is not sufficient enough for the current operation to complete the operation, the execution result of the multiplier is incorrect due to aging effect. These operations are monitored by the Razor flip-flops and it will output an error to inform the system that the current operation needs to be re-executed using two cycles to ensure the operation is correct. In these situations, the extra re-execution cycles caused by timing violation incurs a penalty to overall average latency of the operations. However, in this proposed adoptive hold logic circuit can accurately predict whether the input patterns require one or two cycles. Only a few input patterns may cause a timing variation of the operation, when the adoptive hold logic circuit judges incorrectly. In this case, significant timing degradation did not produce the extra re-execution cycles.

2. Column-Bypassing Multiplier

The multiplier array consists of $(n-1)$ rows of carry save adder (CSA) for faster and smarter addition to save timing degradation, in which each row contains $(n - 1)$ full adder (FA) cells for addition. Each Full Adder in the Carry Save Adder array has two outputs i.e. the sum bit goes down and the carry bit of present addition goes to the lower left Full Adder. For carry propagation, the last row is implemented as ripple adder. The Full Adders in the Array Multiplier are always active regardless of input states and thus consumes more power. In this proposed low-power column-bypassing multiplier design, in which the Full Adder operations are disabled if the corresponding bit in the multiplicand having 0. Fig.1.2 shows a 4×4 column-bypassing multiplier. Suppose the inputs are 1010×1111 , it can be seen that for the Full Adders in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right Full Adder and the partial product $a_i b_j$. Hence the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit,

which is the sum output of its upper Full Adder. Therefore, the Full Adder is modified to add two tri-state gates and one multiplexer.

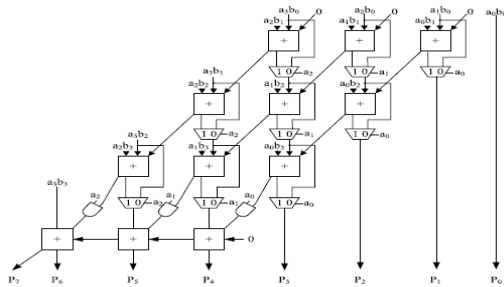


Fig. 2: 4 × 4 column-by-passing multiplier

The multiplicand bit a_i can be used as the selector of the multiplexer to decide the output of the FA, and a_i can also be used as the selector of the tri-state gate to turn off the input path of the FA. If a_i is 0, the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If a_i is 1, the normal sum result is selected.

3. Row-Bypassing Multiplier

A low-power row-bypassing multiplier [9] is also proposed to reduce the activity power of the AM. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing multiplier, but the selector of the multiplexers and the tri-state gates use the multiplier.

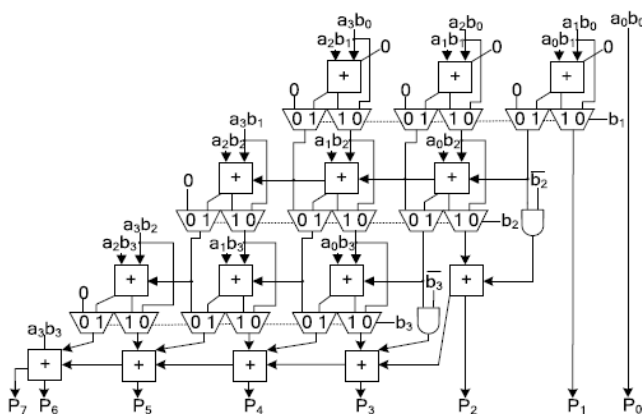


Fig. 3 : 4 × 4 Row-bypassing multiplier

Fig. 1.3 is a 4 × 4 row-bypassing multiplier as shown above. Through a tri-state gate, each input is connected to an Full Adders. When the inputs are 1111 × 1001, the two inputs in the first and second rows are 0 for Full Adders. Because b_1 is 0, the multiplexers in the first row select 0 as

the carry bit and select a_1b_0 as the sum bit. The inputs are bypassed to Full Adders in the second rows, and the input paths to the Full Adders are turned off by the tri-state gates. Therefore, there is no switching activities occur in the first-row Full Adders; as a result, power consumption is reduced. Similarly, no switching activities will occur in the second-row Full Adders, because b_2 is 0. However, because the b_3 is not zero, the Full Adders must be active in the third row.

4. Razor Flip Flop

A 1-bit Razor flip-flop contains a multiplexer, main flip-flop, XOR gate, and shadow latch. Execution result for the combination circuit using a normal clock signal caught by the main flip-flop and the execution result using a delayed clock signal caught by the shadow latch, having the clock which is slower than the normal clock signal. If both the latched bit of the shadow latch and the main flip-flop is different, this means the path delay of the current operation exceeds the cycle period which has assigned and the main flip-flop catches an incorrect result and causes an error.

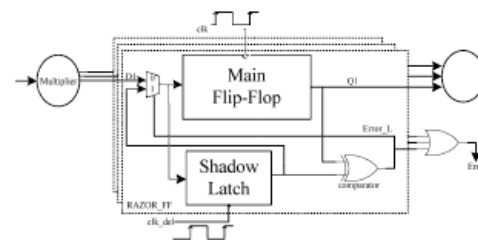


Fig. 4: Razor flip flops.

The Razor flip-flop will set the error signal to 1, If errors occurs to notify the system to re-execute the operation and notify the adoptive hold logic circuit that an error has occurred. In this proposed methodology Razor flip-flops are used to detect whether an operation i.e considered to be a one-cycle pattern can really finish in a given cycle. If not, the operation will re-execute with two cycles to complete the operation. Even though the re-execution may seems time consuming and costly provides the exact output. Since the re-execution frequency is low the overall cost is low.

5. RESULTS

The proposed paper is implemented, synthesized and simulated using Xilinx Synthesis Tools (ISE 14.7) targeted on Virtex 5 family.

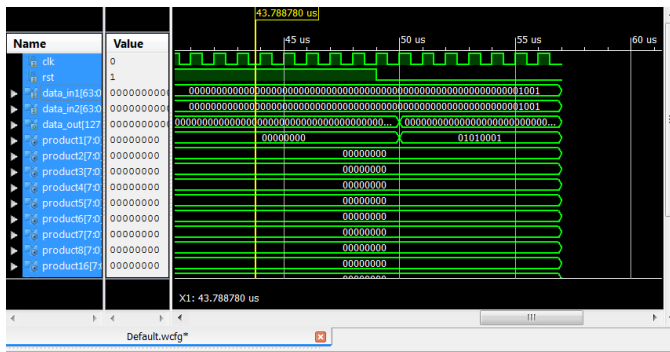


Fig. 5: simulation result of multiplier.

6. CONCLUSIONS

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that our proposed architecture with 4x4 multiplications with CLA as last stage instead of Normal RCA adder it will decrease the delay and improve the performance compared with previous designs.

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