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A Survey on Reversible Flip Flop

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Abstract - *Reversible logic has gained importance in recent times owing to the fact that power consumption in these circuits can be drastically reduced. In conventional digital circuits, a significant amount of energy is dissipated as the bits of information are lost during logical operations. This loss of bits of information can be avoided by using reversible logic gates. Flip flop is the building block of the sequential circuits. Since the output of a sequential circuit depends not only on the present inputs but also on the past input conditions, the construction of sequential element using reversible logic gates is quite complex than that of combinational circuits. This paper provides a survey of the reversible logic gates based flip flop.*

Key Words: Reversible logic, reversible gate, power dissipation, flip flop, garbage.

1. INTRODUCTION

Reversible logic gates - Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. Also in the synthesis of reversible circuits direct fanout is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

Flip Flop - A flip flop can store one bit of information. Flip flop changes their content only either at rising or falling edge of clock signal.

There are basically four main types of flip flops-

1. SR flip flop
2. D flip flop
3. JK flip flop
4. T flip flop

The major differences between these flip flops are the number of inputs they have and how they change state.

Very little previous research has been done on designing sequential circuits using reversible logic. Synthesis of sequential circuits is very difficult from combinational circuits. The difficulty arises from the fact that sequential circuits require a feedback from one of the outputs and reversible logic gates do not allow a fan-out of more than one.

Here as flip flop will be designed using reversible logic, which can be used to construct sequential circuits.

2. LITERATURE REVIEW

In this section, detailed literature review is done that aims to review the critical points of current works. Here the information collected about researches and innovations carried out on the related technologies have been done. This section will highlight the recent trends and innovations in the concerned technology.

Gordon. E. Moore [1] in 1965 predicted that the numbers of components on the chip will double every 18 months. Initially he predicted only for 10 years but due to growth in the integrated circuit technology his prediction is valid till today. His work is widely recognised as the Moore's law. The effect of Moore's law was studied carefully and researches have come to the conclusion that as the number of components in the chip increases the power dissipation will also increase tremendously. It is also predicted that the amount of power dissipated will be equal to the heat

dissipated by the rocket nozzle. Hence power minimization has become an important factor for today's VLSI engineers.

Launder [2] determined that, the amount of energy dissipated for the loss of each bit of information is at least kTln2. During any computation the intermediate bits used to compute the final result are lost, this loss of bits is one of the main reason for the power dissipation.

C. H. Bennett [3] in 1973 discovered that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model. The theory is proved with Turing machine which is a symbolic model for computation developed by Turing. Bennett also showed that the computations that are performed on irreversible or classical machine can be performed with same efficiency on the reversible machine. Based on the above concept the research on the reversibility was started in 1980's.

Soolmaz Abbasalizadeh [4] has designed 4-Bit Comparator Based on Reversible Logic Gates. Here he explained that reversible logic has been considered as one of the promising practical strategies for power-efficient computing. In fact, when the inputs can't be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs. The number of inputs and outputs are equal, and inputs can be recovered from outputs. In order to achieve optimized reversible circuits, the following points should be considered:

1) Fan-out is forbidden.
2) Feedbacks and loops are not allowed.
3) Delay should be minimum.
4) Optimization parameters should be minimum.

The parameters such as number of reversible gates, number of constant inputs, garbage outputs and quantum cost can be named as optimization parameters and as defined as:

1) The inputs, which equal to 0 or 1, are constant inputs.
2) Garbage outputs are output vectors which do not generates any useful functions.
3) Quantum cost refers to the cost of the circuits in ters of primitive gates.

Edward Fredkin and Tommaso Toffoli [5] introduced new reversible gates known as fredkin and Toffoli reversible gates based on the concept of reversibility. These gates have zero power dissipation and are used as universal gates in the reversible circuits.These gates have three outputs and three inputs, hence they are known as 3*3 reversible gates.

In the year 1994 shor [6] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.
Peres [7] introduced a new gate known as Peres gate. Peres gate is also a 3*3 gate but it is not a universal gate like the Fredkin and Toffoli gate. Even though this gate is not universal gate it is widely used in much application because it has less quantum cost with respect to the universal gate. The quantum cost of the Peres gate is 4.

H Thalpliyal and N Ranganathan [8] invented a reversible gate known as TR gate. The main purpose of introducing this reversible TR gate was to decrease the garbage output in a reversible circuit.

H Thalpliyal and N Ranganathan [9] introduced the reversible logic to sequential circuits. Implementation of the sequential circuit such as D-latch, T latch, JK latch and SR latch using Fredkin and Feynman gate has been done. After this work more research has been done on sequential circuits using reversible gates.

Using the combination of Fredkin and Feynman gate a new gate known as Sayem gate was proposed by Sujata S. Chiwande Prashanth R. Yelekar [10] sayem gate is a 4*4 reversible gate and is used in designing sequential reversible circuits.

M.L. Chuang and C.Y. Wang [11] proposed that the numbers of gates, the number of garbage output were reduced in implementing the Latches and when the results will be compared [10] with 25% improvement was achieved.

Arunkumar P Chavan [12] has proposed the pulse detector and unsigned multiplier. He also explained the 4-Bit reversible PISO Shift register. Here the 4-bit PISO shift registers uses four reversible clocked D flip-flops and four Fredkin Gates. Reversible Fredkin Gate is used to develop a multiplier with an enable signal. Similarly a basic 3-bit reversible SIPO shift register can be constructed using three reversible clocked D flip flops and two Feynman gates.

Gopal, Lenin; Mohd Mahayadin and Nor Syahira [13] investigated the ALU designed to show its major implications on the Central Processing Unit (CPU).In this paper, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

Kaur, T. and Singh, N. [14], In this research work, the basic concepts of reversible circuits are briefly discussed. Furthermore, an efficient & low cost fault tolerant reversible Arithmetic and logical unit (ALU) is designed and implemented. The results are then compared with the existing design. The large garbage outputs in the proposed design are compensated by the number of operations that it can perform. The Proposed design can perform almost all arithmetic and logical operations on the other hand existing design performs only four operations.

Rakshith, T.R. and Saligram, R. [15] estimated the power dissipation is an important design criterion during the VLSI process flow. Reversible logic is one of the promising fields having a wide range of applications starting from low power VLSI design, fault tolerant circuits, quantum computing to fields such as bio informatics. An ALU may be regarded as the processor's numerical calculator and logical operation evaluator. In this paper a fault tolerant reversible ALU design is proposed. Parity preserving logic gates are the main component in this design. A parity preserving gate is the one in which the parity of the input and the output vectors is the same. The proposed ALU can produce up to 16 logical and 16 arithmetic operations.

Syamala, Y. and Tilak, A.V.N., [16] researched on a function is reversible if each input vector produces a unique output vector. Reversible logic is of growing importance to many future computer technologies. In this paper, the design of a reversible Arithmetic Logic Unit (ALU) is presented making use of multiplexer unit as well as control signals. ALU is one of the most important components of CPU that can be part of a programmable reversible computing device such as a quantum computer. In multiplexer based ALU the operations are performed depending on the selection line. The control unit based ALU is developed with 9n elementary reversible gates for four basic arithmetic logical operations on two n-bit operands. The series of operations are performed on the same line depending on control signals, instead of selecting the desired result by a multiplexer. The later design is found to be advantageous over the former in terms of number of garbage outputs and constant inputs produced.
In 2014,Neeta Pandey et.al,proposed 2:4 reversible decoder and 3:8 reversible decoder using Feynman and Fredkin gate. They also implemented Feynman and Fredkin gate using transmission gates. They were also compared the various parameters of proposed decoders with exiting decoders [17].

In july 2014, Ashima Malhotra, et.al, proposed different types of reversible multiplexers using modified Fredkin gate. They were proposed 2:1,4:1,8:1 and 16:1 reversible multiplexers. They were also compared with quantum cost and power consumption of proposed reversible multiplexers with exiting one [18].

In July 2014, Ashima Malhotra, et.al, described that reversible modified Fredkin gate used to designed multiplexers. They also compared the quantum cost of multiplexers designed using Fredkin gate with multiplexers designed using modified Fredkin gate[19].

Panchal et al.[20] (2013) proposed an 4x4 reversible multiplier circuit which is implemented using Peres and Toffoli reversible gate and compared with the existing designs , The proposed reversible multiplier is better in terms of hardware complexity, number of gates, garbage output, constant inputs and total quantum cost.

H.Thapliyal, M .B. Srinivas and Mark Zwolinski [21] proposed a reversible D -flip-flop using New gate and Feynman gate. The drawback of this work is that it requires more number of reversible gates and produces more number of garage outputs. As the number of reversible gates required is more, it also increases the quantum cost of their flip-flop.

H.Thapliyal and M.B.Srinivas [22] proposed a reversible D-latch using two Fredkin gates. The drawback of their work is the quantum cost to realize a reversible D-latch with both the outputs Q and Q' is 10. However, to realize a reversible master-slave D-flip-flop 5 Fredkin gates are used which increases t he quantum cost.

Rice [23] proposed a reversible S R latch and all the other latches were designed as the sub-units from reversible RS latch as a part of master-slave flipflops.

Thapliyal and Vinod [24] proposed the designs of reversible latches and flip flops. The proposed designs were shown to be better than the designs presented in Rice [23] in terms of the number of reversible gates and garbage outputs. The quantum cost of the reversible D-latch proposed by Thapliyal and Vinod is 10.

H.Thapliyal and N.Ranganathan [25] proposed a negative enabled reversible D - Latch using Fredkin gate. The advantage of this work is that it does not require the inversion of CLK pulse to realize the master-slave D-flip-flop. To realize both the outputs Q and Q', it requires 1 Fredkin gate and 2 Feynman gates and the quantum cost of their implementation is 7. The transistor implementation is not addressed in this work.

Md. Selim Almamun, Indrani mandal, Md. Hasanuzzaman [26] proposed a reversible D-latch using MG-1 gate. In this work the number of XOR operations involved in realizing a M G-1 gate is more which will increase the transistor count.

S.Ranjith, T.Ravi and E.Logashanmugam [27] proposed a reversible R R gate using which a reversible D-Flip-flop has been realized. The drawback of their work is that to realize a master slave flip-flop an additional reversible gate is required to produce the complement of the clock signal and further to realize the flip-flop with both the outputs Q and Q' one more reversible gate is in need to produce Q'. Thus, the

number of reversible gates required is more which in addition will increase the transistor count.

3. CONCLUSIONS

The main aim is to design and implement the reversible logic based Flip flop. As a prior work, literature survey has been done. It is observed that, there are many innovative ideas and solutions are put forth for the power optimization by many researchers.

So observing all these white papers, one can ensure that reversible logic would be one of the better solutions for the designing of Flip flop in order to reduce power and secure data in sequential circuit

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