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Quantum Mechanical Effects in Sub-40nm Dual Material Double Gate Junctionless Nanowire Transistor(DMDG JLNT)

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Abstract - : *In this paper an investigation on the quantum mechanical effects on gate capacitance, threshold voltage and surface potential of highly downscaled Dual Material Double Gate Junctionless Nanowire Transistor(DMDG JLNT) has been carried out. We have observed a small quantum deviation from the classical model while determining various device parameters of DMDG JLNT in sub-40nm regime.*

***Key Words*: Quantum Mechanical Effect, Quantum Capacitance, Threshold Voltage, Surface Potential.**

1.INTRODUCTION

The continuous downscaling of semiconductor devices has led us to think about the constraints that might let the device performance go below our expectations. To achieve the goals like high speed, better transcoductance, reduced SCE(Short Channel Effects), higher noise margin(NM) and better analog and digital performances, we have used DMDG JLNT as a promising alternative for MOS technology in sub-40nm regime. As we scale down the device dimension, quantum mechanical effect plays an important role in determining device parameters. Quantum capacitance effect also has been taken into consideration while determining gate capacitance which often comes into play in nano scaled device. Quantum capacitance is related to the density of states(DOS).The 2-dimensional electron gas results a capacitance in series with the oxide capacitance. The quantum capacitance strongly decreases when the channel dimensions are scaled[1]. Which should have resulted in strong decrease of gate capacitance, which is true classically. But something different happens as the gate capacitance increases with the continuous reduction of the silicon film thickness below 7nm[1]. We have demonstrated the quantum effects on the threshold voltage determination of DMDG JLNT. Along with that we have also presented its effect on surface potential under full depletion and partial depletion.

2. 3-D STRUCTURE OF DMDG JLNT

Figure-1 shows the 3-D structure of DMDG JLNT. The metal gate near to the source is padded with higher work-function so to enhance the fast transportation of carriers to the drain side through the channel to increase the drain current. Which in turn results in higher operating frequency of the device .We have also used high-k spacer to enhance the fringing electric fields through the spacer[2].

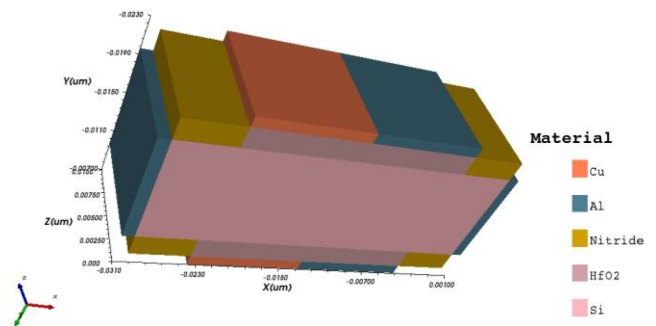

Fig-1: 3-D Structure Of DMDG-JLNT

3. ANALYTICAL MODEL

The gate capacitance can be expressed as,

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_Q}$$

$$\Rightarrow C_G = \frac{C_{ox} \times C_Q}{C_{ox} + C_Q} \qquad (1)$$

Where, the quantum capacitance[4],

$$C_Q = \frac{m^* e^2}{\pi \hbar^2} \qquad (2)$$

Where, m^* = The effective electron mass in the direction perpendicular to the quantum plane.

On simplification,

$$C_G = \frac{\varepsilon_{ox} e^2 m^*}{\varepsilon_{ox} \hbar^2 \pi + e^2 m^* t_{ox}} \qquad (3)$$

The threshold voltage of DMDG JLNT given by [3] can be re-written as,

$$V_{th} = V_{fb1} - \frac{qN_D}{8\varepsilon_{si}} t_{si}^2 - \frac{qN_D}{2\varepsilon_{ox}} t_{si} t_{ox} + V - 3V_t - \frac{4C_{si}}{C_G} V_t \quad (4)$$

Where,

V_{fb1} = Flat-band voltage for gate-1

N_D = Doping Concentration.

$V_t = \frac{kT}{q}$, V = Quasi fermi potential

t_{ox} ,t_{si} = Oxide and silicon thickness respectively.
k= Boltzmann Constant, T=Temperature, q=charge.
Now, including the quantum capacitance effect, the surface potential in [3] can be written as,

For the region under gate-1,

$$\psi_{s1}^* = \alpha_1 e^{\lambda_1 x} + \beta_1 e^{-\lambda_1 x} - \frac{\theta_1^*}{\gamma}; 0 \le x \le L_1 \quad (5)$$

For the region under gate-2,

$$\psi_{s2}^* = \alpha_2 e^{\lambda_2 (x-L_1)} + \beta_2 e^{-\lambda_2 (x-L_1)} - \frac{\theta_2^*}{\gamma}; L_1 \le x \le L \quad (6)$$

Where,

$$\theta_i^* = -\left\{ \frac{qN_D}{\varepsilon_{si} V_t} + \gamma V_{th} \right\} \quad (7)$$

$$\gamma = \left(\frac{2C_G}{t_{si}} + \frac{qN_D}{\varepsilon_{si} V_t} \right) \quad (8)$$

Where, L_1, L_2= Length of the channel under gate-1, gate-2 respectively.

3. RESULT AND DISCUSSION

As we scale down the device dimension, the impact of quantum capacitance reduces extremely[1]. Which implies that the gate capacitance should also have been reduced in parallel. From the equation (1,2,3) we can see that, as C_Q decreases, C_G also decreases. Which in turn implies that the threshold voltage should also have been reduced respectively. But a contrast is seen, as we scale down the silicon thickness below 7nm. The gate capacitance increases as we move down the silicon _lm thickness below 7nm.Which increases the threshold voltage shown in figure-2. In the equation (6), if threshold voltage increases, θ_i^* decreases. Now, if θ_i^* decreases then ψ_{s1}^* and ψ_{s2}^* increases. Which implies that there will be more electrostatic potential energy in the surface confined charges. This is shown in the figure-3.

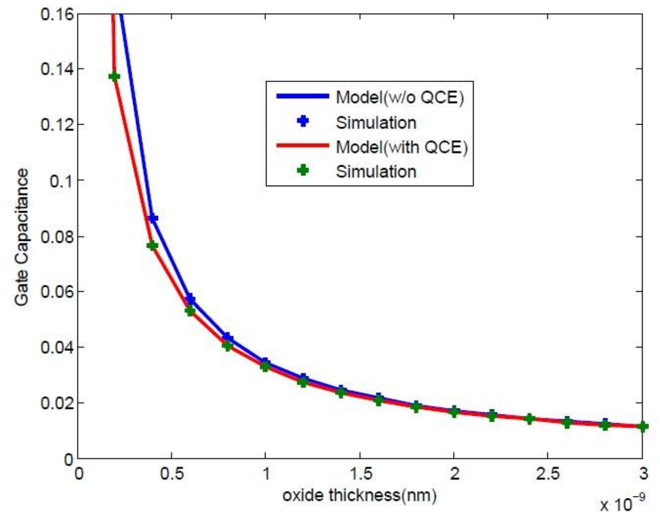

Fig-2: Gate Capacitance w.r.t oxide thickness with Quantum Capacitance Effect(QCE) and without QCE.

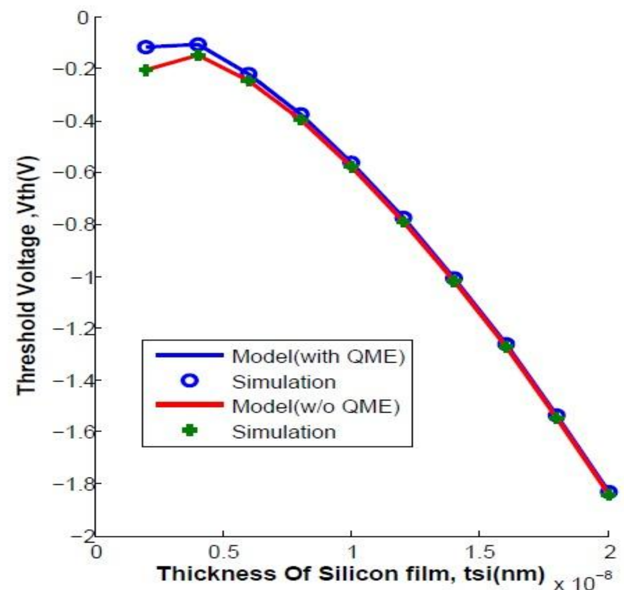

Figure-3: Threshold voltage w.r.t silicon thickness with Quantum Mechanical Effect(QME) and without QME.

Table -1: TCAD Design Parameter

Oxide Thickness	t_{ox}	2nm
Silicon Thickness	t_{si}	7nm
Channel Length	L_{ch}	20nm
Spacer used	Si_3N_4	
Oxide Material	HfO_2	
Gate-1,Gate-2	Cu(5.12)	Al(4.25)

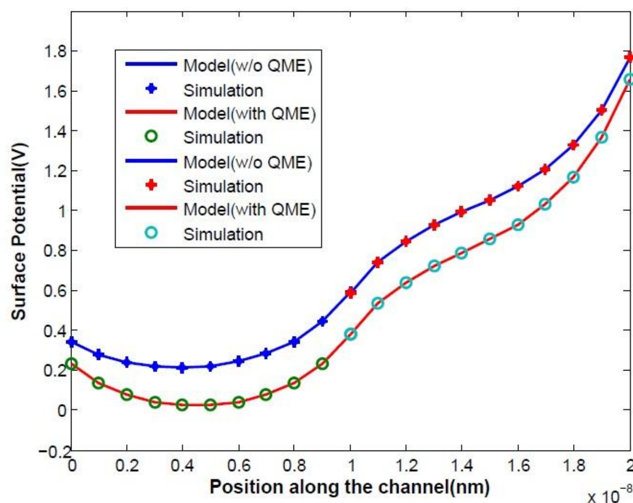

Figure-4: Surface potential along the channel with Quantum Mechanical Effect(QME) and without QME.

4. CONCLUSION

From the above results, we can conclude that the quantum effect has been observed while determining the threshold voltage and surface potential of DMDG JLNT. Since, gate capacitance is an important parameter to be determined to measure the delays in CMOS technology. We have also demonstrated the quantum capacitance effect on gate capacitance.

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